Green-Mode PWM Controller with Primary Side Feedback

Rev.00

General Description

The LD7510/J is an excellent primary side feedback controller, which integrates several functions of protections. It minimizes the components counts and is available in a tiny SOT-26 package. Those make it an ideal design for low cost applications.

It provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD7510/J features OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent the circuit being damaged from the abnormal conditions.

In most cases, the power supply with primary-side feedback controller would accompany with some serious load regulation effect. To deal with this problem, the LD7510/J consists of dedicated load regulation compensation circuit to improve it.

Patent Pending

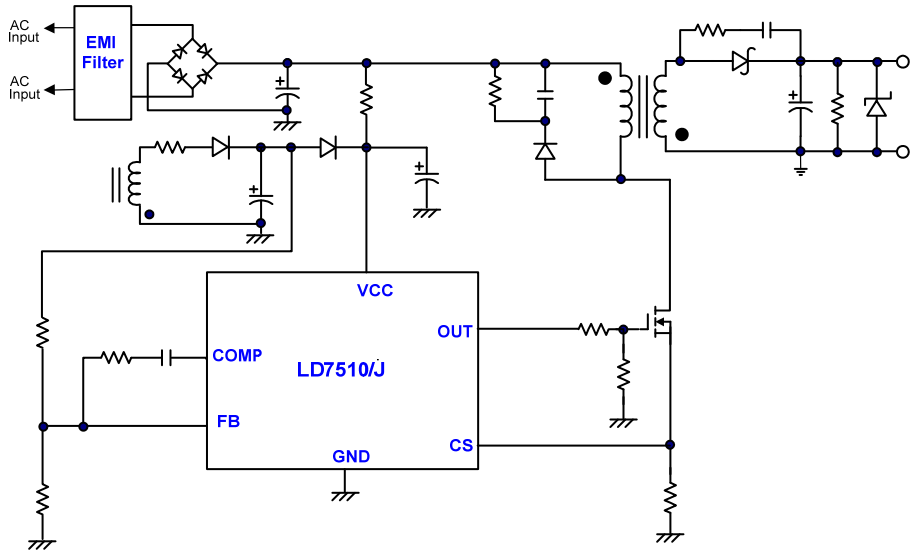
Features

- Primary-side feedback control
- Built-in Load Regulation Compensation
- Built-in Slope Compensation with 75% max duty-cycle
- Low Startup Current (<20μA)
- Current Mode Control with Cycle-by-Cycle Current Limit
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- 300mA Driving Capability

Applications

- Replace for Linear Transformer and RCC SMPS.
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- Auxiliary Power Supply

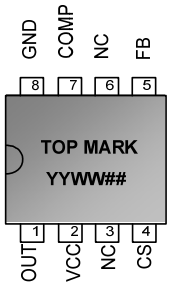
Typical Application



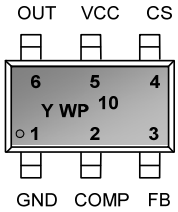
Pin Configuration

LD7510

DIP- 8 (TOP VIEW)



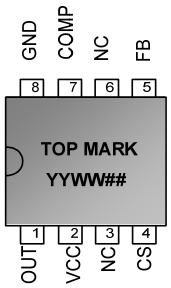
SOT- 26 (TOP VIEW)



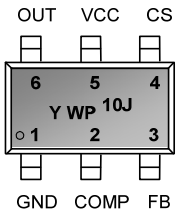
YY, Y : Year code (D: 2004, E: 2005..)
WW, W : Week code
P : LD75..
(Product family code)
: Production code

LD7510J

DIP- 8 (TOP VIEW)



SOT- 26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005..)
WW, W : Week code
P : LD75..
(Product family code)
: Production code

Ordering Information

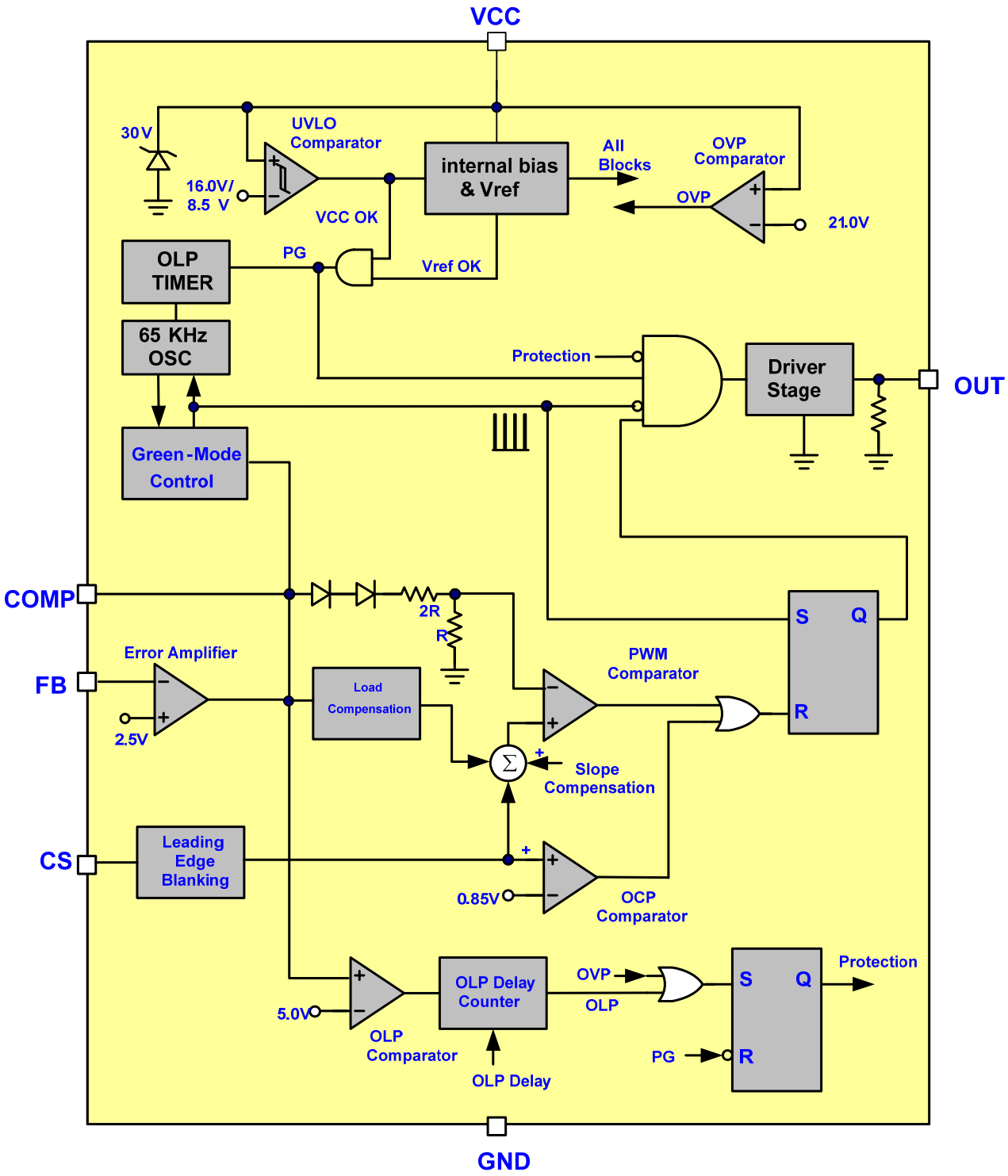
Part number	Jitter	Package		TOP MARK	Shipping
LD7510 GL	No	SOT-26	Green Package	YWP/10	3000 /tape & reel
LD7510 GN	No	DIP-8	Green Package	LD7510GN	3600 /tube /Carton
LD7510J GL	Yes	SOT-26	Green Package	YWP/10J	3000 /tape & reel
LD7510J GN	Yes	DIP-8	Green Package	LD7510JGN	3600 /tube /Carton

The LD7510 and LD7510J are ROHS compliant/Green package.

Pin Descriptions

NAME	PIN (SOT-26)	Pin (DIP-8)	FUNCTION
GND	1	8	Ground
COMP	2	7	Output of the error amplifier for voltage compensation
FB	3	5	Inverting input to the error amplifier
CS	4	4	Current sense pin, connect it to sense the MOSFET current
VCC	5	2	Supply voltage pin
OUT	6	1	Gate drive output to drive the external MOSFET
NC	-	3,6	NC Pin

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
COMP, FB, CS	-0.3 ~7V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 120°C
Operating Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26)	250°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	300mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	10	20	V
Start-up capacitor	2.2	22	μF
Start-up resistor	1.0	4.7	MΩ

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			10	20	μA
Operating Current (with 1nF load on OUT pin)	VFB=3.0V, V_{COMP}=0V		2.25		mA
	$R_{COMP-FB}$=20K, R_{FB-GND}=100K		3.6		mA
	Protection tripped (OLP)		0.65		mA
	Protection tripped (OVP)		0.7		mA
UVLO (off)		7.5	8.5	9.5	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		19.5	21	22.5	V
Error Amplifier					
Feedback Input Voltage	FB=COMP	2.475	2.5	2.525	V
Load Compensation Current	$R_{COMP-FB}$=20K, Vcs=0.7V		-27		μA
Output Sink Current	V_{FB}=2.7V, Comp=1.1V		6		mA
Output Source Current	V_{FB}=2.3V, Comp=4.9V		-2.5		mA
High-level Output Voltage	V_{FB}=2.3V, RL=15 KΩ to GND	5.5			V
Low-level Output Voltage	V_{FB}=2.7V, RL=15 KΩ to GND			1.2	V
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.80	0.85	0.90	V
Leading Edge Blanking Time			225		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency	COMP=4.5V	60	65	70	KHz
Green Mode Frequency	COMP=4.5V		21		KHz
Trembling Frequency	COMP=4.5V LD7510J exclusively.		± 4.5		KHz
Modulation Frequency	LD7510J exclusively		180		Hz
Temp. Stability	(-20°C ~105°C)			5	%
Voltage Stability	(V_{CC}=11V-19.5V)			1	%
Comp Pin Detect					
Green Mode Threshold Voltage			2.5		V
Burst Mode Threshold Voltage			1.6		V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, Io=20mA			1	V
Output High Level	V_{CC}=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF		180	250	nS
Falling Time	Load Capacitance=1000pF		60	100	nS
Maximum Duty			75		%
OLP (Over Load Protection)					
OLP Trip Level	V_{COMP} (OLP)		5		V
OLP Delay Time			107		mS

Typical Performance Characteristics

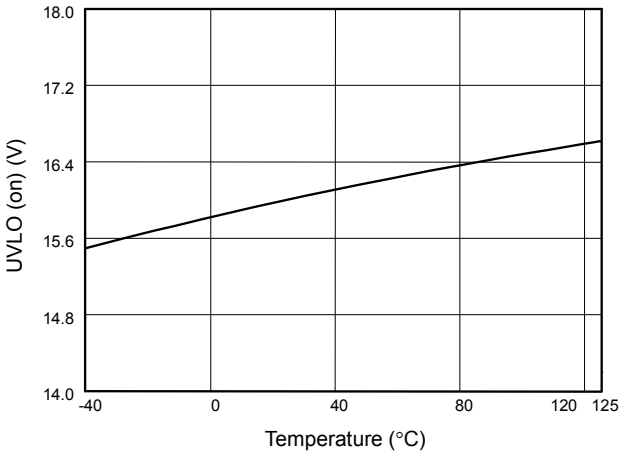


Fig. 1 UVLO (on) vs. Temperature

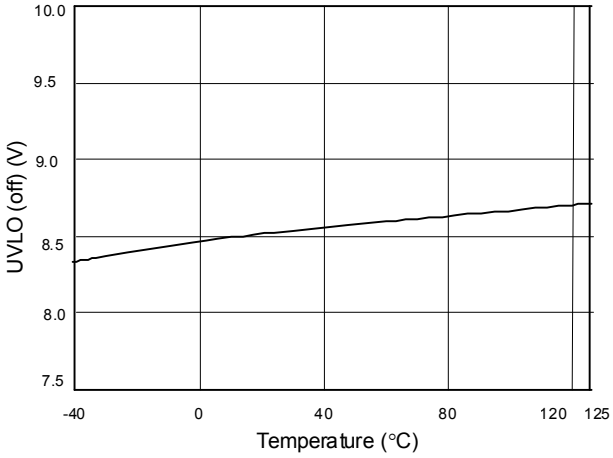


Fig. 2 UVLO (off) vs. Temperature

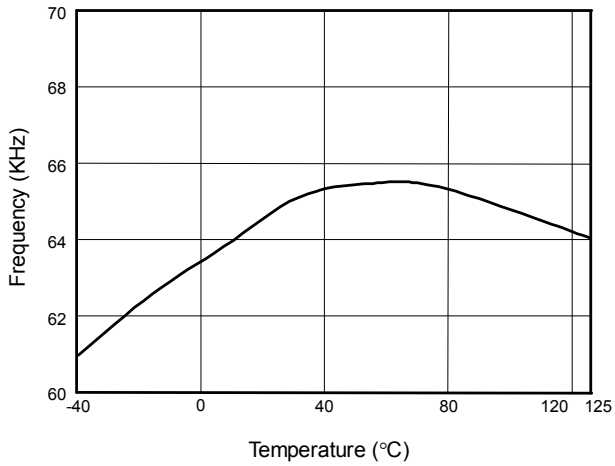


Fig. 3 Frequency vs. Temperature

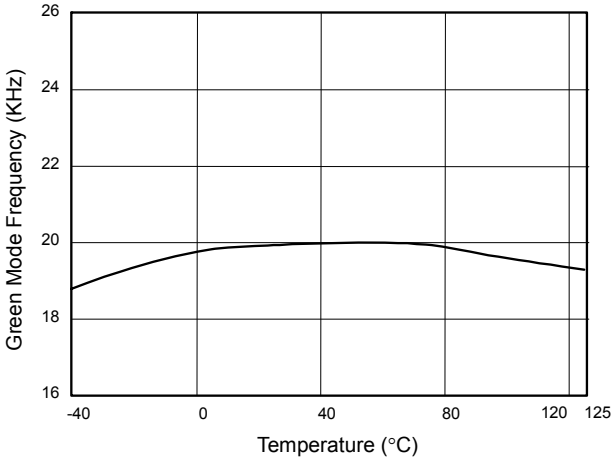


Fig. 4 Green Mode Frequency vs. Temperature

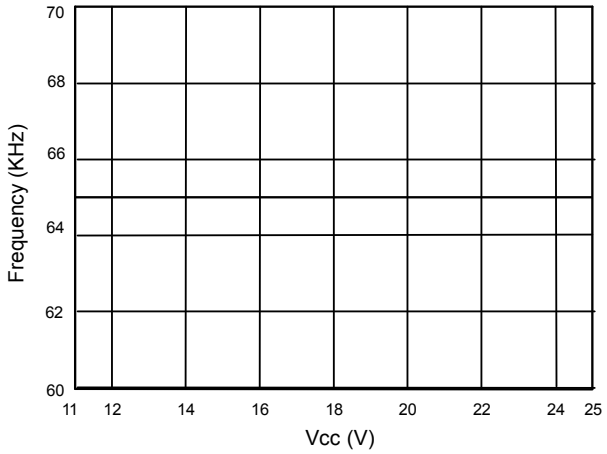


Fig. 5 Frequency vs. Vcc

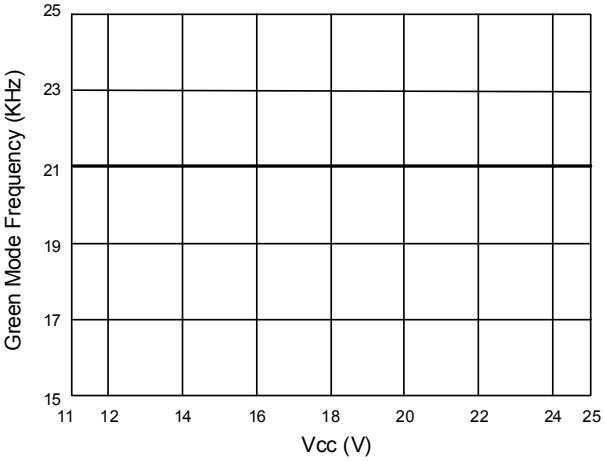


Fig. 6 Green Mode Frequency vs. Vcc

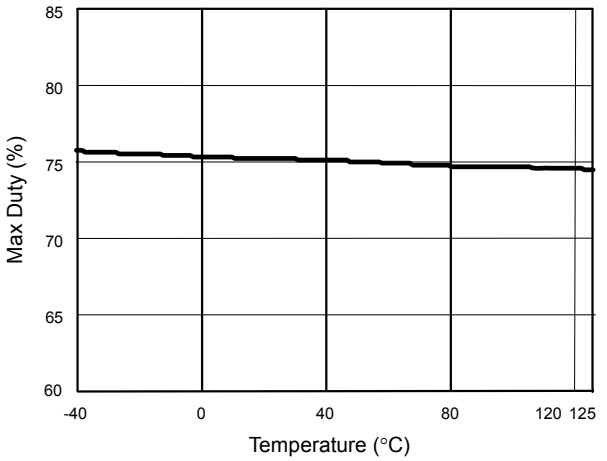


Fig. 7 Max Duty vs. Temperature

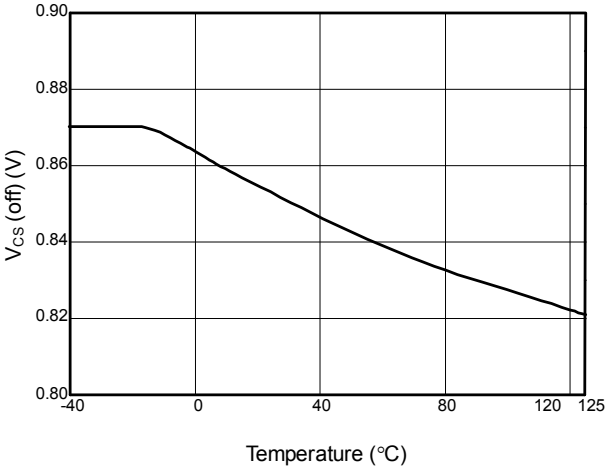


Fig. 8 V_{CS} (off) vs. Temperature

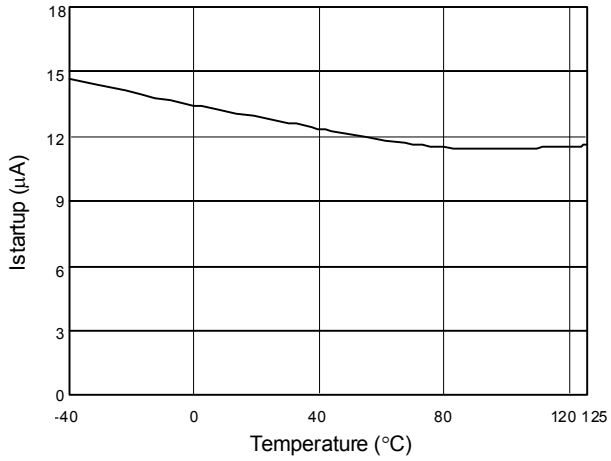


Fig. 9 Startup Current (Istartup) vs. Temperature

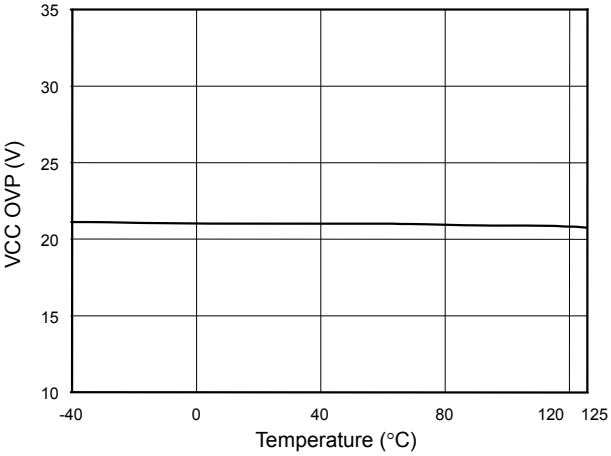


Fig. 10 VCC OVP vs. Temperature

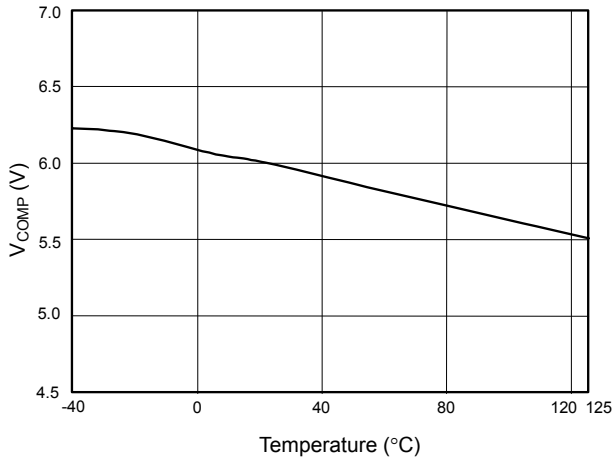


Fig. 11 V_{COMP} open loop voltage vs. Temperature

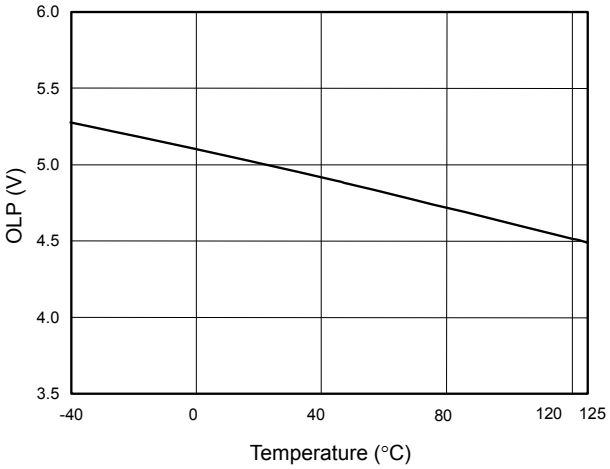


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7510/J is an excellent primary side feedback controller. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and board size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented to detect the voltage of VCC pin. It would assure the supply voltage enough to turn on the LD7510/J PWM controllers and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 8.5V, respectively.

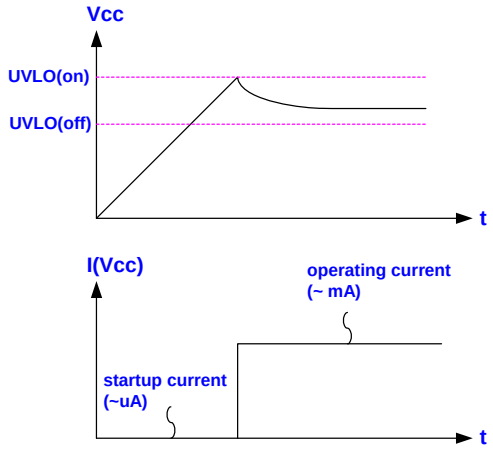


Fig. 13

Output Voltage setting

The LD7510/J monitors the auxiliary fly-back signal from FB pin through a resistor divider pair of Ra and Rb. An error signal, which represents the difference between the voltage at FB and the reference voltage, is integrated with the error amplifier to control switching duty cycle.

The output voltage is determined by the following relationship. For improving the output voltage accuracy, the transformer leakage inductance should be reduced as much as possible.

$$V_{OUT} = 2.5V(1+\frac{Ra}{Ra})(\frac{Ns}{Na})$$

Where,

Ra and Rb are the top and bottom feedback resistor value,

Ns and Na are the turn ratios of transformer secondary and auxiliary (as shown in the figure 14).

The load regulation and line regulation for primary side feedback control are sensitive to the structure of transformer. For getting good regulation and efficiency, the sandwich structure consisting of two secondary separate parallel layer windings surrounding primary winding is recommended.

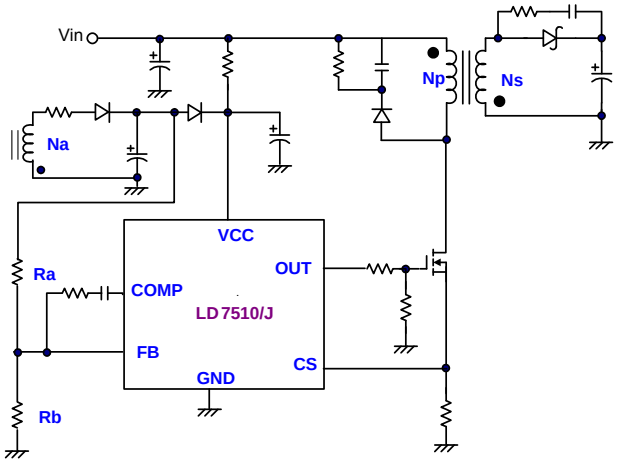


Fig.14

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7510/J Vcc is shown in Fig. 15. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7510/J to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. As soon as the Vcc voltage is high enough to turn on the LD7510/J and further to deliver the gate drive signal, the supply current will be provided from the auxiliary winding of the transformer. Lower startup current requirement for the PWM controller will help to increase the value of R1 and consume less power from R1. By using CMOS process and the special circuit design, the maximum startup current of LD7510/J is only 20μA.

It usually takes more time to start up while using a higher resistance value of R1. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

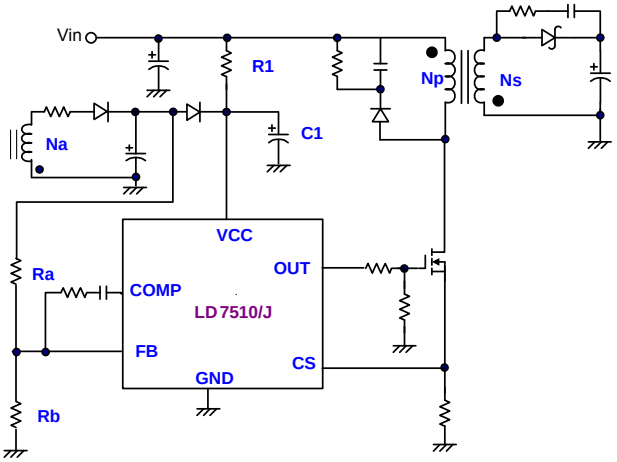


Fig. 15

Current Sensing, load compensation, and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieves regulation. The LD7510/J detects the primary MOSFET current from the CS pin for the peak current mode control and the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. In short, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 225nS leading-edge blanking (LEB) time is programmed in the input of CS pin to prevent false-triggering from the current spike. In some low-power applications, it's not necessary to include a R-C filter if the total pulse width of the turn-on spikes is less than 225nS and the negative spike on CS pin below -0.3V (as shown in the figure 16).

Nevertheless, the total pulse width of the turn-on spike usually correlates to output power, circuit design and PCB layout. In most high-power applications, it is strongly recommended to connect a smaller R-C filter (as shown in figure 17) to avoid the CS pin from damage by the negative turn-on spike.

CS pin also acts as load compensation's duty. The built-in dependent sink current source is proportional to the peak value of V_{CS}. This current sinks from FB pin to get an increment on V_{CC} and induces the secondary output voltage to rise and offset the voltage drop on circuit. The equation is I_{FB}=6+Vcspk*30 (μA)

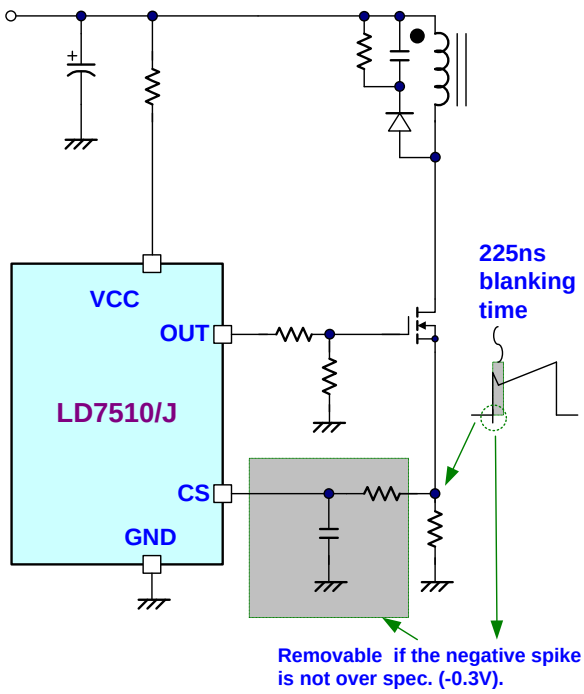


Fig. 16

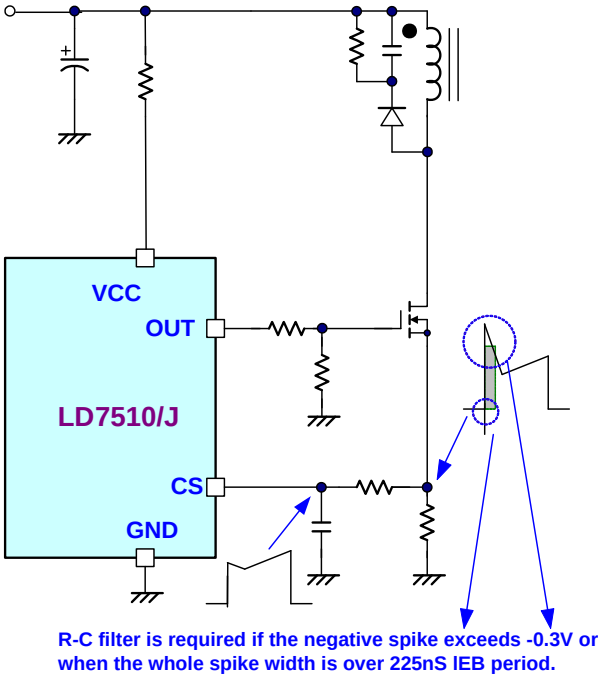


Fig. 17

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with a typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7510/J is limited to 75% to avoid the transformer saturation.

Oscillator and Switching Frequency

The switching frequency of LD7510/J is fixed at 65KHz internally to provide the optimized operations when considering the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

The stability is usually a critical issue for current mode controlling when it operates at a duty cycle in excess of 50%. As the conventional circuit UC384X does, most controllers gain slope compensation by injecting the ramp signal of the RT/CT pin to a coupling capacitor. LD7510/J possesses internal slope compensation to maintain the stability and is free from the extra circuit design.

Frequency Trembling (LD7510J exclusively)

The LD7510J is implemented with an adjustable modulating frequency for trembling function, which enables the power supply designers to achieve optimized EMI performance and excellent system cost. The trembling frequency is internally fixed between ±4.5KHz to incorporate with the 65KHz switching frequency.

Dual-Oscillator Green-Mode Operation

There are many different topologies implemented in different chips for the green-mode or power saving requirements, such as "burst-mode control", "skipping-cycle mode", "variable off-time control "…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using this dual-oscillator control, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are often limited up to max. 30V. To prevent the V_{GS} from the fault condition, LD7510/J is implemented with an OVP function on Vcc. No sooner than the Vcc voltage rises over OVP threshold voltage, the output gate drive circuit will be shutdown and stop the switching of the power MOSFET until the next UVLO(on) is present.

The Vcc OVP function in LD7510/J is an auto-recovery type protection. The figure 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will resume and the output will automatically recover normal operation.

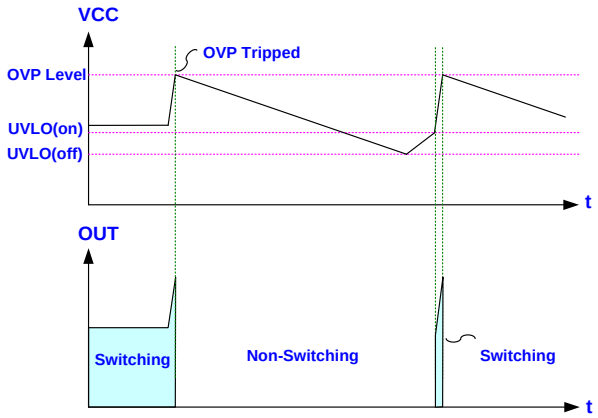


Fig. 18

Over Load Protection (OLP)

To protect the circuit from damage under over load condition or short condition, a smart OLP function is implemented in the LD7510/J. The figure 19 shows the waveforms of the OLP operation. In this case, the feedback system will force the voltage loop proceed toward the saturation and then pull up the voltage on COMP pin (V_{COMP}). Once the V_{COMP} trips over the OLP threshold 5V and stays for more than the OLP delay time (90mS), the protection will activate and then turn off the gate output to stop the switching of power circuit. With such protection mechanism, the average input power can be reduced to extremely low level, so the component temperature and stress can be controlled within the safe operating area.

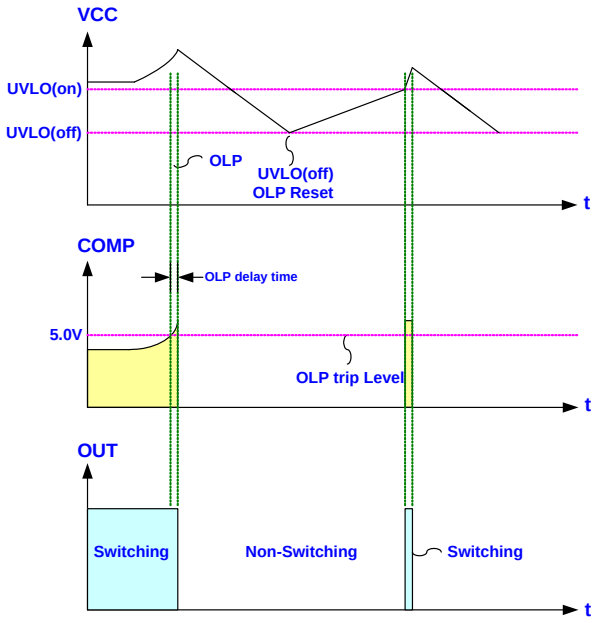
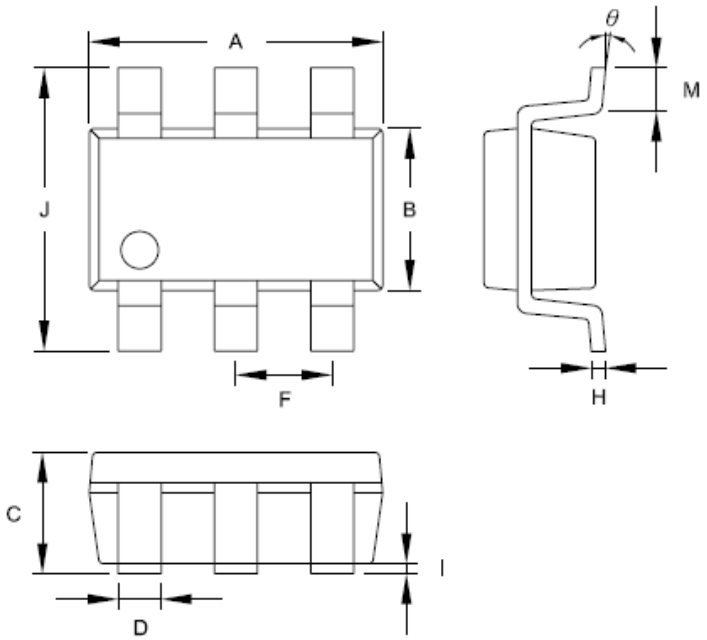

VCC
UVLO(on)
UVLO(off)
OLP
UVLO(off)
OLP Reset
t
COMP
OLP delay time
5.0V
OLP trip Level
t
OUT
Switching
Non-Switching
Switching
t

Fig. 19

Package Information

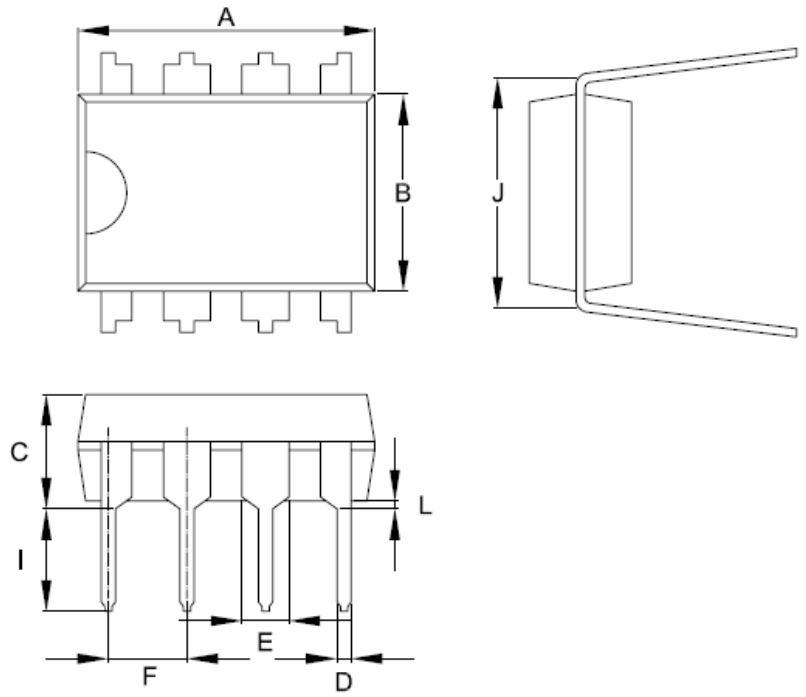
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.290	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	05/05/2009	Original Specification