Green-Mode PWM Controller with Latch off Protections

REV: 00

General Description

The LD7532A is specifically designed for low cost total-system by integrating many functions, protections, and EMI-improved solution in a SOT-26 package which usually need a lot of extra components or circuits on general system designs.

Furthermore, the CT pin latch function by injecting a high above 3.1V provides power circuit designers an easy way to deal with designs for protections, such as OVP and OTP, minimizing component cost and development time.

In order to satisfy different designs, the OVP trig level is adjustable by users adding a Zener diode from VCC pin to CT pin.

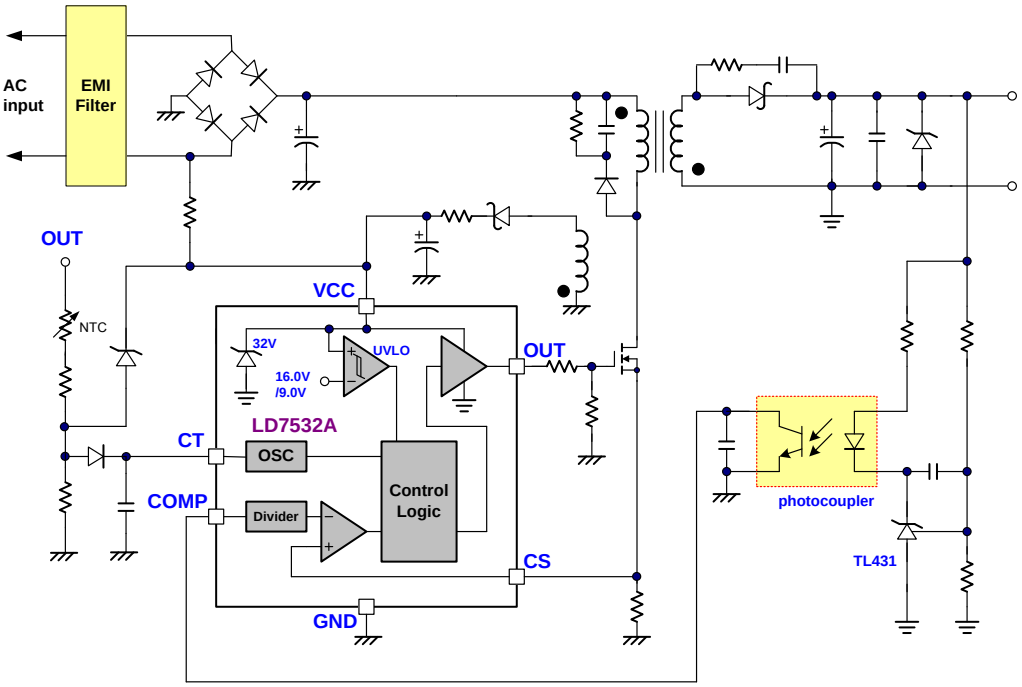
Features

- High-Voltage CMOS Process with ESD protection
- Very Low Startup Current (<20μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout) on VCC Pin
- LEB (Leading-Edge Blanking) on CS Pin
- Programmable OLP Delay Time
- Internal Slope Compensation
- External OVP Latch-off Protection
- OLP (Over Load Protection) Auto-recovery Mode
- External OTP Latch-off Protection
- 300mA Driving Capability

Applications

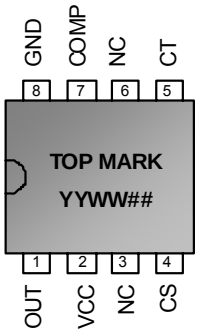
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application

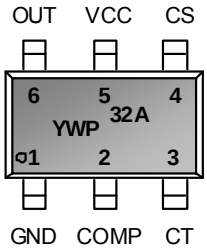


Pin Configuration

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W: Week code
P : LD75..
(Product family code)
: Production code

Ordering Information

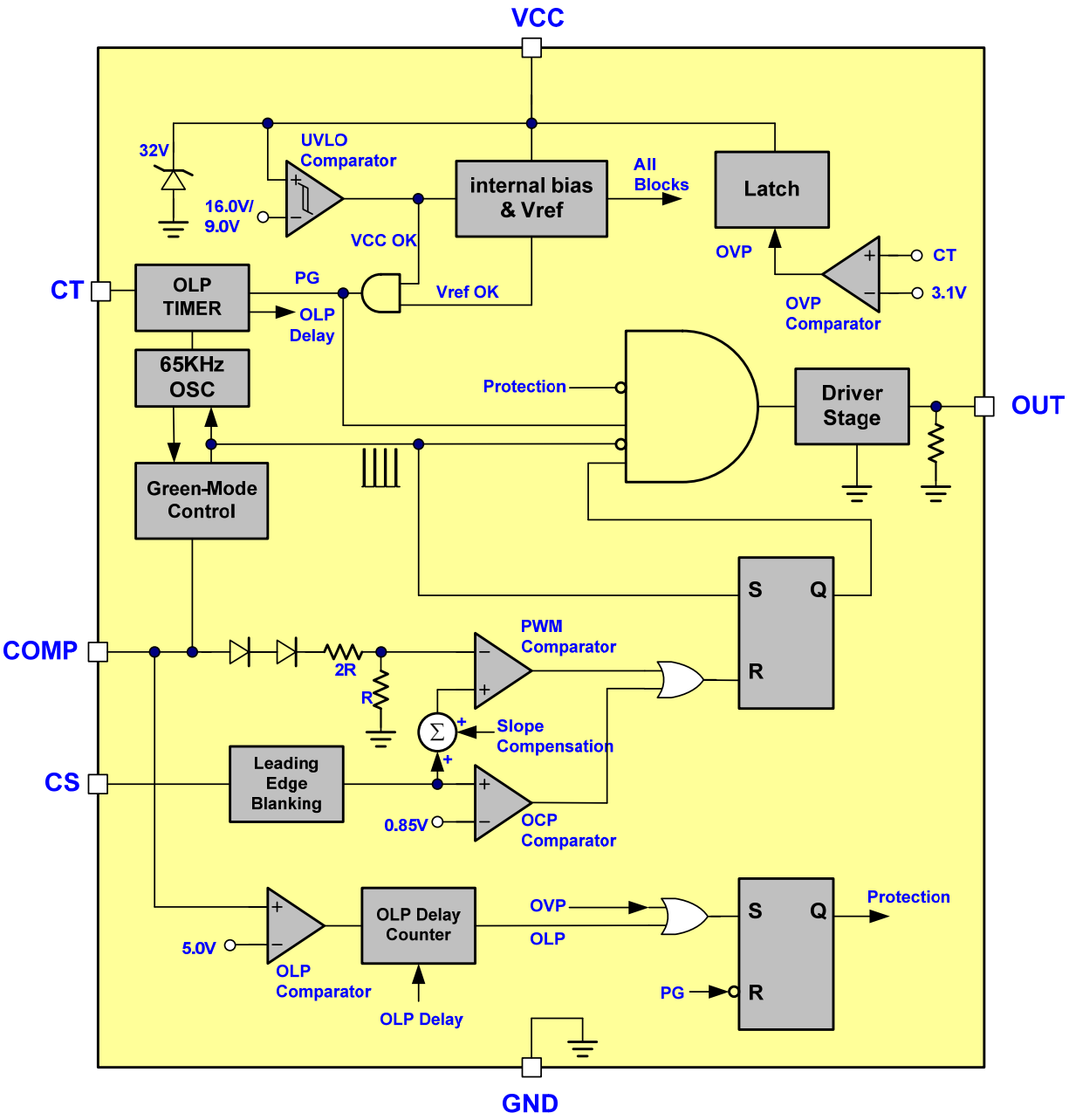
Part number	Package		TOP MARK	Shipping
LD7532A GL	SOT-26	Green Package	YWP/32A	3000 /tape & reel
LD7532A GN	DIP-8	Green Package	LD7532AGN	3600 /tube /Carton

The LD7532A is RoHS compliant.

Pin Descriptions

PIN SOT-26	PIN DIP-8	NAME	FUNCTION
1	8	GND	Ground
2	7	COMP	Voltage feedback pin (same as the COMP pin in UC384X), connected to a photo-coupler to close the control loop and achieve the regulation.
3	5	CT	This pin is to program the frequency of the low frequency timer. Connecting a capacitor to ground sets the trembling frequency and OLP delay time. This pin also provides another function of protection Latch.
4	4	CS	Current sense pin, connected to sense the external MOSFET current.
5	2	VCC	Supply voltage pin.
6	1	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
COMP, CT, CS	-0.3 ~7V
OUT	-0.3 ~VCC+0.3V
Junction Temperature	150°C
Operating Ambient Temperature	-20°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26)	250°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	300mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	11	25	V
CT Capacitor	0.047	0.1	μF
Comp pin Parallel Capacitor	0.001	0.1	μF
Startup Resister	540K	--	Ω

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			12	20	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.5		mA
	V_{COMP}=3V		3.0		mA
	I_{OLP}, OLP Tripped/ Auto		0.45		mA
	I_{OVP}, CT pin OVP Tripped/ Latch		1		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		1.5		mA
Open Loop Voltage	COMP pin open		6.0		V
OLP Current	COMP pin open		0.45		mA
Green Mode Threshold VCOMP			2.35		V
Burst Mode Threshold VCOMP			1.6		V
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.80	0.85	0.90	V
Leading Edge Blanking Time			220		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency		60	65	70	KHz
Trembling Range			± 3.5		KHz
Green Mode Frequency			20.5		KHz
Temp. Stability	(-40°C ~105°C)		5		%
Voltage Stability	(VCC=11V-25V)		1		%
FM Oscillator (CT pin)					
Timer Frequency	CT=0.047μF		220		Hz
OVP trigger level (Latch)		2.9	3.1	3.3	V
Holding Current	Vcc=7V(latched),		250		uA
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1.0	V
Output High Level	VCC=15V, Io=20mA	8			V

Electrical Characteristics

(Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Rising Time	Load Capacitance=1000pF		180	360	nS
Falling Time	Load Capacitance=1000pF		50	100	nS
Max. Duty	Load Capacitance=1000pF		75		%
OLP (Over Load Protection)					
OLP Trip Level	Vcomp(OLP)		5.0		V
OLP Delay time	CT=0.047μF		45		mS

Typical Performance Characteristics

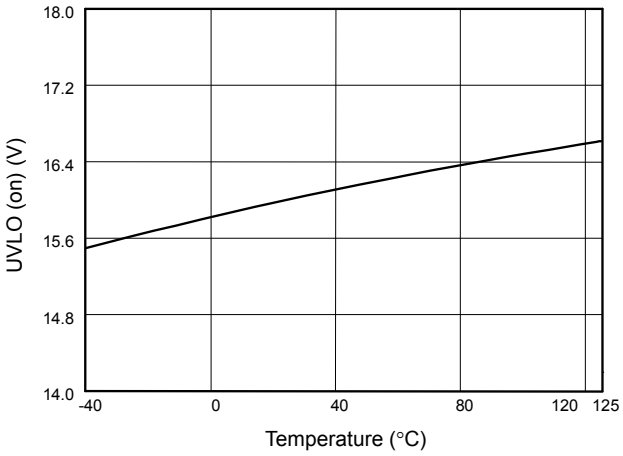


Fig. 1 UVLO (on) vs. Temperature

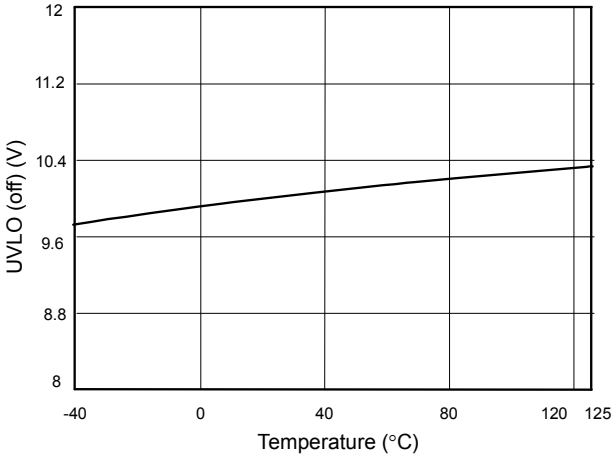


Fig. 2 UVLO (off) vs. Temperature

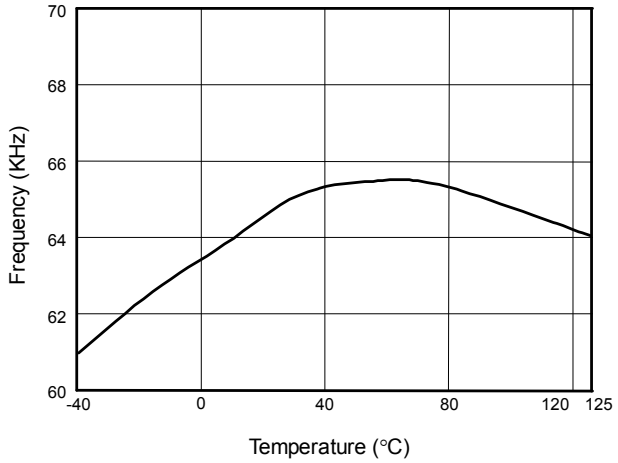


Fig. 3 Frequency vs. Temperature

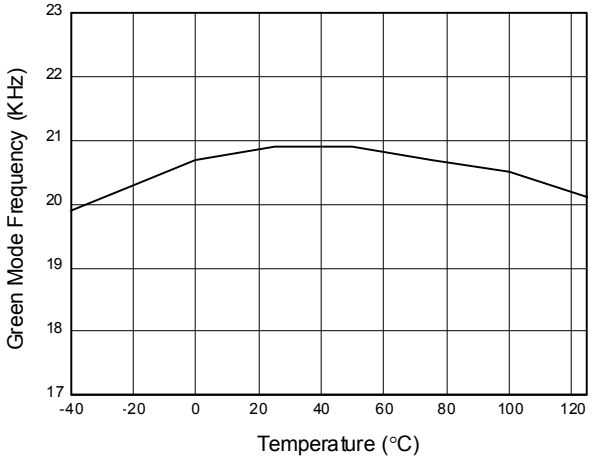


Fig. 4 Green Mode Frequency vs. Temperature

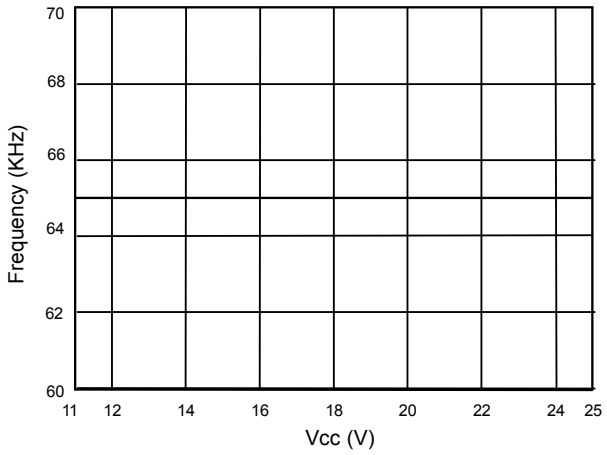


Fig. 5 Frequency vs. Vcc

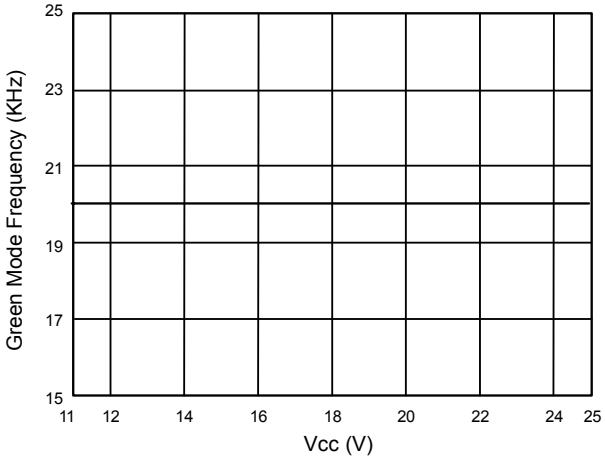


Fig. 6 Green Mode Frequency vs. Vcc

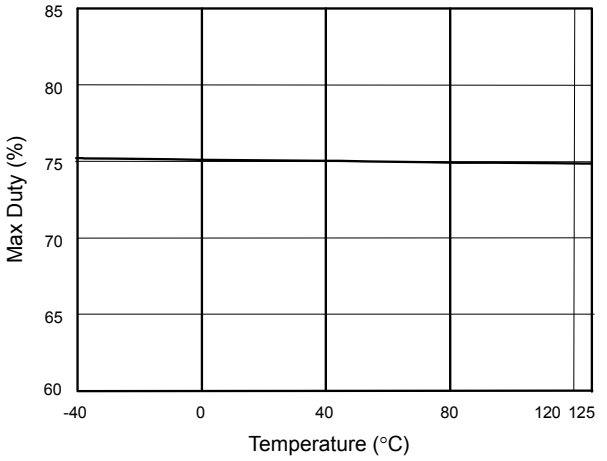


Fig. 7 Max Duty vs. Temperature

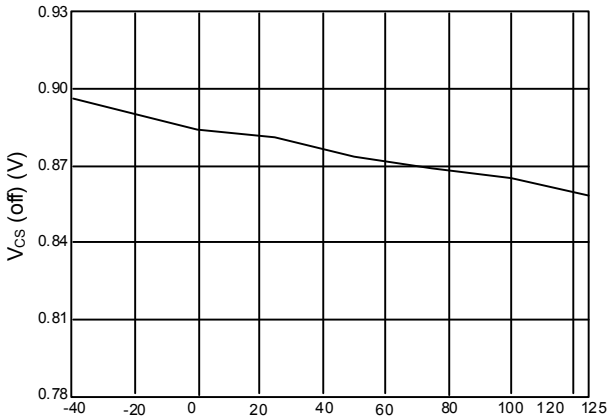


Fig. 8 V_{CS} (off) vs. Temperature

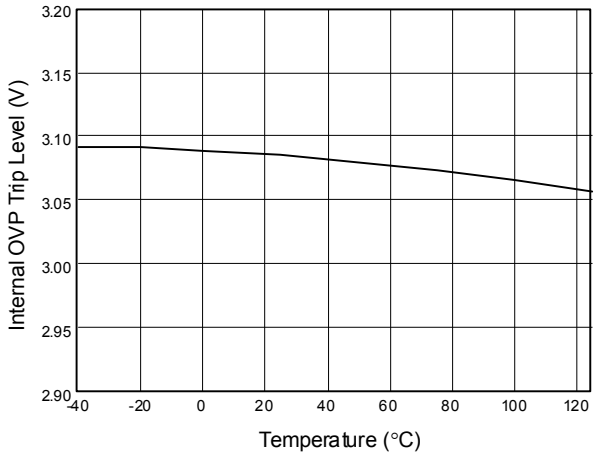


Fig. 9 Internal OVP Trip Level vs. Temperature (°C)

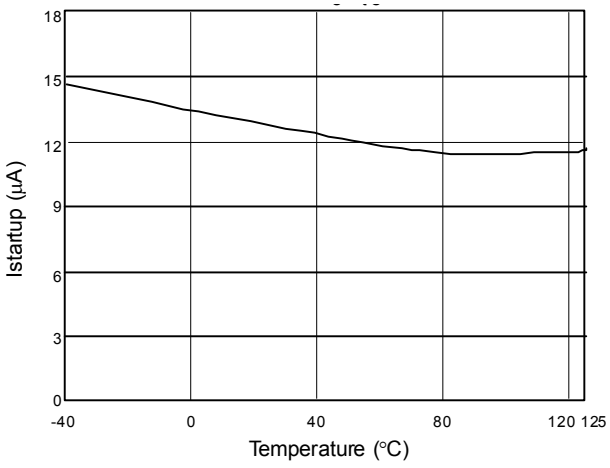


Fig. 10 Startup Current (Istartup) vs. Temperature

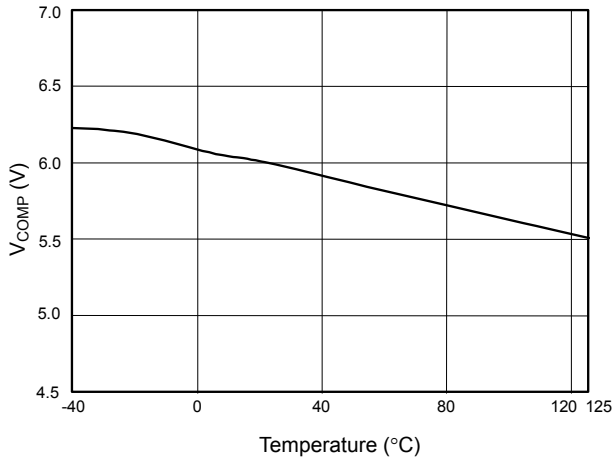


Fig. 11 V_{COMP} open loop voltage vs. Temperature

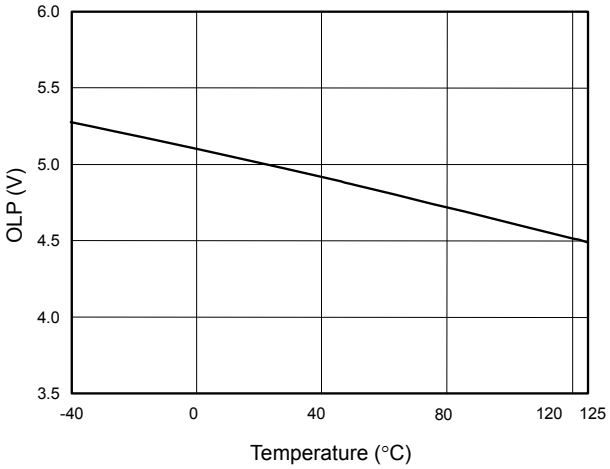


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7532A meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce the external components counts and the system size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage high enough to turn on the LD7532A PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown caused by the voltage dip during startup. The turn-on and turn-off threshold levels are set at 16.0V and 10.0V, respectively.

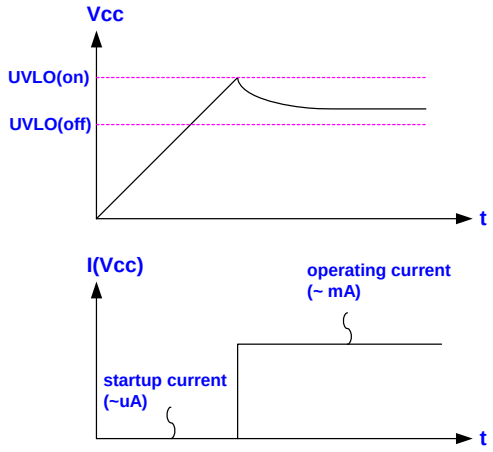


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate the LD7532A Vcc is shown in Fig. 14. During the startup transient, the Vcc is lower than the UVLO threshold thus there is no gate pulse produced from LD7532A to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the Vcc voltage is high enough to turn on the LD7532A and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement on the PWM controller will help increase the value of R1 and then reduce the power consumption on R1. Employing CMOS process

with special circuit design, the maximum startup current of LD7532A is only 20μA.

If a higher resistance value of the R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

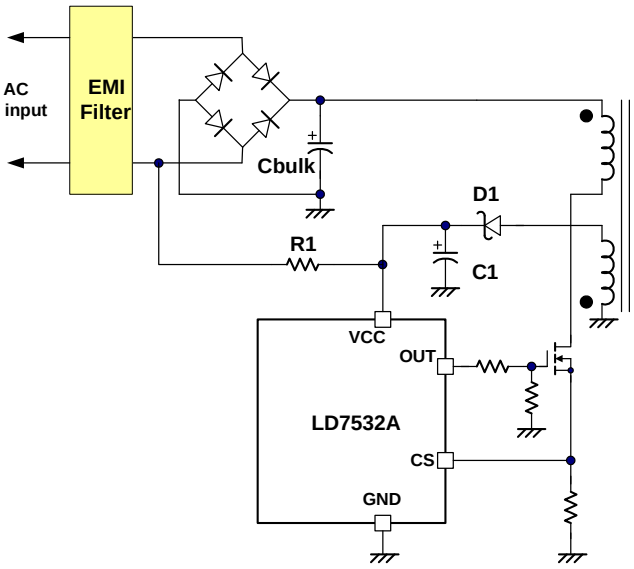


Fig. 14

Current Sensing and Leading-Edge Blanking

The typical current mode of PWM controller feeds back both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD7532A detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. Thus, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

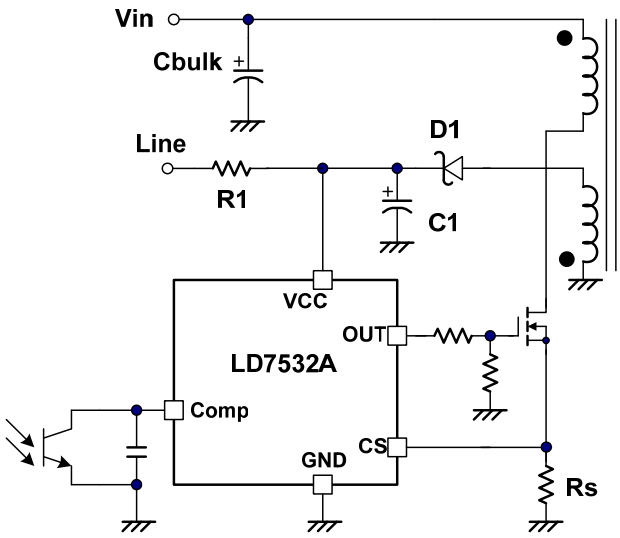


Fig. 15

A 220nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger caused by the current spike. In a low power application, if the total pulse width of the turn-on spikes is less than 220nS and the negative spike on the CS pin doesn't exceed -0.3V, the R-C filter as shown in the figure16 could be eliminated.

However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter as shown in figure 17 for higher power applications to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7532A is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7532A. Similar to UC3842, the LD7530/LD7530A would carry 2 diodes voltage offset at the stage before feeding the voltage feedback signal to the voltage divider at the ratio of 1/3, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally to eliminate the requirement of an external one.

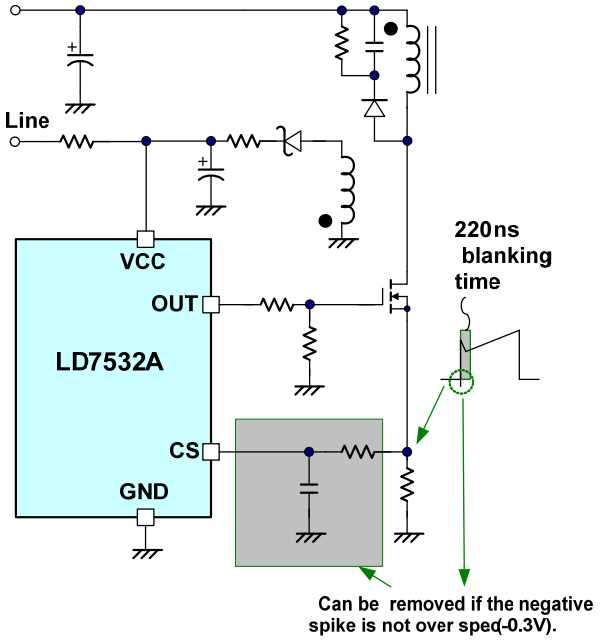


Fig. 16

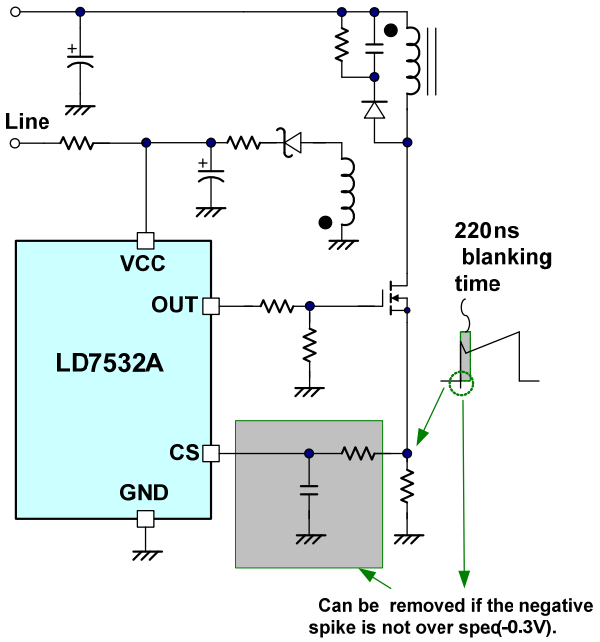


Fig. 17

Oscillator and Switching Frequency

The switching frequency of LD7532A is fixed as 65 KHz internally to provide the optimized operations, considering the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

In conventional applications, stability is a critical issue for current mode controlling, especially when it operates in the duty-cycle higher than 50%. As UC384X, LD7532A implements slope compensation by injecting the ramp signal of the RT/CT pin through a coupling capacitor. Slope compensation, as being integrated already, therefore requires no extra design for the LD7532A.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load conditions either by skipping some switching pulses or reducing the switching frequency.

Latch Off Control

The LD7532A can be latched off by injecting the CT pin a voltage signal higher than 3.1V. The gate output pin of the LD7532A will be disabled immediately under such condition. The off-mode can’t be released unless the VCC goes under a de-latch level by recycled the input power.

OVP/OTP Implementation on CT Pin

The OVP function is implemented by adding a Zener diode from VCC pin to CT pin. The protection is a latch type. If the OVP condition occurs, usually caused by the feedback loop opened, the Vcc will trip up to the OVP level (Vz+3.1V) and shutdown the output. The Vcc will be discharged to a low level for easily resetting. The figure 18 shows its operation.

The OTP function could be implemented by CT PIN connected a simple voltage-divider circuit composed with a proper N.T.C. thermistor connected from OUT pin to this pin. While temperature is rising and causing the resistance down, the CT pin voltage will rise to trigger the IC into latch mode. It could be released by recycling the input power the same as the OVP behavior.

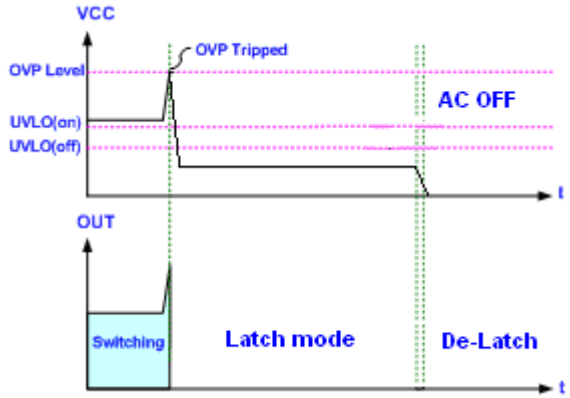


Fig. 18

Over Load Protection (OLP)

To protect circuits from being damaged under over load condition or short condition, a smart OLP function is implemented in the LD7532A. The figure 19 shows the waveforms of the OLP operation. In this case, the feedback system will force the voltage loop proceeding toward the saturation and then pull up the voltage on COMP pin (V_{COMP}). Whenever the V_{COMP} trips up to the OLP threshold 5V and stays longer than the OLP delay time, the protection will be activated to turn off the gate output and stop the switching of power circuit. The OLP delay time, set by CT pin, is to prevent any false trigger caused by the power-on and turn-off transient. The Higher the CT value is, the longer the OLP delay time. For recommendation, the OLP delay time is around 95mS when CT=0.1μF and will be around 45mS when CT=0.047μF.

By such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within the safe operating area.

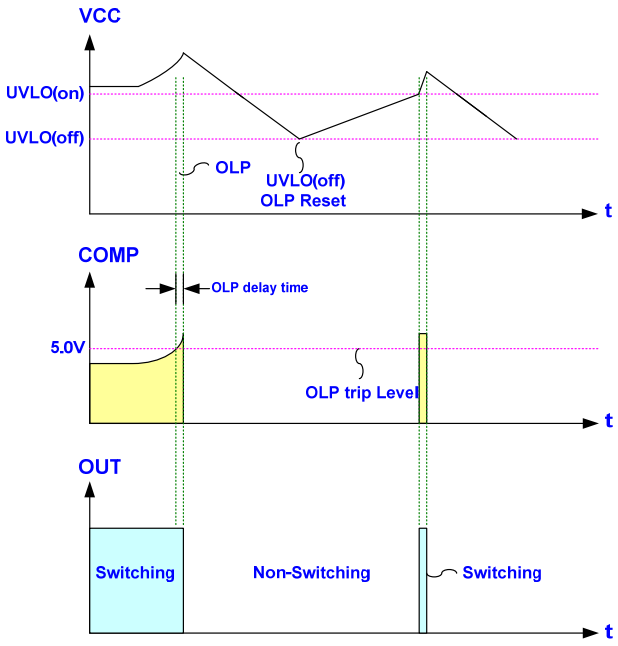
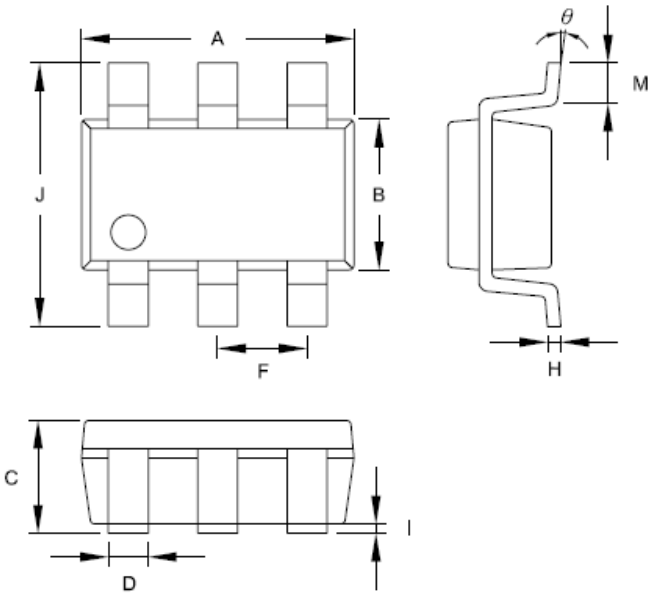


Fig. 19

Package Information

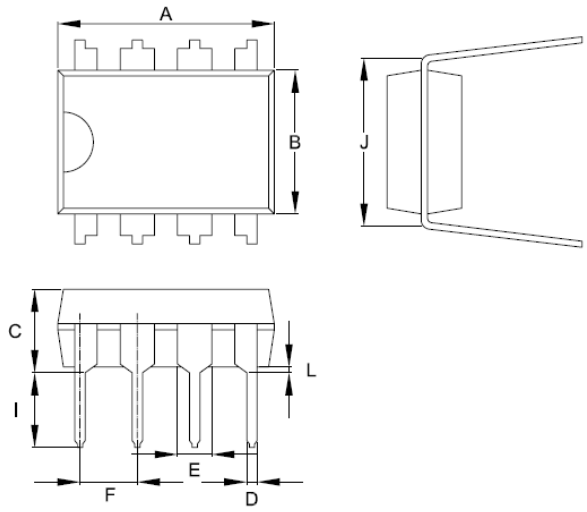
SOT-26



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	--------	1.450	--------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.290	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	12/17/2008	Original specification