



# STN4NF20L

N-channel 200 V, 1.1  $\Omega$ , 1 A SOT-223  
low gate charge STripFET™ II Power MOSFET

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STN4NF20L	200 V	< 1.5 $\Omega$	1 A

- 100% avalanche tested
- Low gate charge
- Exceptional dv/dt capability

## Application

Switching applications

## Description

This N-channel 200 V realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high efficiency isolated DC-DC converters.

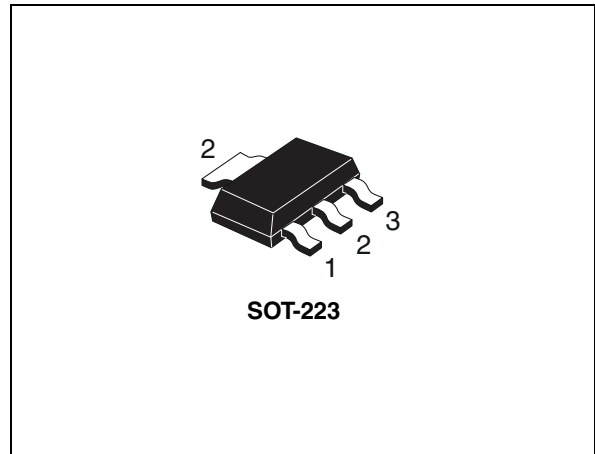


Figure 1. Internal schematic diagram

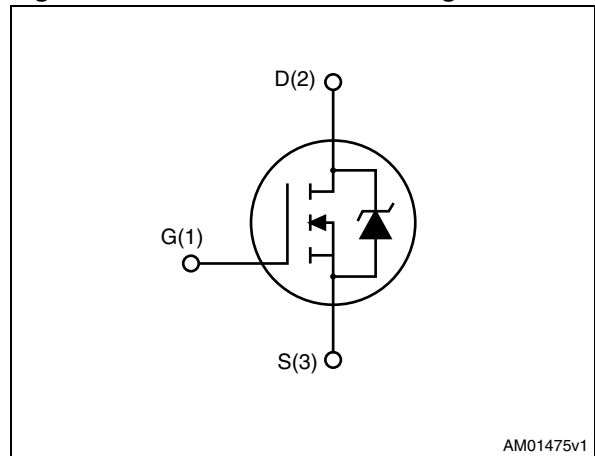


Table 1. Device summary

Order code	Marking	Package	Packaging
STN4NF20L	4NF20L	SOT-223	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current continuous $T_C = 25\text{ }^\circ\text{C}$	1	A
$I_D$	Drain current continuous $T_C = 100\text{ }^\circ\text{C}$	0.63	A
$I_{DM}^{(1)}$	Drain current pulsed	4	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	3.3	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	20	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. This value is rated according to  $R_{thj-amb} \leq 10\text{ sec}$ .
3.  $I_{sd} \leq 1\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction to ambient	38	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(2)}$		62.5	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu, ( $t < 10\text{ sec}$ ).
2. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu, ( $t > 10\text{ sec}$ ).

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive <sup>(1)</sup>	1	A
$E_{AS}$	Single pulse avalanche energy <sup>(2)</sup>	90	mJ

1. Pulse width limited by  $T_{JMAX}$ .
2. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	200			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> =125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> =0			± 100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1	2	3	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A V <sub>GS</sub> = 5 V, I <sub>D</sub> = 0.5 A		1.1 1.13	1.5 1.55	Ω Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	-	150	-	pF
C <sub>oss</sub>	Output capacitance			30		pF
C <sub>rss</sub>	Reverse transfer capacitance			4		pF
R <sub>g</sub>	Intrinsic gate resistance	f=1 MHz open drain	-	5.5	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 160 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13</a> )	-	0.9	-	nC
Q <sub>gs</sub>	Gate-source charge			2.6		nC
Q <sub>gd</sub>	Gate-drain charge			6.9		nC

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t <sub>d(v)</sub>	Voltage delay time	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 0.5 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 12</a> )	-	3.6	-	ns
t <sub>r</sub>	Voltage rise time			2		ns
t <sub>f</sub>	Current fall time			10.4		ns
t <sub>c(off)</sub>	Crossing time			15.4		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		1 4	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 1\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 14</a> )	-	51 90 3.5		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 1\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 14</a> )	-	56 105 3.7		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

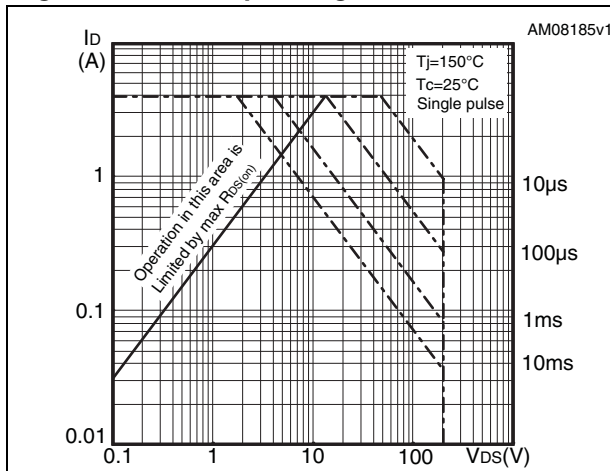


Figure 3. Thermal impedance

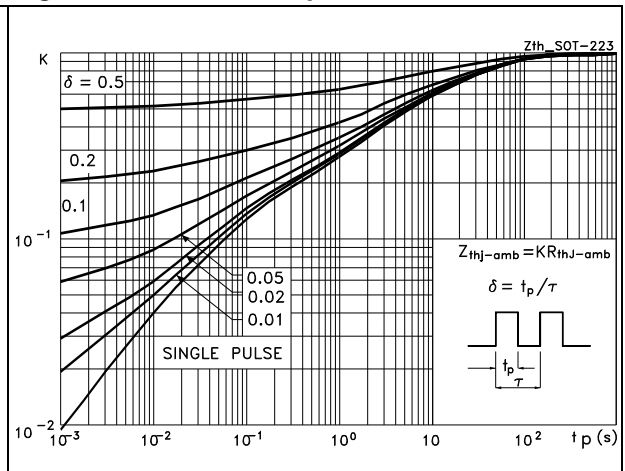


Figure 4. Output characteristics

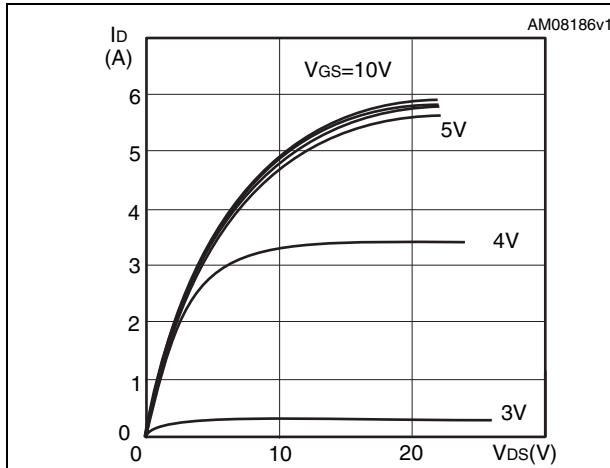


Figure 5. Transfer characteristics

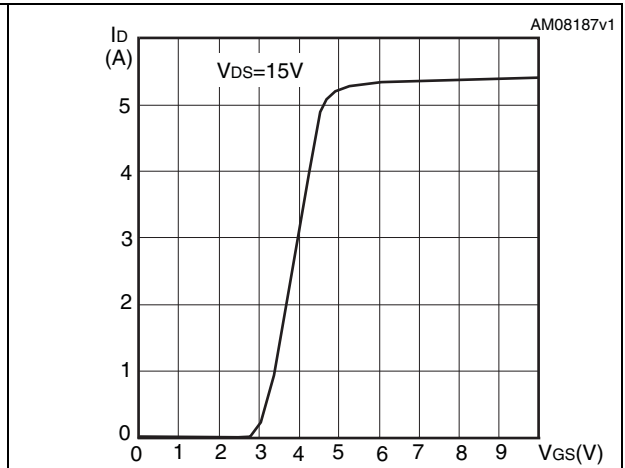


Figure 6. Normalized BV<sub>DSS</sub> vs temperature

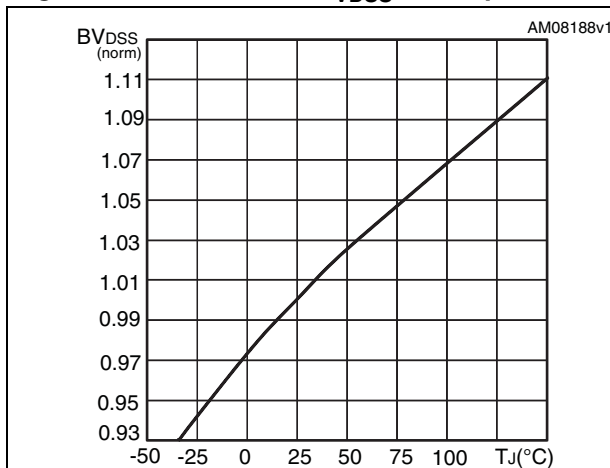


Figure 7. Static drain-source on resistance

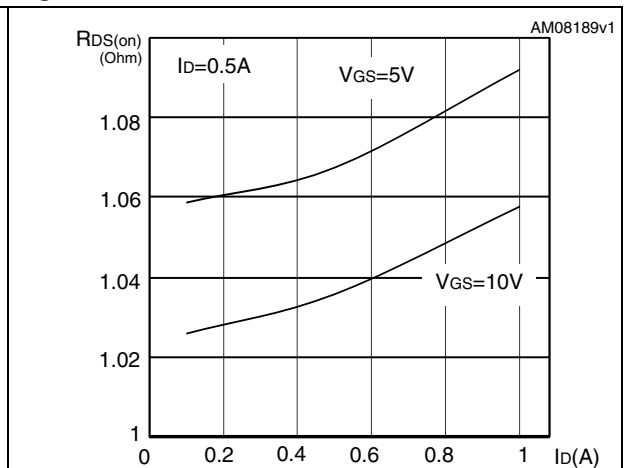


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

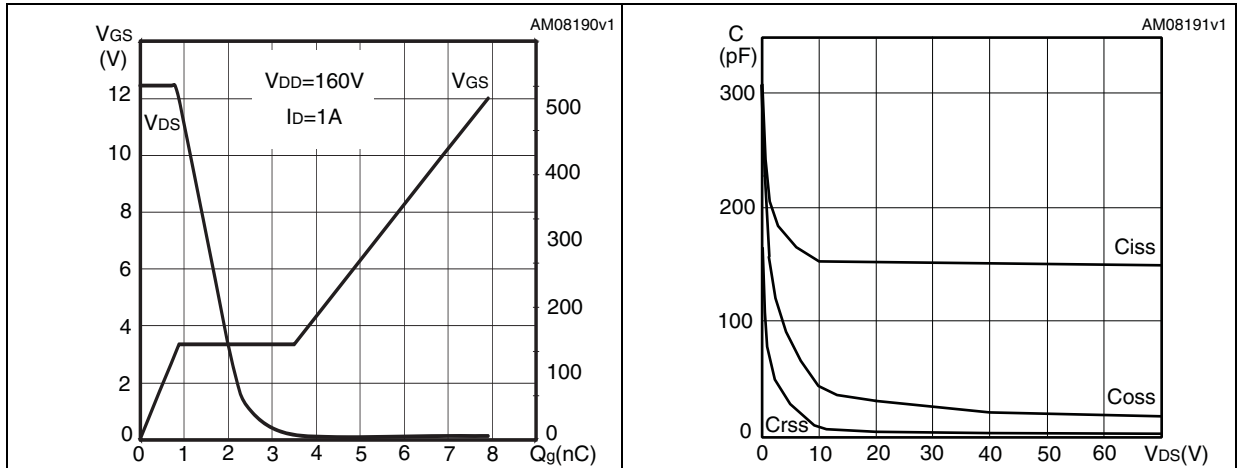
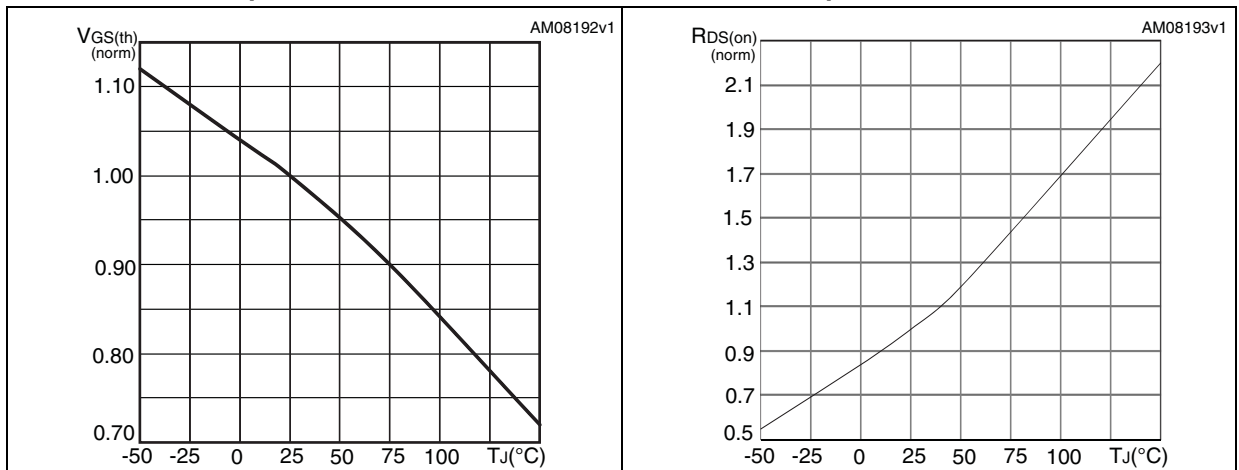
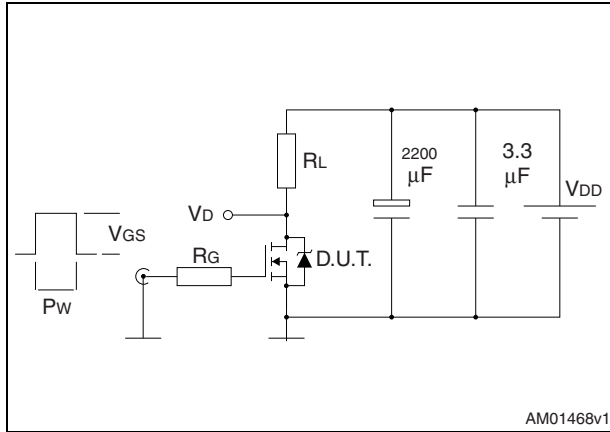


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature



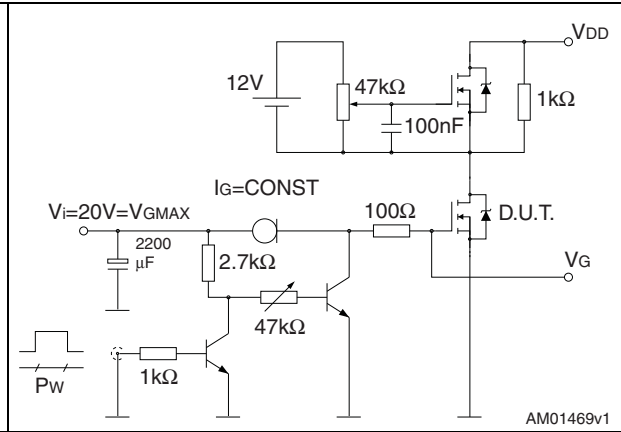
### 3 Test circuits

**Figure 12. Switching times test circuit for resistive load**



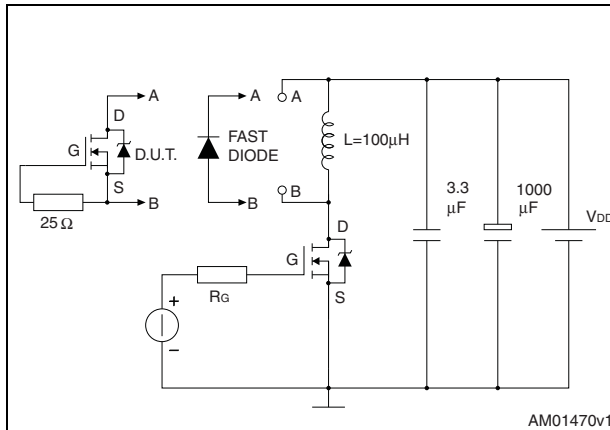
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**Figure 13. Gate charge test circuit**



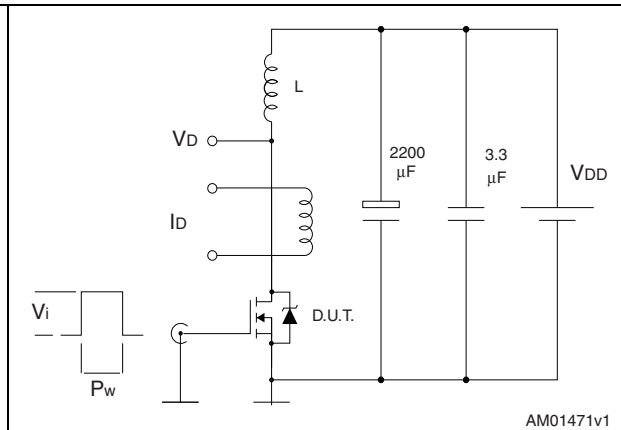
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**Figure 14. Test circuit for inductive load switching and diode recovery times**



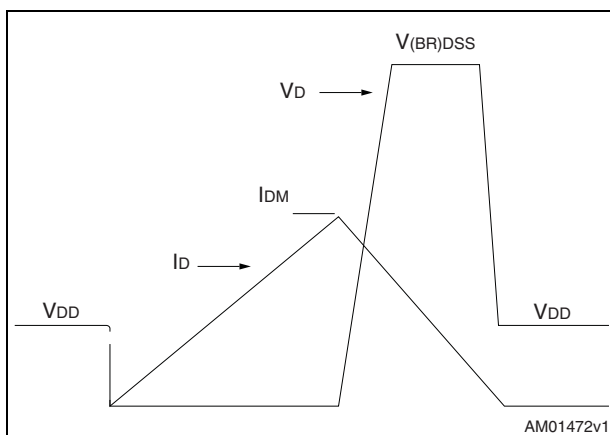
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**Figure 15. Unclamped inductive load test circuit**



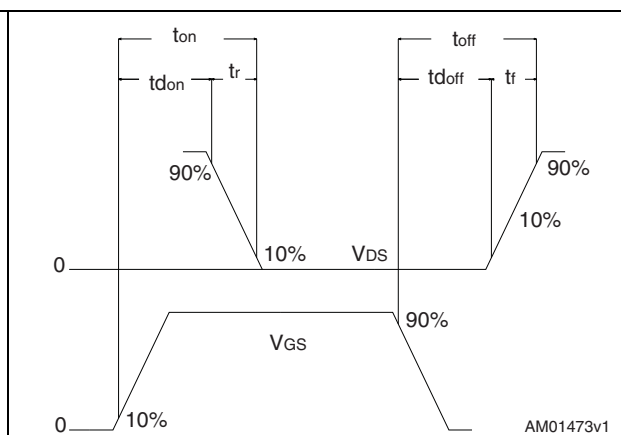
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**Figure 16. Unclamped inductive waveform**



AM01472v1

**Figure 17. Switching time waveform**



AM01473v1

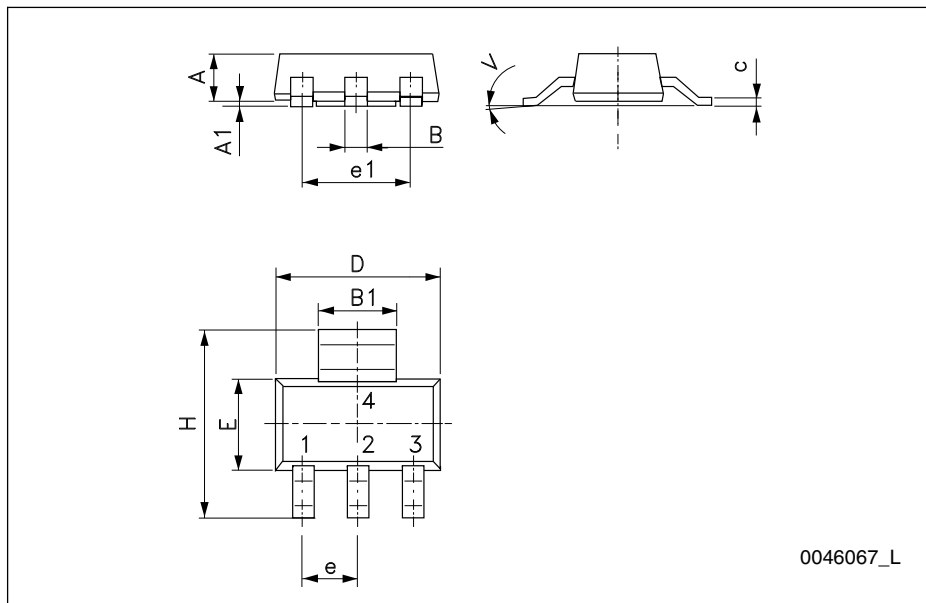


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**SOT-223 mechanical data**

DIM.	mm.		
	min.	typ	max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10°



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
29-Apr-2010	1	First release.
11-Oct-2010	2	Document status promoted from preliminary data to datasheet.

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