



STR-E1500 Family
Application Note

Sanken Electric Co., Ltd

<http://www.sanken-ele.co.jp>

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1. General Description

STR-E1500 family is a hybrid IC for a 2-converter power supply system, which has a pre-converter for power factor correction (PFC) to reduce harmonic waves, and DC-DC converter in the post stage. It incorporates a controller for the pre-converter (boost chopper type Critical Conduction Mode PFC) and the DC-DC converter, as well as a power MOSFET for the output stage of the DC-DC converter in a Sanken original SLA21-pin package (single in-line). Since the power MOSFET for the PFC is external, it is possible to optimize various PFC output power requirements. STR-E1500 is suitable for the down-sizing and the standardization of the power supply, because it requires a small number of external components and also offers easy circuit design. Also incorporated is a multi-mode control system for the DC/DC part, to select the optimized operation mode automatically by monitoring the load condition. It offers high efficiency and low noise power supply system.

2. Features

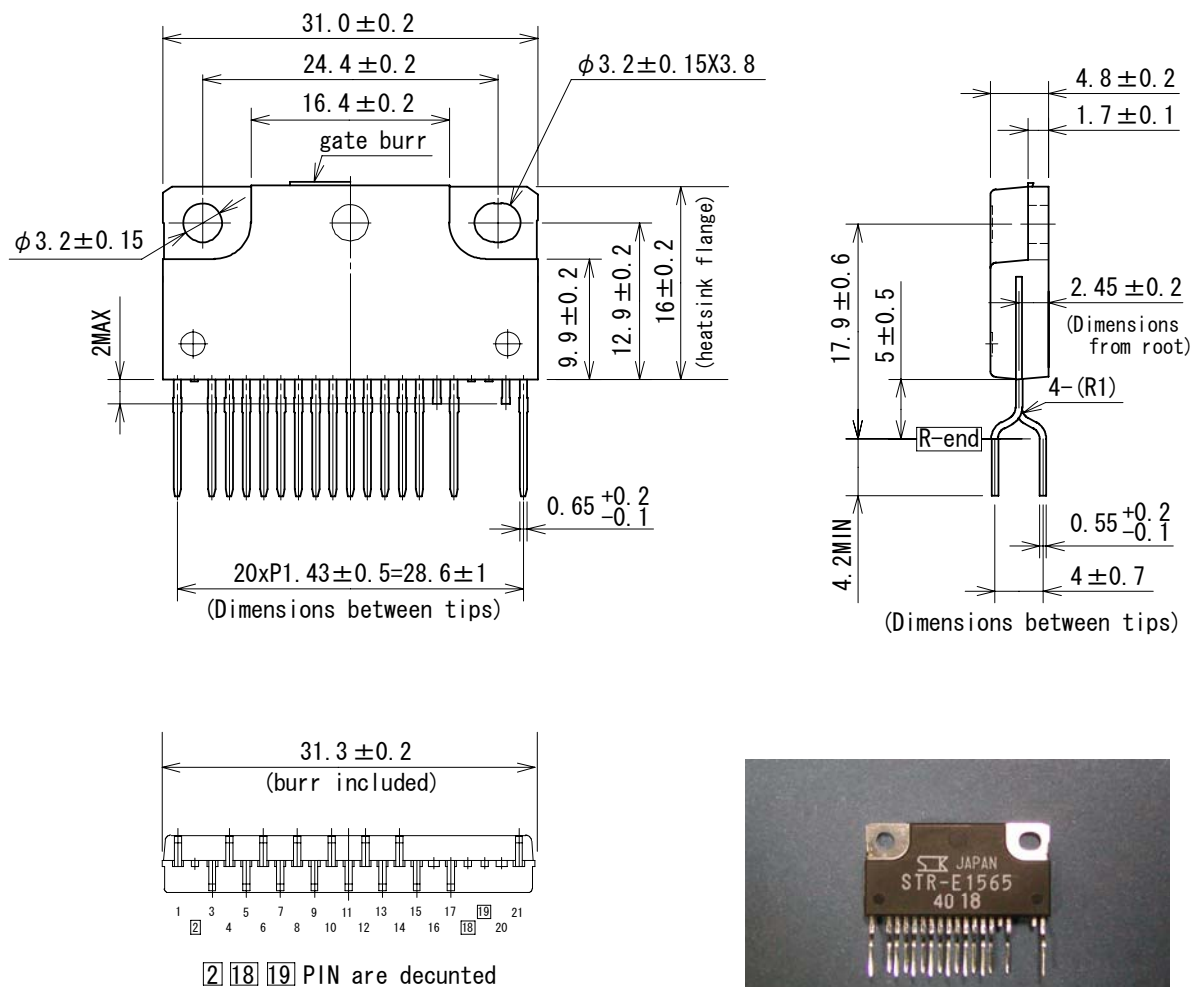
- 600V-high voltage BCD process is adapted for the 1 chip controller (PFC controller, DC/DC controller, Start-Up Circuit)
- Integrated PFC control block
 - 1) Critical Conduction Mode Control
 - 2) Built-in Multiplier with AC Input Voltage Compensation
 - 3) Built-in High Speed Over-Voltage Protection Circuit (Non-Latch Mode)
 - 4) Built-in Pulse by Pulse Over-Current Protection with Auto Input Voltage Compensation
- High Efficiency and Low EMI DC-DC Control Block
 - 1) DC/DC Control Block with Multi-Mode Control for High efficiency and Low Noise Multi-Mode Control
 - ① Quasi-Resonant at Middle to Heavy Load
 - ② PWM (100kHz typ.) with Frequency Jittering at Light to Middle Load
 - ③ Low Frequency Operation at No Load to Extremely Light Load
 - 2) Mixed Mode Control to realize stable operation throughout low to heavy load condition
- PFC ⇔ DC/DC Harmonized Operation
 - 1) Optimized start-up sequence by built-in Start-Up circuit
 - 2) Auto-Standby Function to stop PFC operation automatically in standby
(with adjustable Delay-Timer by an external capacitor)
 - 3) Auto-Standby with Input Voltage Compensation in standby
 - 4) Auto-Bias function to avoid Vcc dip in low frequency operation
- Sufficient Protection Function
 - 1) Pulse by Pulse Over Current Protection
 - 2) High Speed Over-Voltage Protection (at the PFC Block)
 - 3) Over-Load Protection
 - 4) Input Power Suppression System in intermittent operation
 - 5) Thermal Protection
 - 6) "External Latch Protection (ELP)" by imposing external signals on MultFP terminal

3. STR-E1500 Family Line-Up

Type	Internal MOSFET	PFC Part (total) Output Power (Included DC/DC Output Power)	DC/DC Part Output Power
STR-E1555	650V 0.7Ω	200W	200W
STR-E1565	800V 1.8Ω		80W

※Output power of the DC/DC Block is the reference value when it is operated in quasi-resonant in heavy load.

4. Package information



- Material of terminal : Cu
- Treatment of terminal : Ni plating + Solder dip (Pb free)
- Weight : Approx 5.6g

Fig 1. Package outlines (SLA 21-Pin Package)

5. Block Diagram

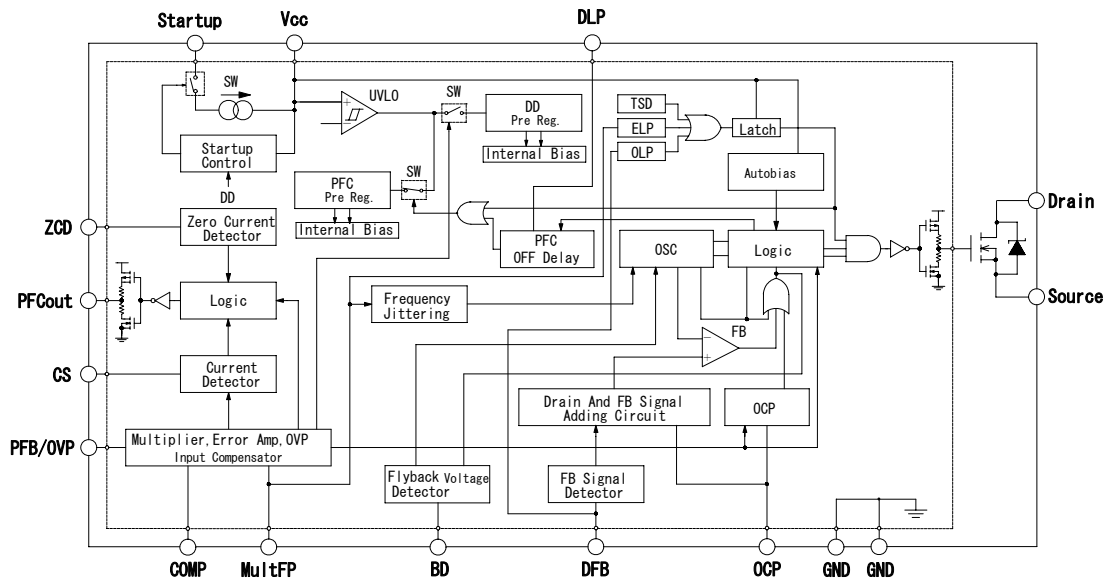


Fig 2. Block Diagram

6. Function of each terminals

Terminal No.	Symbol	Function
1	Startup	Input of startup current for DD and PFC part
2	NC	—
3	PFCout	Output of gate drive signal for MOSFET of PFC part
4	ZCD	Input of zero cross detection signal for PFC
5	CS	Input of drain current sense signal of PFC part
6	PFB/OVP	Input of control signal for constant voltage of PFC part, Input of over voltage protection signal of PFC part, Compensation of input for DD part
7	COMP	Output of Error Amp., phase compensation
8·9	GND	Ground of DD and PFC for control part
10	MultFP	Input of multiplier for PFC, Input of alteration signal for frequency of DD part, Input of alteration signal of output voltage for DD part, Compensation of AC input for PFC, Input of latch signal for DD and PFC part
11	DLP	PFC OFF delay time adjust
12	BD	Input of bottom on detection of DD part
13	OCP	Input of over current detection signal of DD part
14	DFB	Input of control signal for constant voltage of DD part
15	Vcc	Input of power supply of DD and PFC for control part
16	DDout	Output of gate drive signal for MOSFET of DD part (pin cut)
17	Source	MOSFET Source for DD part
18·19	NC	—
20·21	Drain	MOSFET Drain for DD part

7. Electrical Characteristics (Typical example : STR-E1565)

7.1 Absolute Maximum Ratings(Ta=25°C)

Parameter	Terminal	Symbol	Ratings	Unit	Note
Drain current	21-17	IDpeak	10	A	Single Pulse
Maximum switching current	21-17	IDMAX	5.2	A	Ta=-20~+125°C
Single pulse avalanche energy	21-17	EAS ^{※2}	150	mJ	Single Pulse
					VDD=30V, L=10mH ILpeak=5.4A
Input voltage for control part	15-9	Vcc	30	V	
MultFP terminal input current	10-9	ImultFp	10	mA	
Startup terminal voltage	1-9	Vstartup	-0.3~600	V	
CS terminal voltage	5-9	Vcs	-0.5~+10	V	
PFB/OVP terminal voltage	6-9	VPFB/OVP	-0.5~+7	V	
PFB/OVP terminal input current		IPFB/OVP	5	mA	
ZCD terminal input current	4-9	IZCD(I)	5	mA	
ZCD terminal output current		IZCD(O)	-5		
PFCout terminal source current	3-9	IoPFC(source)	300	mA	
PFCout terminal sink current	3-9	IoPFC(sink)	500	mA	
DFB terminal input voltage	14-9	VDFB	-0.5~+15	V	
DFB terminal output current		IDFB	2.2	mA	
OCP terminal input voltage	13-9	VOCP	-0.5~+7	V	
BD terminal input voltage	12-9	VBD	-0.5~+7	V	
Power dissipation for MOSFET	—	PD1 ^{※3}	8.9	W	With infinite heatsink
			1.8		Without heatsink
Power dissipation for control part(MIC)	—	PD2 ^{※4}	1.1	W	
Operating ambient temperature	—	Top	-20 ~ +125	°C	
Storage temperature	—	Tstg	-40 ~ +125	°C	
Channel temperature	—	Tch	+150	°C	

7.2 Electrical Characteristics for Control Part (Vcc=20V, Ta=25°C unless otherwise specified)

7.2.1 Total device part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Operation start voltage	15-9	Vcc(ON)	14.5	16.0	17.5	V
Operation stop voltage	15-9	Vcc(OFF)	9.0	9.7	10.5	V
Circuit current in operation	15-9	Icc(ON)	—	—	22	mA
Circuit current in non-operation	15-9	Icc(OFF)	—	—	350	μA
Latch circuit release voltage [※]	15-9	Vcc(La.off)	6.5	7.2	7.9	V
Input voltage in latch circuit operated [※]	15-9	Vcc(La.on)	8.4	9.6	11.5	V
Latch circuit sustaining current [※]	15-9	IH	—	500	1200	μA

Startup circuit	1-9	Istartup	3.4	5.4	7.7	mA
Bias current at startup terminal when startup circuit is not operated	1-9	Istartup(off)	—	20	80	μA
Latch threshold voltage of MultFP terminal	10-9	Vmult(La)	6.5	7.2	8.0	V
Restart power supply voltage	15-9	Vcc(RS)	7.0	7.8	8.6	V
Auto bias voltage	15-9	Vcc(BIAS)	10.1	11.0	11.8	V
Vcc(RS) – Vcc(La.off)	—	—	0.3	0.6	—	V
Vcc(OFF) – Vmult(La)	—	—	1.7	2.5	—	V
Thermal shutdown operating temperature	—	TSD	135	150	—	°C

* The latch circuit means a circuit operated an external signal over Latch threshold voltage of MultFP terminal.

7.2.2 PFC part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
PFB/OVP terminal threshold voltage(Hi)	6-9	VPFB(Hi)	3.905	4.000	4.056	V
PFB/OVP terminal input bias current	6-9	IPFB(B)	-5	-2	—	μA
COMP terminal source current	7-9	Icomp(SOU)	5	11	16	μA
COMP terminal sink current	7-9	Icomp(SIN)	-16	-11	-5	μA
COMP terminal Hi voltage	7-9	Vcomp(H)	5.8	6.4	—	V
COMP terminal Lo voltage	7-9	Vcomp(Hgl)	—	1.6	1.9	V
Over voltage detective input threshold voltage	6-9	VPFB(th)	4.14	4.27	4.40	V
MultFP terminal input bias current	10-9	Imult(B)	-10	-1	—	μA
Multiplier Gain	—	K	0.4	0.6	0.8	—
Zero Current Detective threshold voltage	4-9	VZCD(th)	1.4	1.6	1.8	V
Zero Current Detective hysteresis	4-9	VZCD(HIS)	150	190	260	mV
Zero Current Detective Hi clamp voltage	4-9	VZCD(HC)	6.0	6.6	7.0	V
Zero Current Detective Lo clamp voltage	4-9	VZCD(LC)	0.53	0.63	0.77	V
Restart delay time	—	tDLY	150	520	—	μs
CS terminal input bias current	5-9	ICS (B)	-8.0	-1	—	μA
CS terminal input offset voltage	5-9	VCS (IOS)	—	16.9	25.0	mV
Maximum current sense input threshold voltage(when compensation is not operated)	5-9	VCSMAX(th1)	1.18	1.37	1.52	V
Maximum current sense input threshold voltage(when compensation is operated)	5-9	VCSMAX(th2)	0.60	0.66	0.73	V
PFB/OVP terminal threshold voltage for DD Operation start signal	6-9	VPFB(DD ON)	2.9	3.2	3.5	V
PFCout terminal output voltage	3-9	VPFCOUT	10.2	11.8	—	V
Operation Voltage at UVLO	3-9	VPFCOUTUMLO	0.9	1.3	1.6	V

7.2.3 DD Part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Oscillation frequency (1)	16-9	fosc(1)	91	100	109	kHz
Oscillation frequency (2)	16-9	fosc(2)	76	83	90	kHz
Maximum ON time(1)	16-9	T _{ON} (MAX1)	7.4	8.8	9.7	μs
Maximum ON time(2)	16-9	T _{ON} (MAX2)	9.0	10.7	11.7	μs
Bottom detective terminal input threshold voltage	12-9	VBD(th)	0.67	0.76	0.84	V
Bottom detective terminal input bias current	12-9	IBD(B)	-6	-3	—	μA
OCP terminal detective voltage(1)	13-9	VOCP(1)	0.70	0.76	0.82	V
OCP terminal detective voltage(2)	13-9	VOCP(2)	0.54	0.60	0.66	V
OCP terminal input bias current	13-9	IOCP(B)	-12	-6	—	μA
Standby operation start on-time	16-9	TON(STB IN)	290	350	410	ns
Minimum on-time in Standby operation (1)	16-9	TON(STBMIN1)	460	580	700	ns
Minimum on-time in Standby operation (2)	16-9	TON(STBMIN2)	0.8	1.2	1.6	μs
Standby operation Release on-time(1)	16-9	TON(STBout1)	1.50	1.85	2.20	μs
Standby operation Release on-time(2)	16-9	TON(STBout2)	2.4	3.0	3.6	μs
Standby detective voltage at input compensation	6-9	VPFB(STB)	1.8	2.4	3.0	V
DLP terminal constant current L	11-9	IDLPL	—	1	4	μA
DLP terminal constant current H	11-9	IDLPH	20	40	60	μA
DLP terminal threshold voltage L for changed over	11-9	VDLPL	0.7	0.9	1.1	V
DLP terminal threshold voltage H for changed over	11-9	VDLPH	4.1	4.6	5.1	V
DFB terminal constant current	14-9	ICONST	15	21	27	μA
OLP terminal threshold voltage	14-9	VOLP	5.9	6.5	7.3	V
DD out terminal output voltage	16-9	VDDOUT	11.7	12.5	—	V

7.3 Electrical characteristics for MOSFET(Ta=25°C)

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Drain-to-Source breakdown voltage	21-17	VDSS	800	—	—	V
Drain leakage current	21-17	IDSS	—	—	300	μA
On-resistance	21-17	RDS(ON)	—	—	1.8	Ω
Switching time	21-17	tf	—	—	350	ns
Thermal resistance *	—	θ _{ch-F}	—	—	3.3	°C/W

* Between channel and internal frame

9. Explanation of PFC Block

Critical Conduction Mode PFC

In critical conduction Mode PFC, the PFC inductor current always operates at the boundary between the continuous and the discontinuous mode, and it is the operation mode that reduces switching loss as well as suppressing switching noise. In STR-E1500, it detects the zero current by monitoring the signal from the auxiliary winding of the PFC coil as the inductor current at ZCD Terminal (Pin 4). It controls that the inductor current always operates at the boundary. Also, it turns on the MOSFET at the bottom of the drain voltage (bottom-on switching) by detecting the falling edge of the auxiliary winding voltage at the ZCD terminal (refer to 11-1). Thus, STR-E1500 realizes the reduction of the switching loss and the low noise system by zero current switching (ZCS) and bottom-on switching.

Also, since STR-E1500 is incorporated with the constant voltage control circuit for the PFC block, it provides stable PFC output voltage in all load conditions by adding a resistor to the PFB/OVP terminal (refer to 11-2).

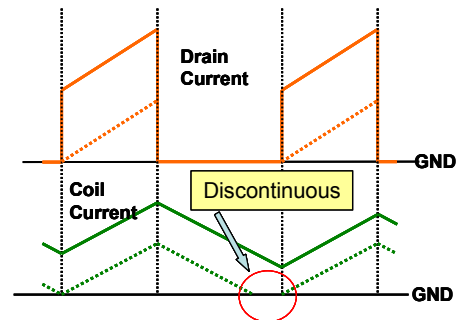


Fig4. Continuous and Discontinuous Mode

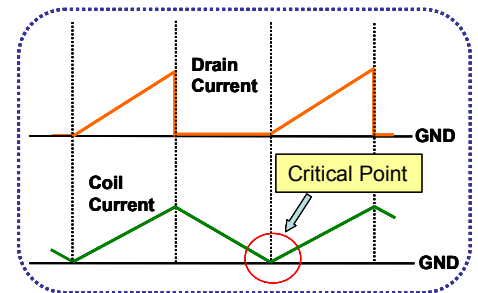


Fig5. Critical Conduction Mode

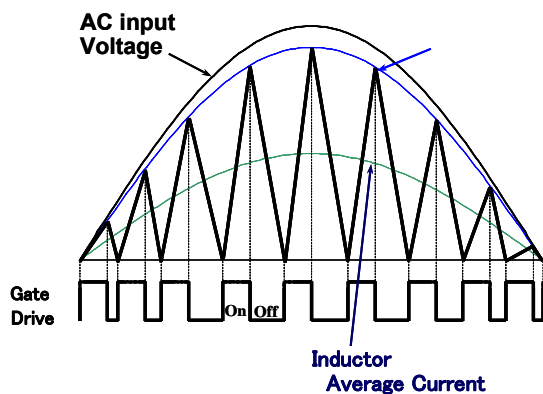


Fig 6. PFC Inductor Current

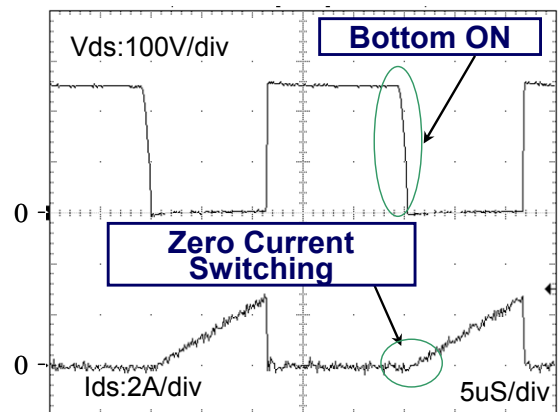


Fig7. Waveform of MOSFET (Vds, Id)

10. Explanation of DC/DC Block

Multi-mode Control

The DC/DC block of STR-E1500 family is a Fly-Back Type converter, and incorporates the multi-mode control that selects the optimized operation mode automatically by monitoring the load condition. The operation modes at each load condition are described in Fig 8 & Fig 9. In heavy load condition it operates as quasi-resonant to reduce switching noise and switching loss. In middle load condition it operates as PWM (100kHz) with frequency jittering. And, when the load gets lower (standby operation), it is switched to the low frequency operation mode automatically. In the low frequency operation, the PFC operation stops automatically in order to lower the power consumption in standby.

Since the delay time to stop the PFC operation (when the operation mode has moved to the low frequency operation) can be set by adding an external capacitor, it is possible to suppress the magnetizing noise from the PFC inductor by continuing operation of the PFC for a certain period, when the dynamic load change happens frequently between light and heavy load condition (refer to 11.6).

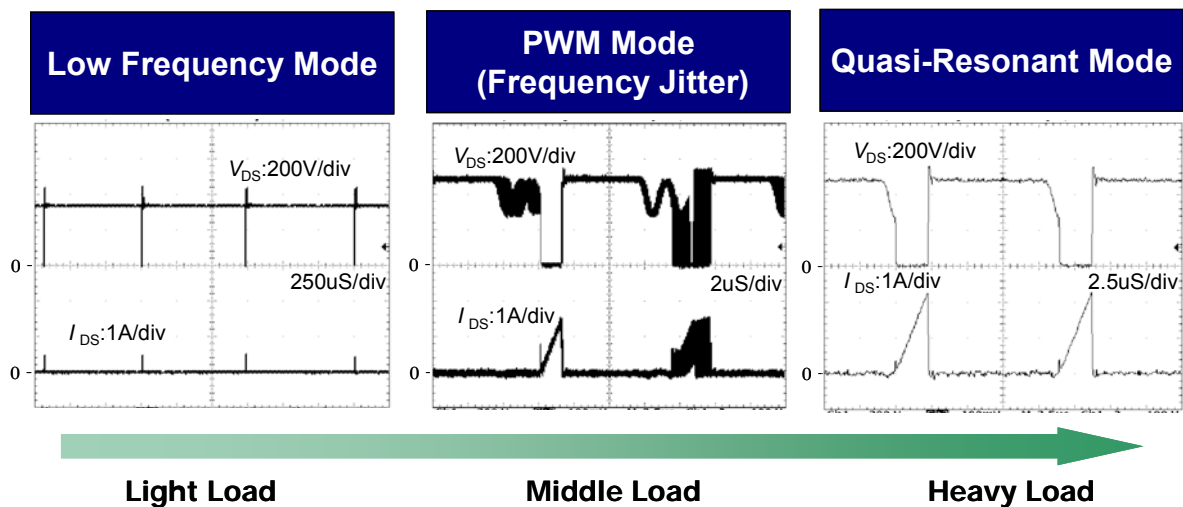


Fig8. Operation mode at each load condition

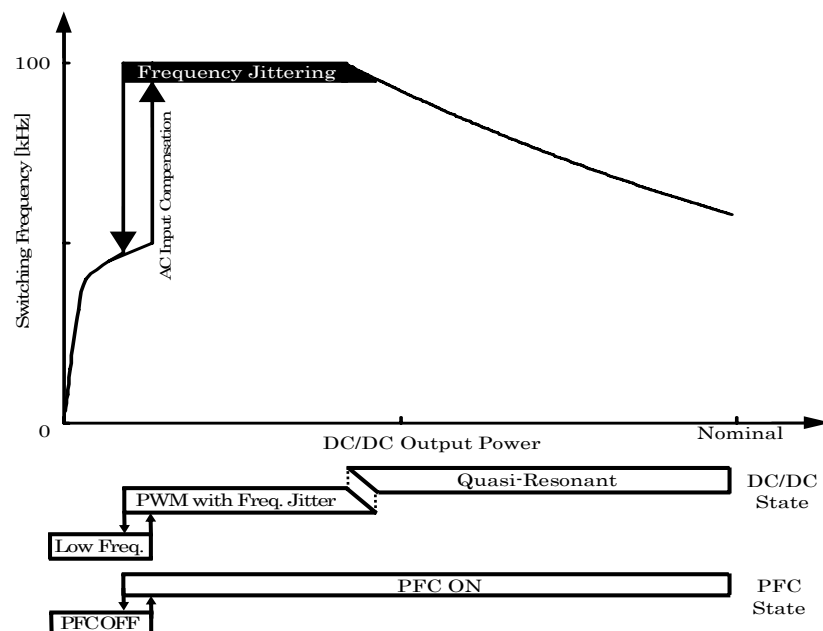


Fig 9. Multi-mode control operation mode transition

11. Description of Functions (PFC Block)

11.1 ZCD Terminal (Pin4)

The ZCD terminal is the input of the zero current detection. The switching of the PFC block starts the operation when the zero current signal is imposed on the terminal. When the peak inductor current reaches the threshold set by the output of the internal multiplier, the MOSFET turns off. The ZCD terminal detects the inductor current indirectly by monitoring that the auxiliary winding (Ns) voltage of the PFC inductor drops lower than the threshold voltage VZCD(th). After the turn-off of the MOSFET, when the auxiliary winding voltage exceeds VZCD(th)=1.6V(typ), the IC recognizes the start of the off-period. Then, when it drops to VZCD(th)-VZCD(HIS), the next cycle will be initiated. In order to avoid malfunction, a 0.19V of hysteresis VZCS(HIS) is added to VZCD.

The ZCD terminal is protected by 2 clamping methods. VZCD(HC)=6.6V(TYP) is to avoid over-voltage, and VZCD(LC)=0.63V(TYP) is to prevent negative voltage being imposed on the terminal (refer to Fig 11). Since current limitation is required to this terminal, it is necessary to select a resistor so that The ZCD terminal input current is

$$I_{ZCD} < 5\text{mA} \quad R > (PFCV_o \times (N_s/N_p)) / 5\text{mA}$$

11.2 PFB/OVP Terminal (Pin 6)

The PFB/OVP terminal is for the constant voltage control for the PFC output and for the zero voltage detection. The threshold of the constant voltage control is VPF(BH)=4V(TYP). The threshold of high speed OVP is VPF(BH)=4.27V(TYP).

Since the PFC block is a boost chopper type, if the inductance value of the boost inductor is low, there is the possibility that the PFC output voltage increases. However, in STR-E1500, it is prevented by the negative feedback constant voltage control and over-voltage protection. Also, this terminal is used for the start-up sequence. After AC input, the PFC output voltage starts rising, and when the PFB/OVP terminal voltage reaches VPF(BDON)=3.2V (TYP), the DC/DC block starts operation. Since this terminal voltage is decided by a resistive divider, if the PFC output voltage is 380V, the DC/DC block starts operation when the PFC output voltage reaches about 302V. As for the external resistors, it is recommended to use high stability resistors such as metal oxide film resistors, because high resistance value resistors are required. Also, since this terminal is used as the input of the error amplifier for the PFC constant voltage control, a capacitor is required for filtering, to avoid unstable operation caused by noise. Usually, a 100pF capacitor is sufficient. If problems such as abnormal oscillation happen, the operation will be stabilized by increasing the capacitor value. Since it affects the transient response of the PFC, it is recommended to adjust it by the smallest possible capacitance.

11.3 MultFP Terminal (Pin 10)

The MultFP terminal is the input of the built-in multiplier. Full-bridge rectified AC voltage is divided by a resistive voltage divider, which is inputted to this terminal as the signal. This voltage waveform is the very important signal to convert the input current to the sinusoidal wave. The

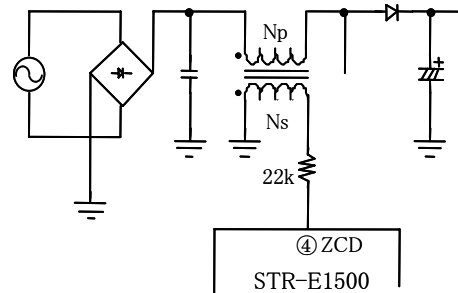


Fig10. Auxiliary winding for zero current detection

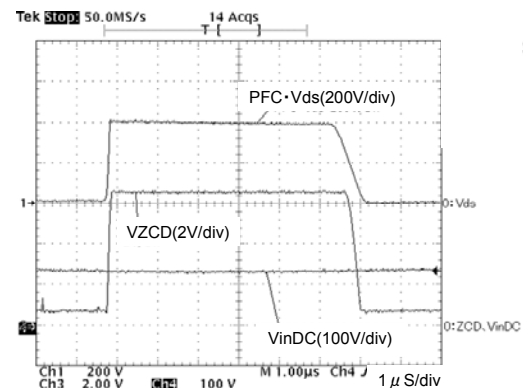


Fig 11. Waveform of ZCD terminal voltage
<VinAC=100V / Po(DC-DC)=50W>

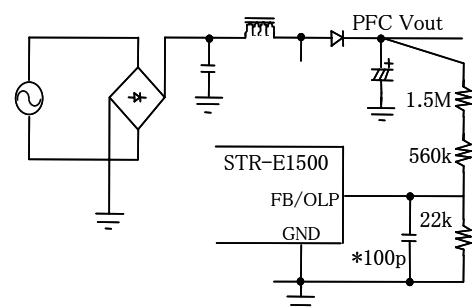


Fig 12. PFC output voltage detection circuit

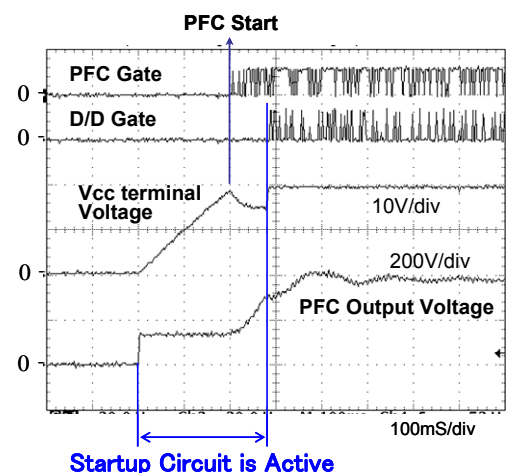


Fig 13. Start-up Sequence

characteristics of the multiplier are described in Fig 16.

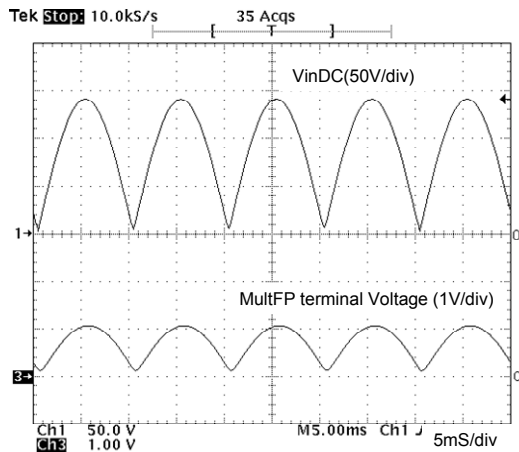


Fig.14 Waveform of MultFP Terminal
<VinAC=100V / Po(DC-DC)=50W>

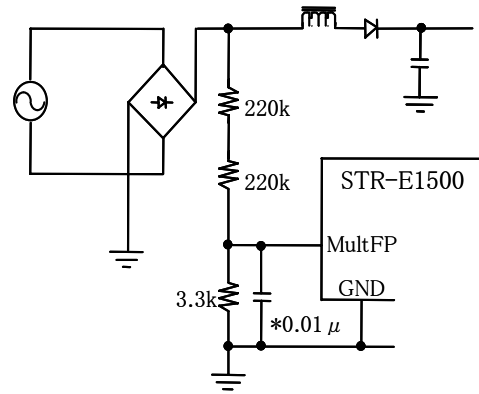


Fig15. Representative circuit near to MultFP Terminal

Please refer to Fig 15 for the value of the external components. It is recommended to use high stability resistors such as metal oxide film resistors, because the resistance is high. It is recommended to use a low capacitance filtering capacitor between the MultFP (Pin 10) and the ground, because the sinusoidal wave signal is smoothed, and it results in unstable operation. But, in the event of the malfunction caused by noise, a certain level of capacitance is required. So, it has to be examined with the actual power supply.

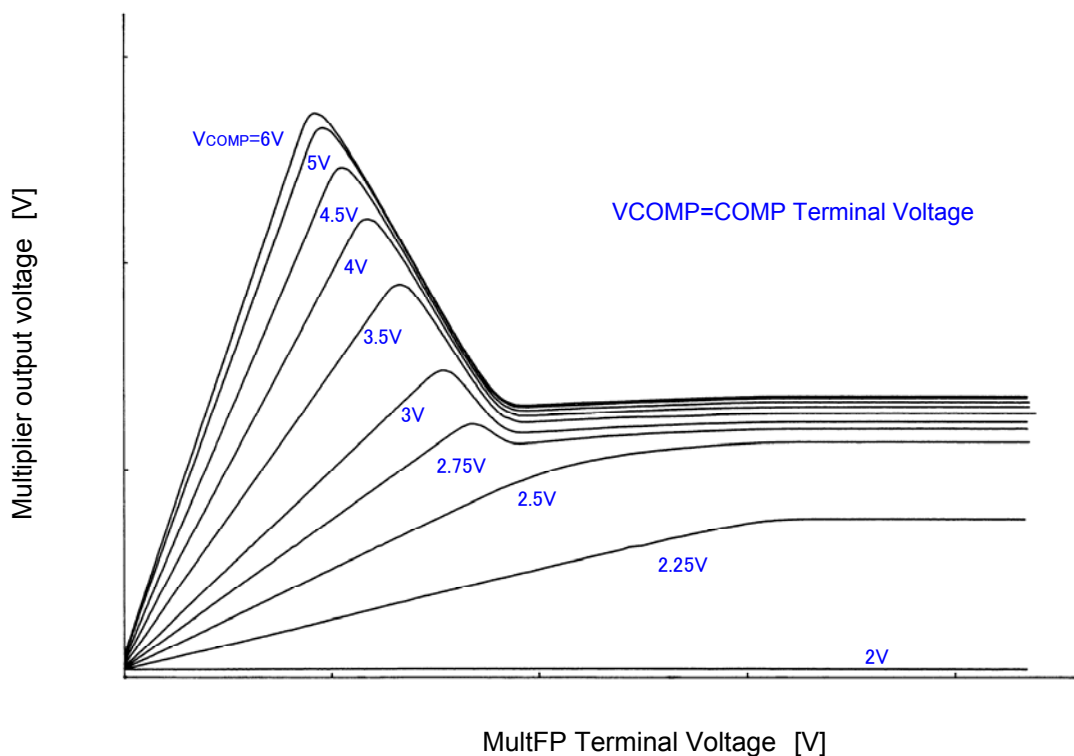


Fig 16 Characteristics of Multiplier

((Latch shut- down by using MultFP Terminal))

This terminal can be used as the latch trigger input. It is possible to shut-down the PFC and the DC/DC blocks in latch mode (ELP) by imposing more than $V_{mult}(La)=7.2V(TYP)$ on this terminal from the external circuit.

Input current to MultFP terminal is 10mA (Max)

11.4 Comp Terminal (Pin 7)

The Comp terminal is for the phase compensation of the PFC block. As for the external capacitor, the operation is stabilized by adding a higher value capacitor. But, it is required to adjust the capacitor value by looking at the phase-shift (forward/ backwards). The capacitor value in Fig 17 is an example. So, it is required to decide the value by confirming the following does not happen;

- 1) Abnormal oscillation
- 2) Start-up failure
- 3) Malfunction in dynamic load change
- 4) Phase distortion for current and voltage

This terminal outputs the voltage corresponding to the threshold voltage of the CS terminal

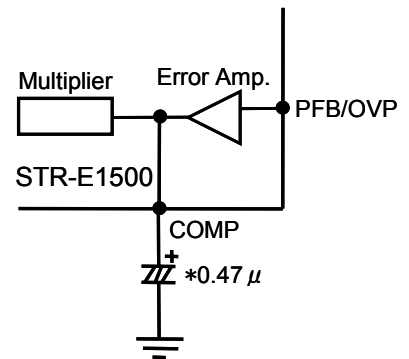


Fig 17 Comp Terminal

11.5 PFCout Terminal (Pin 3)

The PFCout terminal is the output of the gate drive for the external MOSFET for the PFC block. It is possible to drive the MOSFET directly, because it has the output of 300mA for source and 500mA for sink. But, when it is difficult to drive the MOSFET directly depending on the characteristics of the MOSFET such as Ciss, it is effective to add an external buffer circuit.

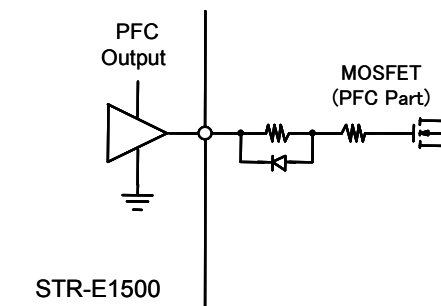


Fig 18 Direct Drive
(Ciss of MOSFET: Small)

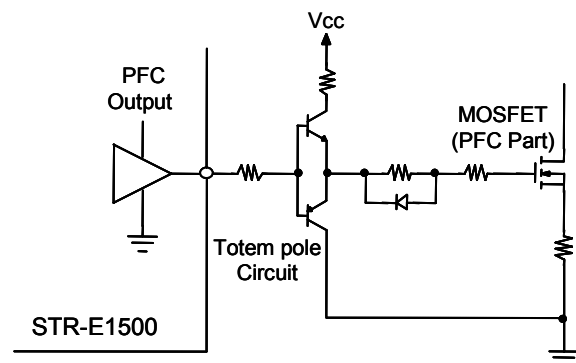


Fig 19 External Buffer Circuit
(Ciss of MOSFET: Large)

Fig 20 is the operation waveform to drive a FTO-3P size MOSFET (Ciss=2000pF~3000pF) by adding an external buffer circuit. This is the reference operation waveform where the switching speed is reduced (both turn-on and turn-off of the MOSFET) by suppressing source and sinks current to reduce switching noise.

Because switching speed and switching loss is in the relationship of trade-off, it is recommended to adjust the value of the gate resistor with the actual board.

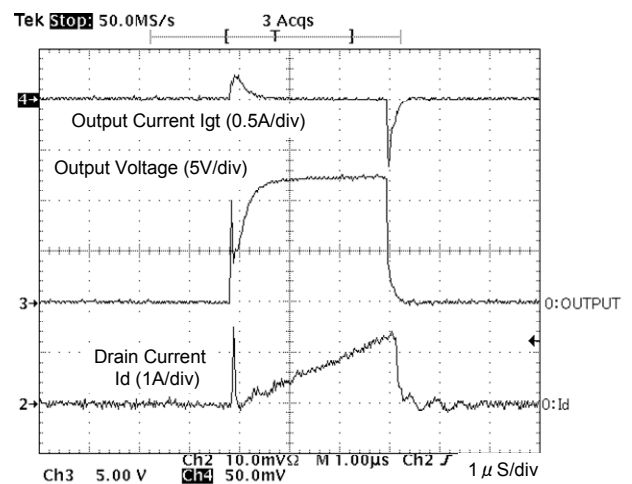


Fig 20 Operation waveform with buffer circuit
<VinAC=100V / Po(DC-DC)=50W>

11.6 DLP Terminal (Pin 11)

If the load condition frequently fluctuates between minimum to maximum dynamically in normal operation, there is the possibility that noise from the PFC coil can be heard, because the PFC block repeats start-up & stop-operation each time when the DC/DC block goes into low frequency operation. In STR-E1500, it is possible to avoid the problem by adding a capacitor to the DLP terminal. STR-E1500 detects the timing when the DC/DC goes into low frequency operation, when the load at the DC/DC block gets lower. Then, it charges up the capacitor connected to the DLP terminal by the internal constant current circuit, and when the DLP terminal voltage reaches $V_{DLPH}=4.6V(TYP)$, the DC/DC block goes into the low frequency operation and at the same time stops the PFC operation.

When the load gets lower, and while the capacitor connected to the DLP terminal is charged at $IDLPH=40\mu A(TYP)$, the PFC operation continues. At the same time, the DC/DC block is banned to shift to the low frequency operation mode, and keeps the PWM operation.

For the period which is proportional to the capacitance, it is possible to avoid the audible noise from the PFC coil. Once the load condition moves away from the light load condition, the capacitor at the DLP terminal is discharged by the internal discharging circuit before the DLP terminal voltage reaches $V_{DLPH}=4.6V(TYP)$.

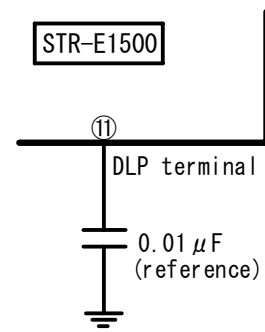


Fig 21 External circuit at DLP Terminal

11.7 CS Terminal: Pin 5

The CS terminal is to detect the drain current to flow to the MOSFET at the PFC block. By inserting a high surge energy capable resistor such as a metal plate resistor to the source of the MOSFET, the drain current is converted to voltage, and then the signal is inputted to this terminal. In order to avoid unstable operation due to the surge current from the MOSFET at turn-on, a CR filter circuit is inserted (the value shown in Fig 22 is reference). If the time constant of the CR filter circuit is too long, there is the possibility that the peak current becomes too large due to the delay of the current detection. Therefore, it is recommended to select the smallest possible value for the filter circuit by confirming with the actual board that there is no malfunction.

In STR-E1500, in order to prevent the excess power of the PFC block at AC200V input range, the threshold voltage of the CS terminal (V_{CSMAX}) is automatically switched depending on the input voltage (AC100V: $1.4V$ □ AC200V: $0.65V$). So, the value of the sense resistor R_s is decided at AC100V input range $V_{CSMAX}(th1)$.

Example:

at $I_d \text{ peak}=8A$, $R_s = 1.4/8A = 0.175\Omega \Rightarrow 0.15\Omega$

When the envelope curve of the drain current at the PFC block is observed, it is a sine wave like input current. If the waveform of the current is not a sine wave at the peak of the instantaneous value of the input voltage because of the current limitation, $I_d \text{ peak}$ may reach the threshold voltage of the CS terminal (V_{CSMAX}). Therefore, it is necessary to be re-confirmed by reducing the value of the sense resistor R_s . Fig 23 shows the operational waveform in normal operation when I_d does not reach the threshold voltage.

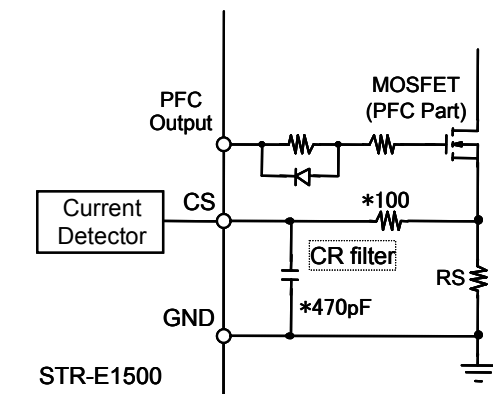


Fig 22 Circuit at CS terminal (Reference)

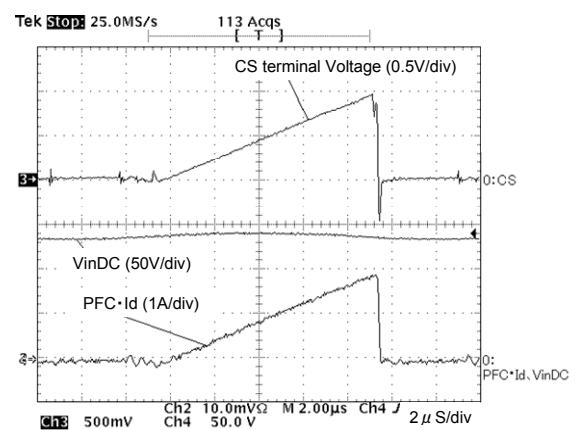


Fig 23 Operational waveform of CS Terminal

12. Functions of Each Terminal (DC/DC Block)

12.1 StartUp Terminal (Pin 1), and Vcc Terminal (Pin 15)

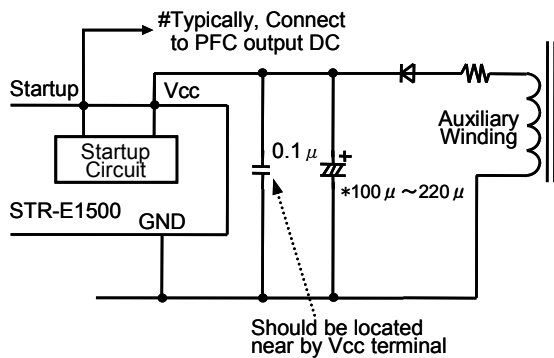
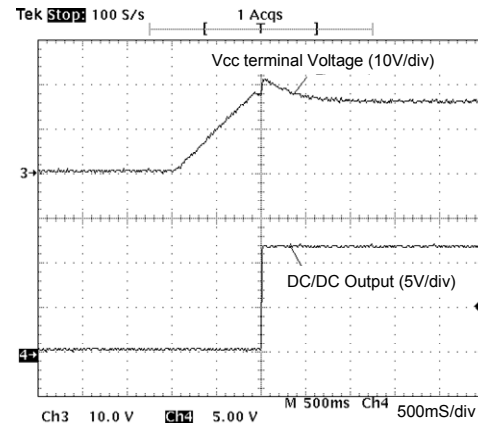


Fig 24 IC Buck-up Circuit

Fig 25 Waveform of Vcc Terminal at start-up
<VinAC=100V>

After AC input, the electrolytic capacitor connected to the Vcc terminal is charged by the internal start-up circuit at the constant current of 5.6mA, and the IC starts operation at $V_{cc} > 16.2V(TYP)$. The StartUp terminal is connected to the Vcc terminal through the start-up circuit, and the start-up circuit stops operation automatically when it reaches $V_{PFB}(DD ON)=3.2V$. Then, the IC continues operation by the power supply from the auxiliary winding of the transformer. Please refer to the following to select the auxiliary winding output voltage and the capacitance for the capacitor connected to the Vcc terminal.

- # Output voltage of the auxiliary winding: 23V (Target), to be calculated from the number of turns of the secondary winding & Vout
- # Vcc capacitor value is required $100\mu F \sim 220\mu F$ to cope with rapid load changes including no-load or light load condition.

12.2 DFB Terminal (Pin 14)

The DFB terminal is for the constant voltage feedback of the DC/DC block. It is negative feedback by the photo coupler. The resistor and the capacitor shown in Fig 26 are for phase compensation. If a high gain amplifier such as a shunt regulator is used, the operation is stabilized by inserting a resistor and a capacitor as shown in Fig 26. Usually, the operation is stabilized with the value shown in Fig 24. But, it is recommended to set the value by confirming the following;

- Regulation when the load changes dynamically
- Abnormal oscillation in high or low temperature

The DFB terminal voltages fluctuates depending on the load condition. If the photo coupler is short-circuited, the output voltage from this terminal rises to around 12V.

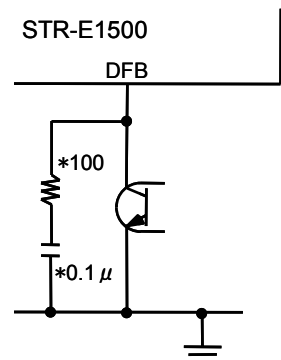


Fig 26 Circuit near to DFB Terminal

12.3 OCP Terminal (Pin 13), and Source Terminal (Pin 17)

The OCP terminal is for the detection of over current. The threshold voltage of the OCP terminal is $VOCP(1)=0.76V/VOCP(2)=0.6V$, and $VOCP(1)$ is applicable for STR-E1555V with the PFC output voltage boost ratio control function. As for STR-E1555 or STR-E1565 without the PFC output voltage boost ratio control function, the value of the sense resistor R_s is to be calculated from $R_s = VOCP / I_{dp}$ by applying $VOCP(2)$.

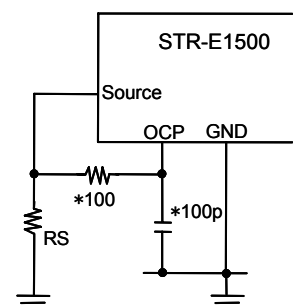


Fig 27 Circuit around OCP Terminal

12.4 BD Terminal (Pin 12)

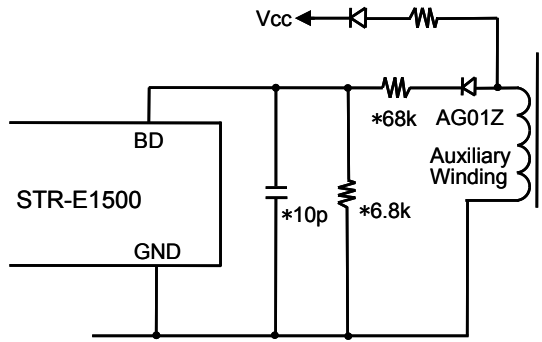
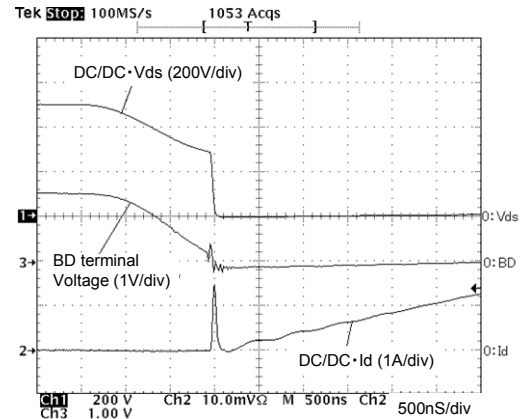


Fig 28 Bottom detection circuit

Fig 29 Operation waveform of BD Terminal
<VinAC=100V / Po(DC-DC)=50W>

The BD terminal is to detect the quasi resonant signal. Quasi resonant is to match the timing of the MOSFET turn-on to the bottom point of voltage resonant waveform after a transformer releases the energy or to match 1/2 cycle of the resonant-frequency.

The quasi resonant operation is started by inputting the quasi resonant signal to the BD terminal. The fly-back voltage generated in the auxiliary winding is transformed to the quasi resonant signal by a resistive voltage divider. The timing of the bottom point of the voltage resonant is adjusted by the capacitor. The circuit shown in Fig 28 is the bottom detection circuit to adjust the bottom point. It is required to adjust the capacitor value so that the MOSFET turns on at the bottom of the VDS, by observing the operation waveform of the actual board with the actual load. The threshold voltage of the BD terminal is $V_{BD(th)}=0.76V(TYP)$. If the signal inputted to this terminal does not exceed the threshold voltage, the operation mode does not shift to the quasi resonant operation and continues the 100kHz PWM operation.

Generally, the pulse height of the quasi resonant signal is set around twice that of the threshold voltage. As for the delay time, since there is the relationship of $\tau = \pi \sqrt{L_p \times C_r}$ between L_p of the transformer at the DC/DC block and the element that is corresponding to the capacitance of the voltage resonant capacitor, it is required to secure about twice as large a signal amplitude against the threshold voltage. At the same time, the timing of the bottom-on that is corresponding to τ , is to be adjusted by the capacitor value at the quasi resonant circuit.

13. Example of Application Circuit

13.1 OVP and Thermal shutdown by using Latch Function of MultFP Terminal

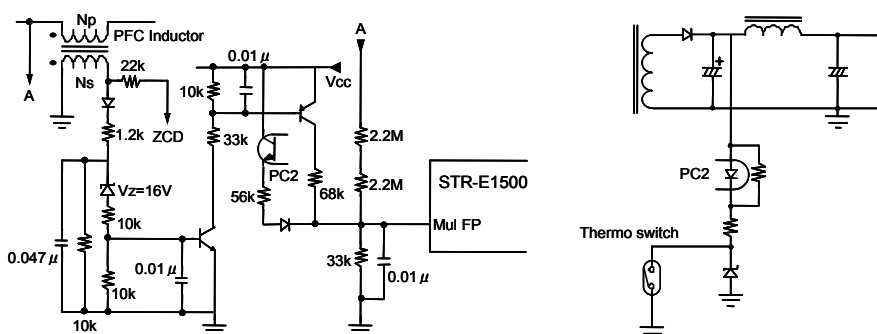


Fig.30 OVP and Thermal shutdown circuit by using Latch Function of MultFP Terminal

The circuit shown in Fig 30 is the reference circuit of Over Voltage Protection at the PFC and direct detection OVP/ Thermal Protection at the secondary side for abnormal operation. It is possible to detect the PFC output voltage directly. But, since it is high voltage, it detects the PFC inductor auxiliary winding voltage that is rectified and smoothed, and it triggers the MultFP terminal by using the Vcc terminal voltage. As for the secondary detection OVP, similarly it triggers the MultFP terminal by using the Vcc terminal voltage through the photo coupler.

13.2 Cancellation of OLP Function

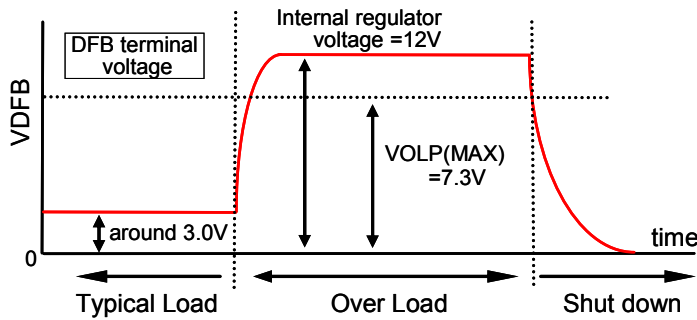


Fig.31 DFB terminal voltage at Overload condition

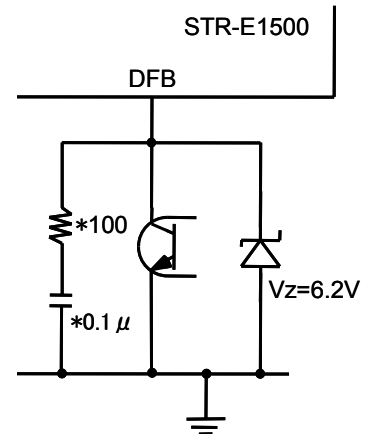


Fig 32 OLP Operation Cancellation

Fig 31 shows the state of the DFB terminal in over-load. When the secondary side is in over-load and the feedback through the photo coupler is suspended, the DFB terminal voltage starts rising by the pull-up of the internal regulator.

When the DFB terminal voltage reaches VOLP=6.5V(TYP), the internal latch circuit starts operation. Then, both the PFC and the DC/DC blocks are shut-down. It is possible to cancel the OLP function by adopting the circuit shown in Fig 32, in case a problem is caused by the OLP operation such as at the cut-off of AC input.

13.3 ON/OFF of DC/DC Output

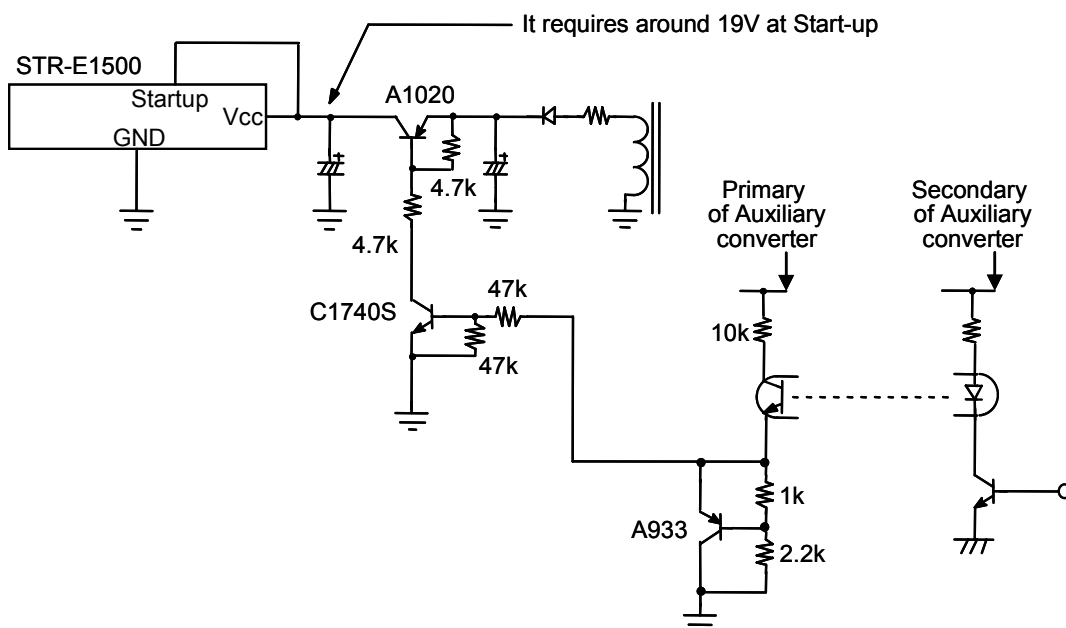


Fig 33 DC/DC Output ON/OFF

In STR-E1500, it is possible to switch off the output of the DC/DC block by grounding the DFB terminal. But, since the power supply from the auxiliary winding is suspended, the start-up circuit continues operation, and it results in the power loss. Even if the auxiliary power supply is used in standby, the power loss is inevitable. However, it is possible to minimize the power loss by adopting the circuit shown in Fig 33. In Fig 33, the auxiliary winding is added to the transformer of the auxiliary power supply to supply the power to the Vcc of STR-E1500. Since STR-E1500 is operated from start-up to normal operation by the supply of the auxiliary winding voltage, it is switched ON/OFF by switching the ON/OFF at the output of the auxiliary winding. The number of turns of the auxiliary winding is to be decided by considering that the Vcc terminal voltage is required around 19V at start-up. Also, in this case, the Startup terminal is short-circuited to the Vcc terminal, so as not to connect to the high voltage side.

13.4 Smoothing Capacitor and Commutating Diode at PFC Block

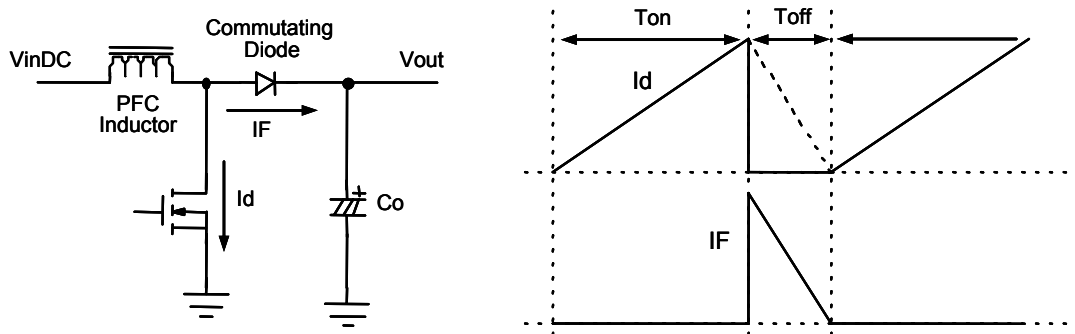


Fig 34 Outline of Boost Chopper Type PFC Operation

(1) Smoothing Capacitor at PFC Block

① Select By Output Sustaining Time

It is possible to calculate the capacitance of the smoothing capacitor by using the following formula decided by the output sustaining time.

$$Co = \frac{2 \times Po \times \eta \times th}{Vout^2 - Vop(Low)^2}$$

Po: Output Power of DC/DC Block (W) **η**: Efficiency at PFC Block **th**: Output sustaining time at DC/DC Block (S)

Vout: Output Voltage at PFC Block (V) **Vop(Low)**: Minimum input voltage of DC/DC Block (V)

Co: Capacitance of Smoothing Capacitor (F) **Irl**: Ripple Current at PFC Block (A) **Iout(DC)**: DC output current at PFC (A)

② Select By Ripple Current

$$Irl = \frac{Iout(DC)}{\sqrt{2}} \quad *** \quad Iout(DC) = \frac{Po \times \eta}{Vout}$$

Switching current of the primary side of the DC/DC block flows to Co, and shows the ripple current as Ir2.

$$Ir(total) = \sqrt{Irl^2 + Ir2^2} \quad (Ir2 \text{ is the effective value of } Id \text{ at DC/DC Block})$$

It is required to select the capacitor value using the severest condition of the two options.

(2) Commutating Diode

Since STR-E1500 is a hybrid IC for Critical Conduction Mode PFC, on the contrary to Continuous Mode PFC

it does not require considering the recovery loss at the delay of PFC turn-on. It is to be selected by considering VRM, IFSM, and I_o (output current of the DC/DC block). Since output voltage is 260V to 400V usually, the withstanding voltage of the diode is 600V. It is to be selected by considering the commutating current at normal operation and the inrush current when AC is imposed. Finally, it is to be selected by looking at the temperature rise.

14. Design of PFC Inductor and Transformer

14.1 PFC Inductor

STR-E1500 is for Critical Conduction Mode PFC. Inductance (L_p) at boundary current mode is calculated with the following formula.

$$L_p = \frac{T \times 10^{-6} \times \left(\frac{V_o}{\sqrt{2}} - V_{inAC(min)} \right) \times \eta \times V_{inAC(min)}^2}{V_o \times P_o \times \sqrt{2}} \quad I L_p = I_{dp} = \frac{2\sqrt{2} \times P_o}{\eta \times V_{inAC(min)}}$$

T: Time of 1 cycle (S) **V_o**: Output voltage of PFC Block (V) **P_o**: Output power of PFC block (W)
η: Efficiency at PFC block (usually around 0.9) **V_{inAC(min)}**: Minimum AC input voltage (V)
I L_p: Peak inductor current (A) **I_{dp}**: Peak drain current (A) **L_p**: Inductance of PFC Inductor (H)

T (time of 1 cycle) can be set up to T=20μS~15μS in a practical use. At the time switching frequency is around 50kHz~70kHz. It is possible to reduce the inductance (L_p) and down-size the inductor by increasing the switching frequency. But, the switching loss at turn-off is increased according to higher frequency operation.

The number of turns of the main PFC inductor winding (N_p) is calculated from the following formula.

$$N_p = \sqrt{\frac{L_p \times 10^{-6}}{AL - Value \times 10^{-9}}}$$

AL-value is to be selected so that the magnetic saturation is not caused, by considering NI(AT) value that is calculated from N_p and $I L_p$. The calculated NI value ($=I L_p \times N_p$) has to be within the NI vs AL-value characteristics curve. As for the selection of a ferrite core to satisfy the relationship of AL-value vs NI, it is to be considered in the design margin such as temperature rise or other tolerances. It is recommended to set the calculated NI value ($=I L_p \times N_p$) so that it has around a 30% margin against the NI limit linear curve in the core data.

Table1. Example of calculation

Input Value		Calculated Value	
V _o	400 V	I _{dp}	4.44 A
V _{inAC(min)}	85 V	I _{in(Ave)}	2.22 A
η	0.9	L _p	379.04 μH
T	20 μS	N _p	44 T
P _o	120 W	NI	193.15 AT
AL-Value	200 nH/N ²		

The table in the left is an example of calculation following each formula.
PFC output voltage: 400V PFC output power: 120W

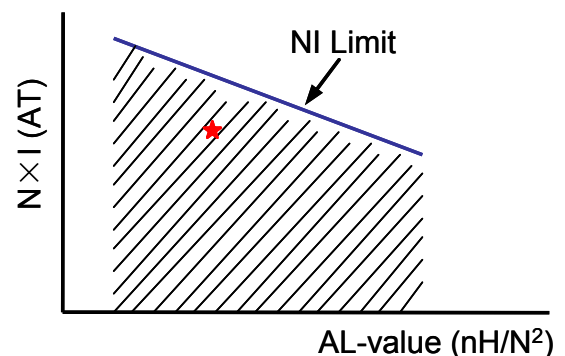


Fig 35 NI vs AL-Value characteristics (reference figure)

* Core for PFC Inductor

In discontinuous mode or critical conduction mode, the inductor current is operated between zero ⇔ peak. Toroidal coils are made from dust-core or amorphous alloy. Even though a centre gap is added, the current waveform may be distorted, because its DC superimposed inductance characteristics are not flat. Also, STR-E1500 requires the zero current detection winding (ZCD winding), so it is recommended to use a transformer type ferrite core such as an EER type, which DC superimposed inductance characteristics are flat. As for the ZCD winding, usually it is to set the voltage amplitude at around 30V, that happens in off-time of the MOSFET of the PFC block. If the setting in the above table is taken as an example, the number of turns of the ZCD winding (Ns) is set as 4turn (Ns=4T), because Ns is calculated as Ns=44×(30V/400V)=3.3 from Np=44.

* Winding Material

Since the PFC inductor is in the primary circuit, it is sufficient with the basic insulation + additional insulation. But, it is recommended to use litz wire for the main winding due to the skin effect. As for the ZCD winding, there is no problem with the conventional UEW wire.

14.2 Transformer at DC/DC Block

When the bottom detection function of the BD terminal is used, it is operated at the quasi resonant at heavy load condition. It is required to compensate duty by the period that the turn-on is delayed. Lp is calculated from the following formula (ON duty is described as D).

$$Lp = \frac{(VIN \cdot D)^2}{\left(\sqrt{\frac{2 \cdot Po \cdot fo}{\eta}} + VIN \cdot \pi \cdot fo \cdot D \cdot \sqrt{Cr} \right)^2}$$

fo: Minimum oscillation frequency (Hz) **D**: ON Duty at minimum AC input voltage

η: efficiency of transformer =0.9 (when output voltage is high), 0.75~0.85 (When output voltage is low)

π: Cycle Ratio **Cr**: Capacitance of Voltage Resonant Capacitor (F) **Po**: Maximum output power (W)

VIN: DC voltage after AC input is rectified and smoothed, at min AC input voltage (V) **Lp**: Primary Inductance (H)
(Smoothing capacitor terminal voltage)

Also, each parameter such as peak drain current is calculated from the following formula.

$$D = \frac{VD}{Vin + VD}$$

$$T = \pi \sqrt{Lp \times Cr}$$

$$D' = (1 - fo \times T)D$$

$$Iin = \frac{Po}{\eta 2 \times VinDC(\min)}$$

$$Idp = \frac{2 \times Iin}{D'}$$

$$Np = \sqrt{\frac{Lp}{AL - Value}}$$

$$Ns = \frac{Np(Vo + VF)}{VD}$$

f_o: Min. Oscillation Freq.(Hz) **η₂**: efficiency of converter (around 0.85) **L_p**: Primary inductance (H)
I_{in}: Average input current (A) **I_{dp}**: Peak switching current (A) **V_{inDC(min)}**: Min. DC input voltage (V)
D: Set Duty **D'**: Compensated Duty **V_D**: Input DC voltage at duty 50% (V) **V_o**: Output DC voltage (V)
P_o: Max. output power (W) **N_p**: Number of turns at primary winding **N_s**: Number of turns at 2ndary winding
V_F: V_f of secondary diode (V) **C_r**: Capacitance of resonant Cap.(F) **T**: Delay Time (S)

Table2. Example of the calculation (V_o=12V, P_o=120W)

Input Item	Input Value	Unit	Calculated Item	Calculated Value	Unit
V _{inAC} (Min)	85	V	L _p	238.3	μH
V _{inDC} (Min)	108.2	V	T	1.05	μS
F _{sw} (Min)	50	kHz	D'	0.54	
C _r	470	pF	I _{in}	1.30	A
η ₂	0.85		I _{dp}	4.83	A
V _D	141	V	N _p	34.52	T
D	0.57		N _s	3.11	T
P _o	120	W	ND	5.96	T
AL-Value	200	nH/N ²	N _s /N _p	0.09	
V _o	12	V			
V _F	0.7	V			

Note

If the transformer designed for the PWM operation is used in the quasi resonant operation, it is required to make sure that there is no problem with the actual board in N*I (I_d peak at DC/DC times number of turns of N_p winding) vs AL value relationship, because the switching frequency is reduced in the quasi resonant operation.

* Winding Methods (Structure)

The winding method (structure) is the same as for the conventional RCC type. Since the previously mentioned transformer calculation example is for low output voltage, it is required to suppress the V_{ds} surge voltage at turn-off of the MOSFET by reviewing the coupling between the primary and the secondary winding. Therefore, it is recommended to adopt the sandwich structure of the primary and secondary winding. Also, it is required to have sufficient creepage distance between the primary and the secondary winding depending on the required safety regulation. It is also recommended to operate at higher input voltage (which is boosted up by PFC) than $V_{inAC} \times \sqrt{2}$.

15. Other Instructions for Use

15.1 Pattern Layout of Printed Circuit Board and EMI Filter

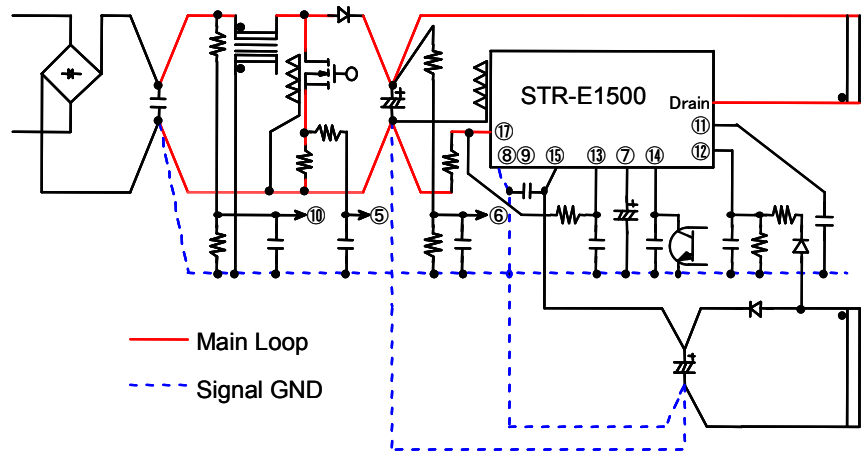


Fig 36 High current loop

(1) Pattern Layout

Since high current flows in the main loop highlighted in red in Fig 36, it is required to draw the pattern as thick and short as possible. In order to avoid the interference between the PFC and the DC/DC block, it is required not to have the same impedance for the pattern that switching current flows directly. The blue dotted lines are for the ground of the signal side, and high current such as switching current, does not flow. But, it is also required for the signal ground lines to have the lowest possible impedance in order to avoid the interference between the PFC and the DC/DC block.

The terminals of the control part of the IC are high impedance input. This is to minimize the power consumption at the control part. Therefore, it is required to make sure that these terminals do not pick up noises. As for the capacitors around the IC, it is also required to connect the ground side of the capacitors as close as possible to the terminal 8 & 9.

Please note that if these patterns cross just underneath the PFC inductor or the transformer, it may cause problems due to the leakage flux.

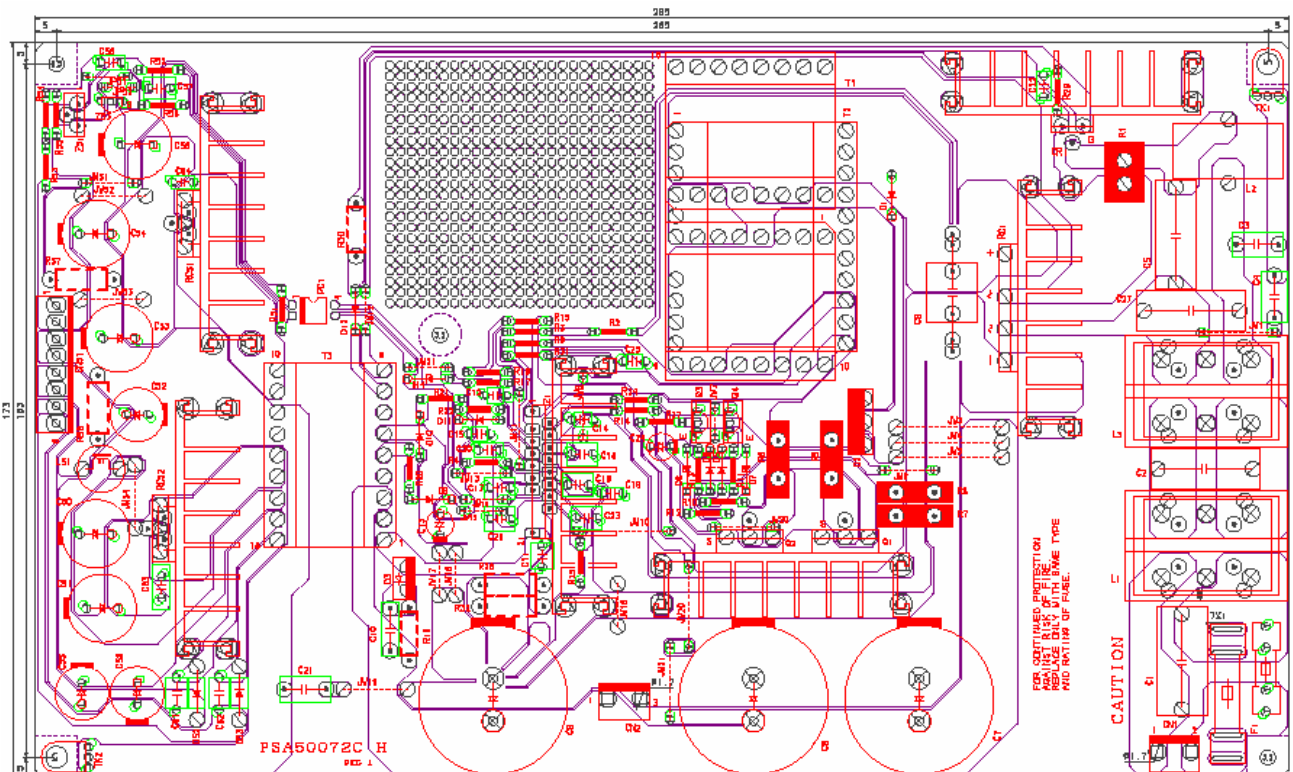


Fig 37 Pattern Layout (Reference)

Fig 37 is the reference printed circuit board pattern that is designed for our operation confirmation purpose. It is a single-sided board, and the mount of surface mount components has not been considered. As for the output power, it is around 200W output for the PFC and 100W for the DC/DC block (it is possible to supply the balance 100W PFC output power with other outputs). A ferrite core with an air gap is used for the PFC inductor and the transformer for the DC/DC block.

Usually, a heat sink is to be attached to the MOSFET of the PFC and STR-E1500. If the heat sink is floated, it is likely to be affected by noises due to the stray capacitance between the drain of the internal MOSFET and the heat sink. And, there is the possibility that the heat sink radiates noise as an aerial. Therefore, it is recommended to connect the either side of the heat sink to the stable electric potential such as the negative side of the electrolytic capacitor (output of the PFC, input of the DC/DC block).

(2) EMI Noise

① Low-Pass Filter

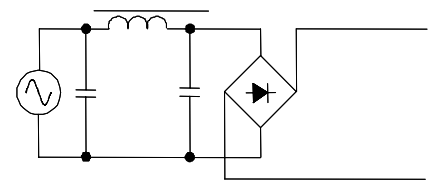
STR-E1500 is for Critical Conduction Mode PFC. For Critical Conduction Mode or Discontinuous Mode PFC, it is recommended to adopt the low-pass filter, (which consists of a normal mode coil, a film capacitor, etc) to eliminate high frequency elements from the waveform of the AC input current.

The PFC inductor current fluctuates zero to peak in Critical Conduction Mode PFC, and the average current of the AC input is about half of the peak current.

In Critical Conduction Mode PFC, in principal there is the possibility that the superimposed high frequency elements remain on the current waveform of the power frequency. In that case, there is the possibility that the conduction noise is worse in the high frequency band that is the underlying wave of the oscillation frequency at the PFC block. So, it is recommended to eliminate the high frequency elements by composing the normal mode filter in addition to the common mode filter.

Fig 39 & Fig 40 are the operational waveforms when the low-pass filter is added. It is the LC filter that consists of a 100 μ H normal mode coil and a 0.47 μ F capacitor. If the actual waveforms are not like the ones in Fig 39 & Fig 40 and the noises are observed on the current waveform at the high instantaneous value of AC input voltage, the high frequency elements are not eliminated completely. Therefore, it is required to review the noise filter.

(1) AC Side



(2) DC Side

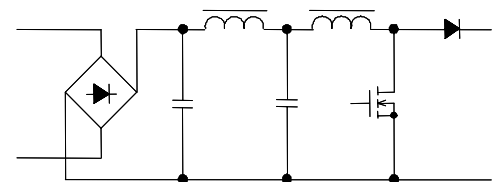


Fig 38 Low-Pass Filter

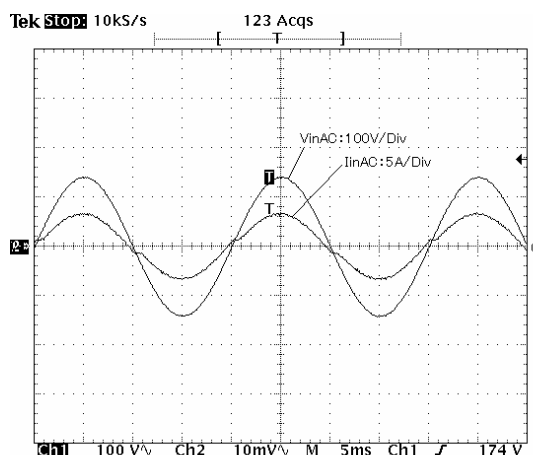


Fig 39 Operational Waveform with a low-pass filter (at AC100V input)

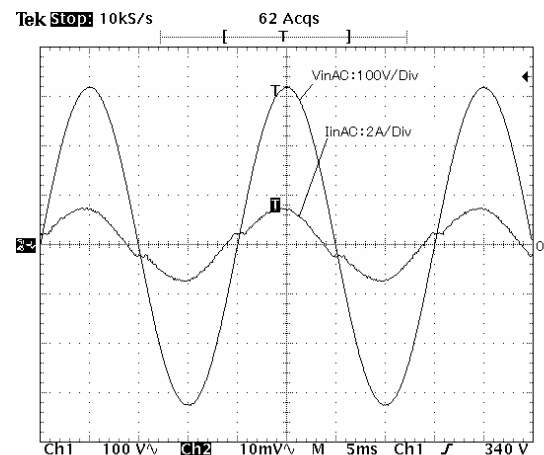


Fig 40 Operational Waveform with a low-pass filter (at AC200V input)

15.2 Releasing Latch Shut-Down and Restart

It is required to re-start the power supply with the following procedure when it is shut-down by triggering the MultFP terminal.

① Latch Trigger



② Shut-down
(Oscillation suspended)



③ AC input cut-off



④ Vcc drops



⑤ $V_{cc} < \text{Latch circuit release voltage} \rightarrow \text{Possible to re-start}$

※ V_{cc} drops \rightarrow UVLO(9.7V TYP) \rightarrow Restart Power Supply Voltage (7.8VTYP) \rightarrow

\rightarrow Latch Circuit Release Voltage (7.2V TYP) \rightarrow Possible to re-start

Due to the sequence of the start-up circuit, it is not possible to restart the power supply at the moment when the V_{cc} terminal voltage drops lower than the Operation Stop Voltage $V_{cc}(\text{OFF})$. The start-up circuit is initialized to operate, when the restart voltage of the start-up circuit is under $V_{cc}(\text{OFF})$ and the V_{cc} terminal voltage drops to the Restart Power Supply Voltage $V_{cc}(\text{RS})$. It is possible to restart when it is $V_{cc} < \text{Latch Circuit Release Voltage}$.

* In case the time period to re-start the power supply is too long against the power supply requirement, it is required to add a solution to discharge the back-up capacitor of the V_{cc} terminal compellingly.

15.3 Input power suppression system

If it is operated in the intermittent mode in the over load condition at the DC/DC block, the switching IC is over-heated due to the short burst cycle, when the AC input voltage is high. But, in STR-E1500, since the hysteresis ΔV is set between the Operation Stop Voltage $V_{cc}(\text{OFF})$ and the Restart Power Supply Voltage $V_{cc}(\text{RS})$, the burst cycle is extended compellingly. Thus, the temperature-rise of the STR-E1500 is minimized in the intermittent operation.

Please note that if the discharging period of the back-up capacitor of the V_{cc} terminal (C15) is slow in the time period of the above mentioned ΔV , there is the possibility that the IC does not respond/ re-start depending on the timing of ON/OFF, when the AC ON/OFF test is conducted. But, after a certain period, the V_{cc} terminal voltage drops to the Restart Power Supply Voltage $V_{cc}(\text{RS})$. Then, it is possible to re-start the power supply.

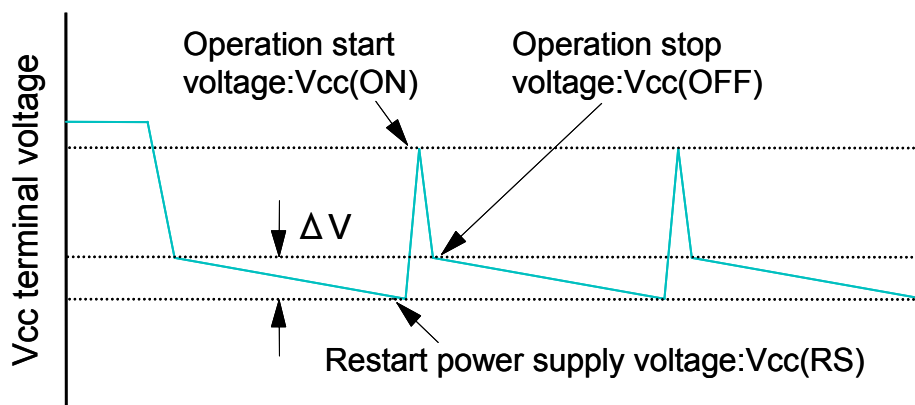


Fig 41 Input power suppression system

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STR-E1555

■General Description

STR-E1555 is a Hybrid IC power-factor-corrected switching mode power supply (SMPS). Start-up circuit and a controller of PFC and DC/DC parts are built in one chip. In addition, this chip and Power MOS FET for DC/DC part are incorporated into a SIP package thanks to High Voltage BCD Process technology. STR-E1555 includes the System of Prioritized PFC-Startup for prevention of Start-up Error.

Our proprietary Multi Mode Control system simplifies the design of High Efficiency and Low EMI power supply system with a small number of discrete components.

Additionally, since built-in Auto Standby Function with AC input compensation reduces power consumption at standby, STR-E1555 is optimum for downsizing and standardization of power supply system. STR-E1555 enables to configure the optimum system for diverse PFC outputs because the power MOSFET is provided externally.

■Features

● Integrated PFC Control Block

1. Critical Conduction Mode for High Efficiency and Low EMI

2. Built-in Multiplier with AC input compensation

● High Efficiency and Low EMI DC/DC Control Block

1. Multi Mode Control

(1) Quasi Resonant

----- Middle ~ Heavy Load

(2) PWM (100kHz) with Frequency Jitter

----- Light ~ Middle Load

(3) Low Frequency Operation

----- No Load ~ Extremely Light Load

● PFC \Leftrightarrow DC/DC Part Harmonized Operation System

1. PFC Priority Start-up System for Prevention of Start-up error

2. Auto Standby System with AC input compensation

3. PFC operation stops automatically with delay timer (at standby)

● Protection Functions

1. Over Current Protection with AC input voltage compensation for PFC part (OCP)

2. High Speed Over Voltage Protection for PFC part (OVP)
<No latch mode>

3. Over Current Protection for DC/DC part (OCP)

4. Over Load Protection for DC/DC part (OLP)

5. Input Power Limitation System at Intermittent Oscillation

6. Thermal Shut Down (TSD)

7. External Latch Protection by External Signal (ELP)

■Package---SLA21Pin



Terminal No.	Symbol	Function
1	Startup	Input of startup current for DD and PFC part
2	NC	—
3	PFCout	Output of gate drive signal for MOSFET of PFC part
4	ZCD	Input of zero cross detection signal for PFC
5	CS	Input of drain current sense signal of PFC part
6	PFB/OVP	Input of control signal for constant voltage of PFC part, Input of over voltage protection signal of PFC part, Compensation of input for DD part
7	COMP	Output of Error Amp. ,phase compensation
8-9	GND	Ground of DD and PFC for control part
10	MultFP	Input of multiplier for PFC, Input of alteration signal for frequency of DD part, Input of alteration signal of output voltage for DD part, Compensation of AC input for PFC ,Input of latch signal for DD and PFC part
11	DLP	PFC OFF delay time adjust
12	BD	Input of bottom on detection of DD part
13	OCP	Input of over current detection signal of DD part
14	DFB	Input of control signal for constant voltage of DD part
15	Vcc	Input of power supply of DD and PFC for control part
16	DDout	Output of gate drive signal for MOSFET of DD part(pin cut)
17	Source	MOSFET Source for DD part
18-19	NC	—
20-21	Drain	MOSFET Drain for DD part

■Applications

- LCD-TV
- LCD-Monitor
- Projection-TV
- AC Adapter

*Electrical equipment requiring the measures against higher harmonics.

■Line-up

Part Number	Internal MOSFET	PFC Part (total) Output Power (Included DC/DC Output Power)	DC/DC Part Output Power
STR-E1555	650V / 0.7Ω	200W	200W
STR-E1565	800V / 1.8Ω		80W

The schematic diagram illustrates a power supply unit (PSU) for a 150W LED street lighting system. The circuit is powered by an 85V ~ 264V AC input, which is connected to a transformer (T1) with a 22kV primary and a 22kV secondary. The secondary is connected to a bridge rectifier (RC1) and a filter capacitor (C1). The rectified output is connected to the positive terminal of the LED string (D1) and the positive terminal of the power supply (P1). The negative terminal of the LED string (D2) is connected to the negative terminal of the power supply (N1). The power supply is a switching power supply (STR-E1555) with a 150W output. The circuit includes a feedback network (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100) and a compensation network (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100). 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Key Specifications

1 Absolute Maximum Ratings (Ta=25°C)

Parameter	Terminal	Symbol	Ratings	Unit	Note
Drain current	21-17	IDpeak ^{*1}	10	A	Single Pulse
Maximum switching current	21-17	IDMAX ^{*5}	9.2	A	Ta=-20 to +125°C
Single pulse avalanche energy	21-17	EAS ^{*2}	222	mJ	Single Pulse
					VDD=30V, L=10mH IL peak=5.4A
Input voltage for control part	15-9	Vcc	30	V	
MultFP terminal input current	10-9	ImultFp	10	mA	
Startup terminal voltage	1-9	Vstartup	-0.3 to 600	V	
CS terminal voltage	5-9	Vcs	-0.5 to +10	V	
PFB/OVP terminal voltage	6-9	VPFB/OVP	-0.5 to +7	V	
PFB/OVP terminal input current		IPFB/OVP	5	mA	
ZCD terminal input current	4-9	IZCD(I)	5	mA	
ZCD terminal output current		IZCD(O)	-5		
PFCout terminal source current	3-9	IoPFC(source)	300	mA	
PFCout terminal sink current	3-9	IoPFC(sink)	500	mA	
DFB terminal input voltage	14-9	VDFB	-0.5 to +15	V	
DFB terminal output current		IDFB	2.2	mA	
OCP terminal input voltage	13-9	VOCP	-0.5 to +7	V	
BD terminal input voltage	12-9	VBD	-0.5 to +7	V	
Power dissipation for MOSFET	-	PD1 ^{*3}	9.6	W	With infinite heatsink
			1.8		Without heatsink
Power dissipation for control part(MIC)	-	PD2 ^{*4}	1.1	W	
Operating ambient temperature	-	Top	-20 to +125	°C	
Storage temperature	-	Tstg	-40 to +125	°C	
Channel temperature	-	Tch	+150	°C	

*1 Refer to MOS FET A.S.O characteristic

*3 Refer to MOS FET Ta-PD1 characteristic

*5 Maximum switching current

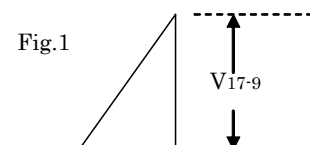
*2 Refer to MOS Tch-EAS characteristic

*4 Refer to MIC TF-PD2 characteristic

The maximum switching current is the Drain current determined by the drive voltage of the IC and threshold voltage (Vth) of MOS FET.

Therefore, in the event that voltage drop occurs between No.17 and No.9 terminals due to patterning, the maximum switching current decreases as shown by V17-9 in Fig.1

Accordingly please use this device within the decrease value, referring to the derating curve of the maximum switching current.



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2 Electrical Characteristics

2-1 Electrical Characteristics for Control Part (Vcc=20V, Ta=25°C unless otherwise specified)

2-1-1 Total device part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Operation start voltage	15-9	Vcc(ON)	14.5	16.0	17.5	V
Operation stop voltage	15-9	Vcc(OFF)	9.0	9.7	10.5	V
Circuit current in operation	15-9	Icc(ON)	-	-	22	mA
Circuit current in non-operation	15-9	Icc(OFF)	-	-	350	μA
Latch circuit release voltage ^{*6}	15-9	Vcc(La.off)	6.5	7.2	7.9	V
Input voltage in latch circuit operated ^{*6}	15-9	Vcc(La.on)	8.4	9.6	11.5	V
Latch circuit sustaining current ^{*6}	15-9	IH	-	500	1200	μA
Startup circuit	1-9	Istartup	3.4	5.4	7.7	mA
Bias current at startup terminal when startup circuit	1-9	Istartup(off)	-	20	80	μA
Latch threshold voltage of MultFP terminal	10-9	Vmult(La)	6.5	7.2	8.0	V
Restart power supply voltage	15-9	Vcc(RS)	7.0	7.8	8.6	V
Auto bias voltage	15-9	Vcc(BIAS)	10.1	11.0	11.8	V
Vcc(RS) - Vcc(La.off)	-	-	0.3	0.6	-	V
Vcc(OFF) - Vmult(La)	-	-	1.7	2.5	-	V
Thermal shutdown operating temperature	-	TSD	135	150	-	°C

^{*6} The latch circuit means a circuit operated an external signal over Latch threshold voltage of MultFP terminal.

2-1-2 PFC part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
PFB/OVP terminal threshold voltage(Hi)	6-9	VPFB(Hi)	3.905	4.000	4.056	V
PFB/OVP terminal input bias current	6-9	IPFB(B)	-5	-2	-	μA
COMP terminal source current	7-9	Icomp(SOU)	5	11	16	μA
COMP terminal sink current	7-9	Icomp(SIN)	-16	-11	-5	μA
COMP terminal Hi voltage	7-9	Vcomp(H)	5.8	6.4	-	V
COMP terminal Lo voltage	7-9	Vcomp(Hgl)	-	1.6	1.9	V
Over voltage detective input threshold voltage	6-9	VPFB(th)	4.14	4.27	4.40	V
MultFP terminal input bias current	10-9	Imult(B)	-10	-1	-	μA
Multiplier Gain	-	K	0.4	0.6	0.8	-
Zero Current Detective threshold voltage	4-9	VZCD(th)	1.4	1.6	1.8	V
Zero Current Detective hysteresis	4-9	VZCD(HIS)	150	190	260	mV
Zero Current Detective Hi clamp voltage	4-9	VZCD(HC)	6.0	6.6	7.0	V
Zero Current Detective Lo clamp voltage	4-9	VZCD(LC)	0.53	0.63	0.77	V

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Restart delay time	-	tDLY	150	520	-	μs
CS terminal input bias current	5-9	ICS (B)	-8.0	-1	-	μA
CS terminal input offset voltage	5-9	VCS (IOS)	-	16.9	25.0	mV
Maximum current sense input threshold	5-9	VCSMAX	1.18	1.37	1.52	V
Maximum current sense input threshold	5-9	VCSMAX	0.60	0.66	0.73	V
PFB/OVP terminal threshold voltage for DD Operation start signal	6-9	VPFB (DD ON)	2.9	3.2	3.5	V
PFCout terminal output voltage	3-9	VPFC OUT	10.2	11.8	-	V
Operation Voltage at UVLO	3-9	VPFCOUTUVLO	0.9	1.3	1.6	V

2-1-3 DD Part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Oscillation frequency (1)	16-9	fosc(1)	91	100	109	kHz
Oscillation frequency (2)	16-9	fosc(2)	76	83	90	kHz
Maximum ON time(1)	16-9	T _{ON} (MAX1)	7.4	8.8	9.7	μs
Maximum ON time(2)	16-9	T _{ON} (MAX2)	9.0	10.7	11.7	μs
Bottom detective terminal input threshold voltage	12-9	VBD (th)	0.67	0.76	0.84	V
Bottom detective terminal input bias current	12-9	I BD (B)	-6	-3	-	μA
OCP terminal detective voltage(1)	13-9	VOCP(1)	0.70	0.76	0.82	V
OCP terminal detective voltage(2)	13-9	VOCP(2)	0.54	0.60	0.66	V
OCP terminal input bias current	13-9	IOCP(B)	-12	-6	-	μA
Standby operation start on-time	16-9	TON (STB IN)	290	350	410	ns
Minimum on-time in Standby operation (1)	16-9	TON(STBMIN	460	580	700	ns
Minimum on-time in Standby operation (2)	16-9	TON(STBMIN	0.8	1.2	1.6	μs
Standby operation Release on-time(1)	16-9	TON(STBout1)	1.61	1.96	2.31	μs
Standby operation Release on-time(2)	16-9	TON(STBout2)	2.58	3.18	3.78	μs
Standby detective voltage at input compensation	6-9	VPFB(STB)	1.8	2.4	3.0	V
DLP terminal constant current L	11-9	IDLPL	-	1	4	μA
DLP terminal constant current H	11-9	IDLPH	20	40	60	μA
DLP terminal threshold voltage L for	11-9	VDLPL	0.7	0.9	1.1	V
DLP terminal threshold voltage H for	11-9	VDLPH	4.1	4.6	5.1	V
DFB terminal constant current	14-9	ICONST	15	21	27	μA
OLP terminal threshold voltage	14-9	VOLP	5.9	6.5	7.3	V
DD out terminal output voltage	16-9	VDDOUT	11.7	12.5	-	V

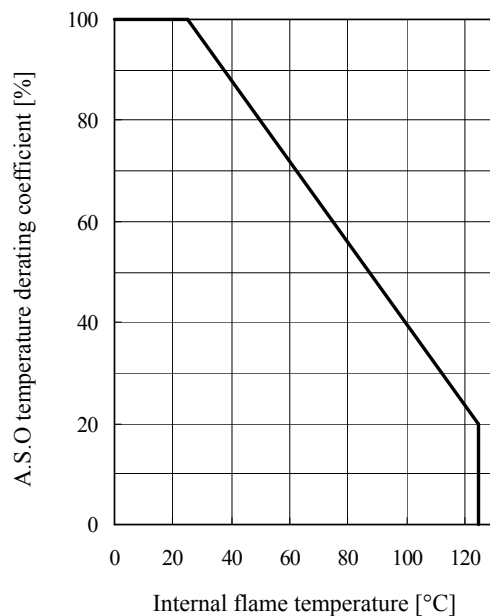
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2-2 Electrical characteristics for MOSFET(Ta=25°C)

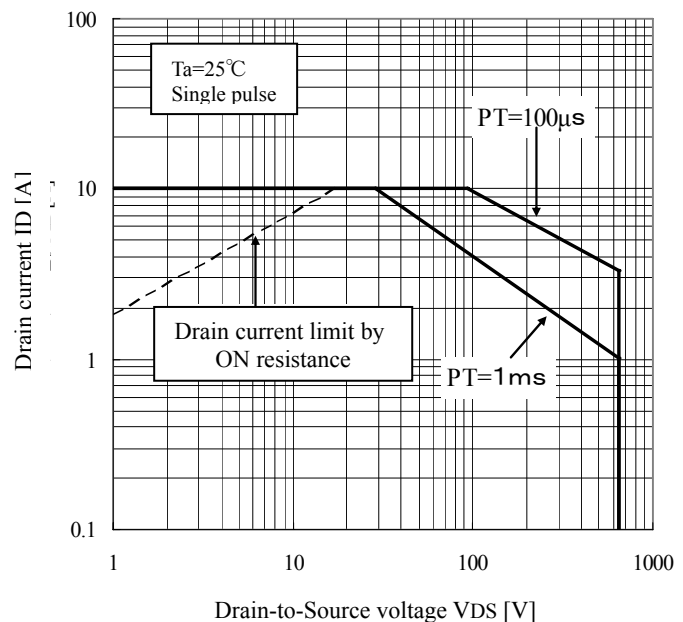
Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Drain-to-Source breakdown voltage	21-17	VDSS	650	-	-	V
Drain leakage current	21-17	IDSS	-	-	300	μA
On-resistance	21-17	RDS(ON)	-	-	0.7	Ω
Switching time	21-17	tf	-	-	450	ns
Thermal resistance *	-	θch-F	-	-	1.7	°C/W

*Between channel and internal frame

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Fig2 A.S.O. temperature derating coefficient characteristic



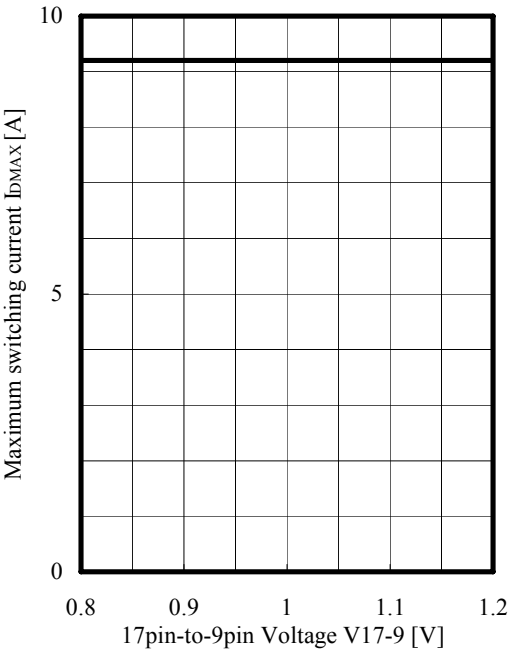
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Fig3 MOSFET A.S.O. characteristic (Ta=25°C/single pulse)



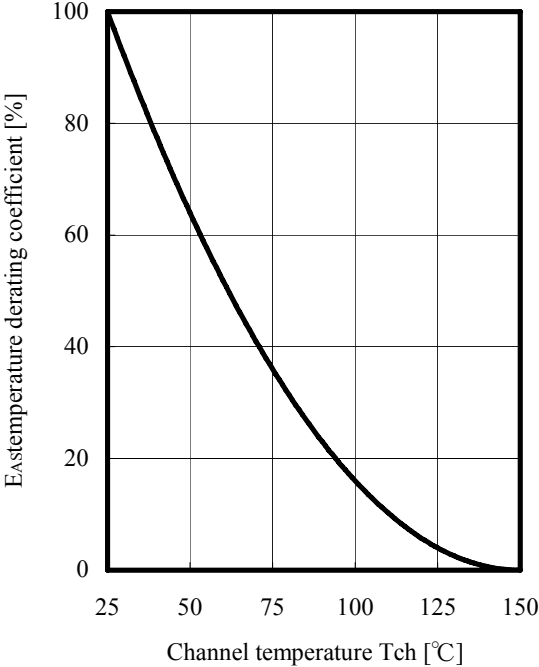
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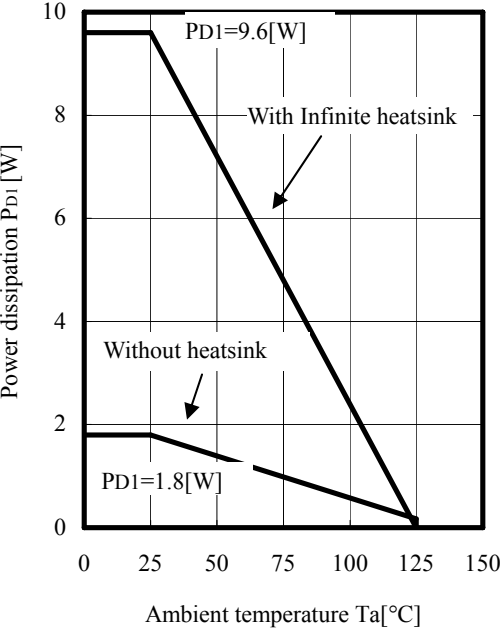
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Fig4 Maximum switching current
derating characteristic



STR-E1555
Fig5 Avalanche energy derating
characteristic



STR-E1555
Fig6 MOSFET Ta-PD1
characteristic

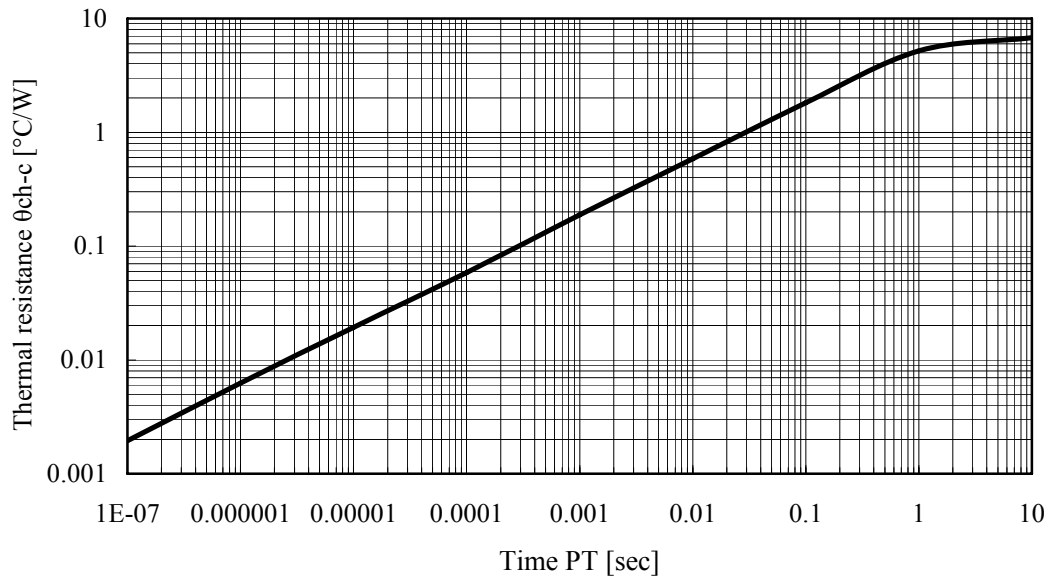


Power dissipation Pd2[W]

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Fig8 MOSFET Transient thermal resistance characteristic



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CAUTION / WARNING

Since reliability can be affected adversely by improper storage environment and handling methods during Characteristic tests, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%) and avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust in leads and solderability that have been stored for a long time.

Cautions for characteristic Tests and Handling

When characteristic tests are carried out during inspection testing and other standard tests periods, protect the devices from surge of power from the testing device, shorts between the devices and the heatsink.

Remarks in using silicone grease for a heatsink

When silicone grease is used in mounting this product on a heatsink, it shall be applied evenly and thinly. If more silicone grease than required is applied, it may produce forced stress.

Volatile type silicone grease may produce cracks after elapse of long term, resulting in reducing heat radiation effect. Silicone grease with low consistency (hard grease) may cause cracks in the mold resin when screwing the product to a heatsink.

Recommended operating temperature

Inner frame temperature in operation $T_F=105(^{\circ}\text{C})\text{MAX.}$

Recommended Screw Torque

0.588 to 0.785[N•m] (6 to 8[kgf•cm])

Soldering Temperature

When soldering the products, please be sure to minimize the working time, within the following conditions.

- $260\pm 5^{\circ}\text{C}$ 10sec.
- $350\pm 5^{\circ}\text{C}$ 3sec. (Soldering iron)

Considerations to protect the Products from Electrostatic Discharge

- When handling the devices, operator must be grounded. Grounded wrist straps be worn and should have at least $1\text{M}\Omega$ of resistance near operators to ground to prevent shock hazard.
- Workbenches where the devices are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should also be grounded.
- When soldering the devices, the head of a soldering iron or a solder bath must be grounded in other to prevent leak voltage generated by them from being applied to the devices.
- The devices should always be stored and transported in our shipping containers or conductive containers, or be wrapped up in aluminum foil.

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STR-E1565

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■General Description

STR-E1565 is a Hybrid IC power-factor-corrected switching mode power supply (SMPS). Start-up circuit and a controller of PFC and DC/DC parts are built in one chip. In addition, this chip and Power MOS FET for DC/DC part are incorporated into a SIP package thanks to High Voltage BCD Process technology. STR-E1565 includes the System of Prioritized PFC-Startup for prevention of Start-up Error.

Our proprietary Multi Mode Control system simplifies the design of High Efficiency and Low EMI power supply system with a small number of discrete components.

Additionally, since built-in Auto Standby Function with AC input compensation reduces power consumption at standby, STR-E1565 is optimum for downsizing and standardization of power supply system. STR-E1565 enables to configure the optimum system for diverse PFC outputs because the power MOSFET is provided externally.

■Features

● Integrated PFC Control Block

1. Critical Conduction Mode for High Efficiency and Low EMI

2. Built-in Multiplier with AC input compensation

● High Efficiency and Low EMI DC/DC Control Block

1. Multi Mode Control

(1) Quasi Resonant Operation

----- Middle to Heavy Load

(2) PWM(100kHz) with Frequency Jitter

----- Light to Middle Load

(3) Low Frequency Operation

----- No Load to Extremely Light Load

● PFC <=> DC/DC Part Harmonized Operation System

1. PFC Priority Start-up System for Prevention of Start-up error

2. Auto Standby System with AC input compensation

3. PFC operation stops automatically with delay timer (at standby)

● Protection Functions

1. Over Current Protection with AC input voltage compensation for PFC part (OCP)

2. High Speed Over Voltage Protection for PFC part (OVP)
<Without latch mode>

3. Over Current Protection for DC/DC part (OCP)

4. Over Load Protection for DC/DC part (OLP)

5. Input Power Limitation System at Intermittent Oscillation

6. Thermal Shut Down (TSD)

7. External Latch Protection by External Signal (ELP)

■Package---SLA21Pin



Terminal No.	Symbol	Function
1	Startup	Input of startup current for DD and PFC part
2	NC	—
3	PFCout	Output of gate drive signal for MOSFET of PFC part
4	ZCD	Input of zero cross detection signal for PFC
5	CS	Input of drain current sense signal of PFC part
6	PFB/OVP	Input of control signal for constant voltage of PFC part, Input of over voltage protection signal of PFC part, Compensation of input for DD part
7	COMP	Output of Error Amp., phase compensation
8, 9	GND	Ground of DD and PFC for control part
10	MultFP	Input of multiplier for PFC, Input of alteration signal for frequency of DD part, Input of alteration signal of output voltage for DD part, Compensation of AC input for PFC, Input of latch signal for DD and PFC part
11	DLP	PFC OFF delay time adjust
12	BD	Input of bottom on detection of DD part
13	OCP	Input of over current detection signal of DD part
14	DFB	Input of control signal for constant voltage of DD part
15	Vcc	Input of power supply of DD and PFC for control part
16	DDout	Output of gate drive signal for MOSFET of DD part (pin cut)
17	Source	MOSFET Source for DD part
18, 19	NC	—
20, 21	Drain	MOSFET Drain for DD part

■Applications

- LCD-TV
- LCD-Monitor
- Projection-TV
- AC Adapter

*Electrical equipment requiring the measures against higher harmonics.

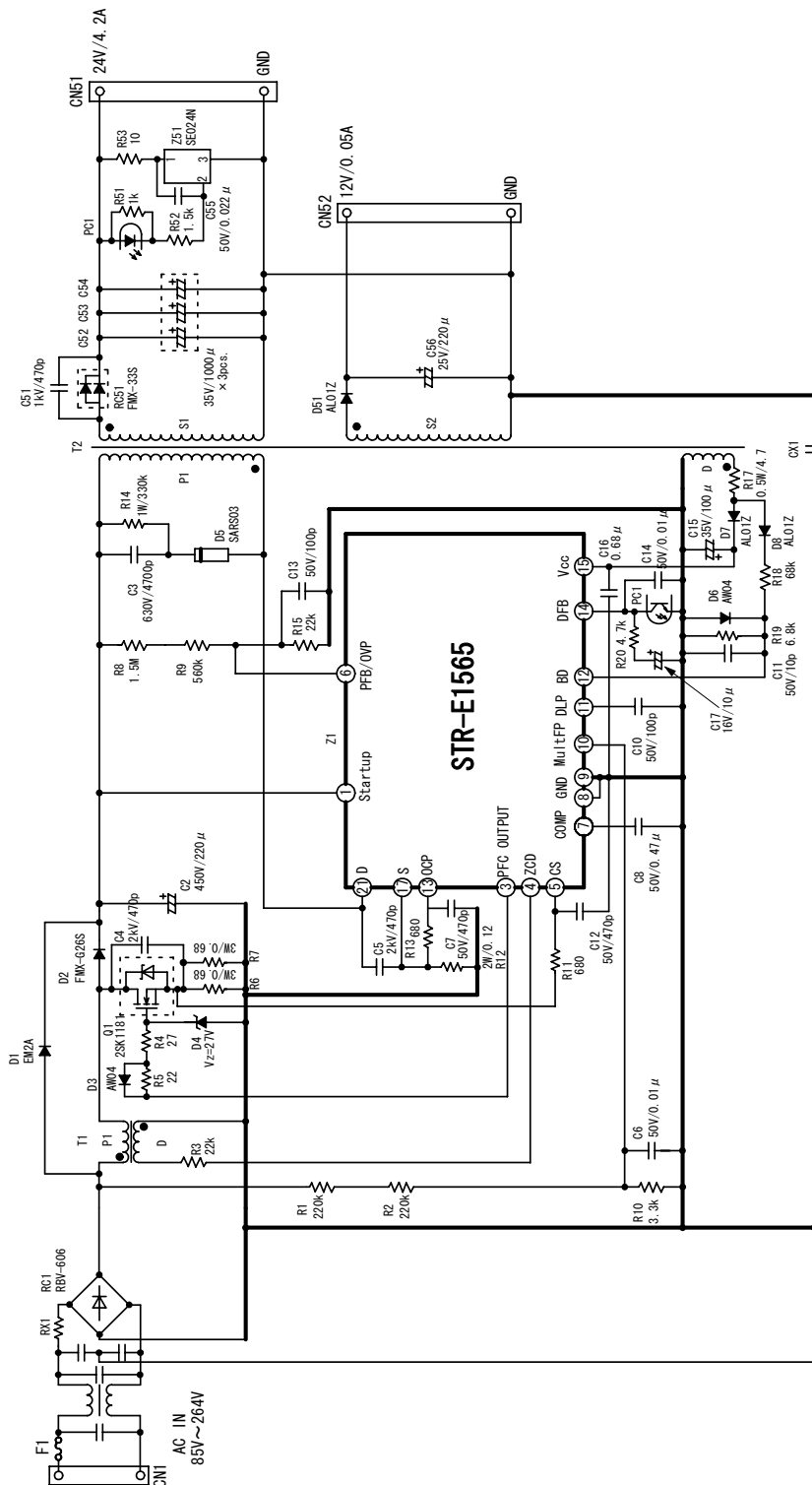
■Line-up

Part Number	Built-in MOSFET	PFC Part (total) Output Power (Including DC/DC Output Power)	DC/DC Part Output Power
STR-E1555	650V / 0.7Ω	200W	200W
STR-E1565	800V / 1.8Ω		80W

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Typical Connection



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Key Specifications

1 Absolute Maximum Ratings (Ta=25°C)

Parameter	Terminals	Symbol	Ratings	Unit	Note
Drain current	21-17	IDpeak ^{*1}	10	A	Single Pulse
Maximum switching current	21-17	IDMAX ^{*5}	5.2	A	Ta=-20~+125°C
Single pulse avalanche energy	21-17	EAS ^{*2}	150	mJ	Single Pulse
					VDD=30V, L=10mH ILpeak=5.4A
Input voltage for control part	15-9	Vcc	30	V	
MultFP terminal input current	10-9	ImultFp	10	mA	
Startup terminal voltage	1-9	Vstartup	-0.3~600	V	
CS terminal voltage	5-9	Vcs	-0.5~+10	V	
PFB/OVP terminal voltage	6-9	VPFB/OVP	-0.5~+7	V	
PFB/OVP terminal input current		IPFB/OVP	5	mA	
ZCD terminal input current	4-9	IZCD(I)	5	mA	
ZCD terminal output current		IZCD(O)	-5		
PFCout terminal source current	3-9	IoPFC(source)	300	mA	
PFCout terminal sink current	3-9	IoPFC(sink)	500	mA	
DFB terminal input voltage	14-9	VDFB	-0.5~+15	V	
DFB terminal output current		IDFB	2.2	mA	
OCP terminal input voltage	13-9	VOCP	-0.5~+7	V	
BD terminal input voltage	12-9	VBD	-0.5~+7	V	
Power dissipation for MOSFET	—	PD1 ^{*3}	8.9	W	With infinite heatsink
			1.8		Without heatsink
Power dissipation for control part(MIC)	—	PD2 ^{*4}	1.1	W	
Operating ambient temperature	—	Top	-20 ~ +125	°C	
Storage temperature	—	Tstg	-40 ~ +125	°C	
Channel temperature	—	Tch	+150	°C	

*1 Refer to MOS FET A.S.O curve

*2 Refer to MOS Tch-EAS curve

*3 Refer to MOS FET Ta-PD1 curve

*4 Refer to MIC TF-PD2 curve

*5 Maximum switching current

The maximum switching current is the Drain current determined by the drive voltage of the IC and threshold voltage (Vth) of MOS FET.

Therefore, in the event that voltage drop occurs between No.17 and No.9 terminals due to patterning, the maximum switching current decreases as shown by V17-9 in Fig.1. Accordingly please use this device within the decrease value, referring to the derating curve of the maximum switching current.

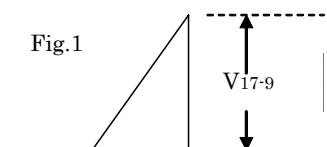


Fig.1

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2 Electrical Characteristics

2-1 Electrical Characteristics for Control Part (Vcc=20V, Ta=25°C unless otherwise specified)

2-1-1 Total device part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Operation start voltage	15-9	Vcc(ON)	14.5	16.0	17.5	V
Operation stop voltage	15-9	Vcc(OFF)	9.0	9.7	10.5	V
Circuit current in operation	15-9	Icc(ON)	—	—	22	mA
Circuit current in non-operation	15-9	Icc(OFF)	—	—	350	μA
Latch circuit release voltage ^{*6}	15-9	Vcc(La.off)	6.5	7.2	7.9	V
Input voltage in latch circuit operated ^{*6}	15-9	Vcc(La.on)	8.4	9.6	11.5	V
Latch circuit sustaining current ^{*6}	15-9	IH	—	500	1200	μA
Startup circuit	1-9	Istartup	3.4	5.4	7.7	mA
Bias current at startup terminal when startup circuit	1-9	Istartup(off)	—	20	80	μA
Latch threshold voltage of MultFP terminal	10-9	Vmult(La)	6.5	7.2	8.0	V
Restart power supply voltage	15-9	Vcc(RS)	7.0	7.8	8.6	V
Auto bias voltage	15-9	Vcc(BIAS)	10.1	11.0	11.8	V
Vcc(RS) — Vcc(La.off)	—	—	0.3	0.6	—	V
Vcc(OFF) — Vmult(La)	—	—	1.7	2.5	—	V
Thermal shutdown operating temperature	—	TSD	135	150	—	°C

*6 The latch circuit means a circuit operated an external signal over Latch threshold voltage of MultFP terminal.

2-1-2 PFC part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
PFB/OVP terminal threshold voltage(Hi)	6-9	VPFB(Hi)	3.905	4.000	4.056	V
PFB/OVP terminal input bias current	6-9	IPFB(B)	-5	-2	—	μA
COMP terminal source current	7-9	Icomp(SOU)	5	11	16	μA
COMP terminal sink current	7-9	Icomp(SIN)	-16	-11	-5	μA
COMP terminal Hi voltage	7-9	Vcomp(H)	5.8	6.4	—	V
COMP terminal Lo voltage	7-9	Vcomp(Hgl)	—	1.6	1.9	V
Over voltage detective input threshold voltage	6-9	VPFB(th)	4.14	4.27	4.40	V
MultFP terminal input bias current	10-9	Imult(B)	-10	-1	—	μA
Multiplier Gain	—	K	0.4	0.6	0.8	—
Zero Current Detective threshold voltage	4-9	VZCD(th)	1.4	1.6	1.8	V
Zero Current Detective hysteresis	4-9	VZCD(HIS)	150	190	260	mV
Zero Current Detective Hi clamp voltage	4-9	VZCD(HC)	6.0	6.6	7.0	V
Zero Current Detective Lo clamp voltage	4-9	VZCD(LC)	0.53	0.63	0.77	V
Restart delay time	—	tDLY	150	520	—	μs

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CS terminal input bias current	5-9	ICS (B)	-8.0	-1	—	μA
CS terminal input offset voltage	5-9	VCS (IOS)	—	16.9	25.0	mV
Maximum current sense input threshold	5-9	VCSMAX(Ⓢ1)	1.18	1.37	1.52	V
Maximum current sense input threshold	5-9	VCSMAX(Ⓢ2)	0.60	0.66	0.73	V
PFB/OVP terminal threshold voltage for DD Operation start signal	6-9	VPFB(DD ON)	2.9	3.2	3.5	V
PFCout terminal output voltage	3-9	VPCOUT	10.2	11.8	—	V
Operation Voltage at UVLO	3-9	VPCOUTUVLO	0.9	1.3	1.6	V

2-1-3 DD Part

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Oscillation frequency (1)	16-9	fosc(1)	91	100	109	kHz
Oscillation frequency (2)	16-9	fosc(2)	76	83	90	kHz
Maximum ON time(1)	16-9	T _{ON} (MAX1)	7.4	8.8	9.7	μs
Maximum ON time(2)	16-9	T _{ON} (MAX2)	9.0	10.7	11.7	μs
Bottom detective terminal input threshold voltage	12-9	VBD(Ⓢ)	0.67	0.76	0.84	V
Bottom detective terminal input bias current	12-9	IBD(B)	-6	-3	—	μA
OCP terminal detective voltage(1)	13-9	VOCP(1)	0.70	0.76	0.82	V
OCP terminal detective voltage(2)	13-9	VOCP(2)	0.54	0.60	0.66	V
OCP terminal input bias current	13-9	IOCP(B)	-12	-6	—	μA
Standby operation start on-time	16-9	TON(STB IN)	290	350	410	ns
Minimum on-time in Standby operation (1)	16-9	TON(STBMIN1)	460	580	700	ns
Minimum on-time in Standby operation (2)	16-9	TON(STBMIN2)	0.8	1.2	1.6	μs
Standby operation Release on-time(1)	16-9	TON(STBout1)	1.50	1.85	2.20	μs
Standby operation Release on-time(2)	16-9	TON(STBout2)	2.4	3.0	3.6	μs
Standby detective voltage at input compensation	6-9	VPFB(STB)	1.8	2.4	3.0	V
DLP terminal constant current L	11-9	IDLPL	—	1	4	μA
DLP terminal constant current H	11-9	IDLPH	20	40	60	μA
DLP terminal threshold voltage L for	11-9	VDLPL	0.7	0.9	1.1	V
DLP terminal threshold voltage H for	11-9	VDLPH	4.1	4.6	5.1	V
DFB terminal constant current	14-9	ICONST	15	21	27	μA
OLP terminal threshold voltage	14-9	VOLP	5.9	6.5	7.3	V
DD out terminal output voltage	16-9	VDDOUT	11.7	12.5	—	V

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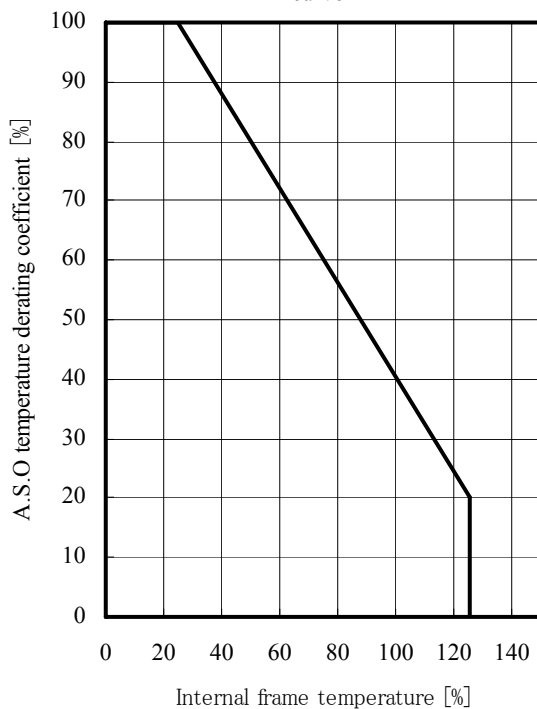
2-2 Electrical characteristics for MOSFET(Ta=25°C)

Parameter	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Drain-to-Source breakdown voltage	21-17	VDSS	800	—	—	V
Drain leakage current	21-17	IDSS	—	—	300	μA
On-resistance	21-17	RDS(ON)	—	—	1.8	Ω
Switching time	21-17	tf	—	—	350	ns
Thermal resistance *	—	θch-F	—	—	3.3	°C/W

* Between channel and internal frame

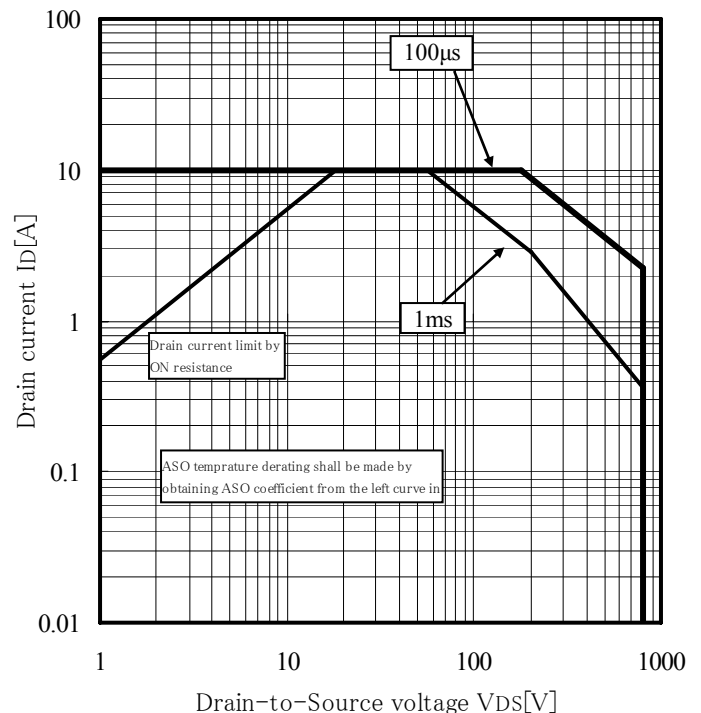
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Fig2. A.S.O.temperature derating coefficient curve



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Fig3. MOSFET A.S.O.curve (Ta=25°C/Single Pulse)

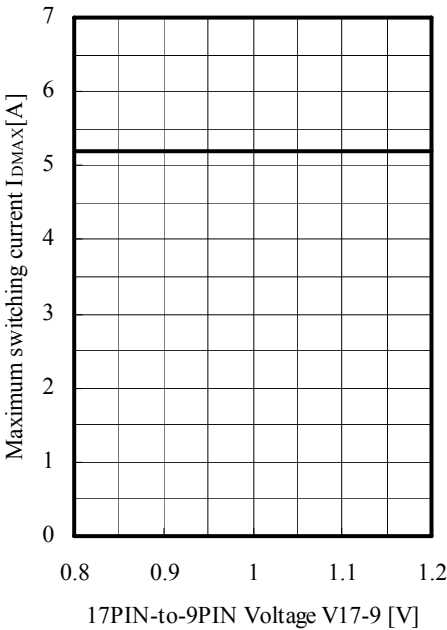


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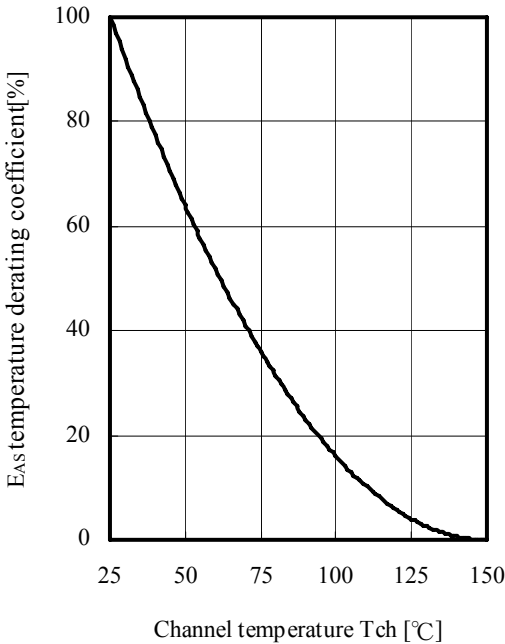
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Fig4. Maximum switching current derating curve



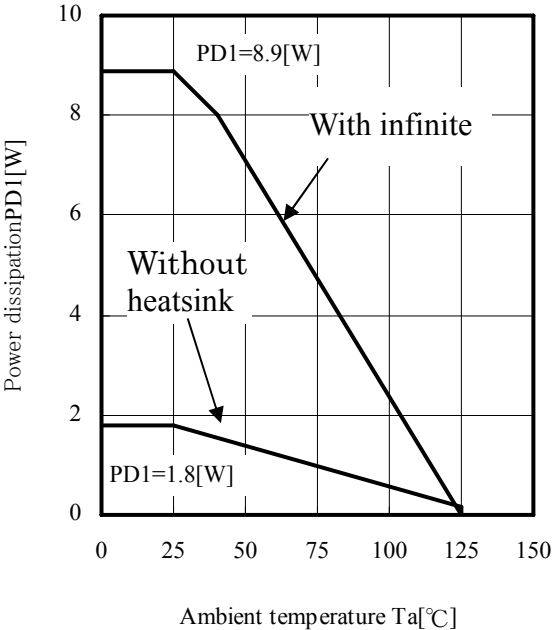
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Fig5. Avalanche energy derating curve



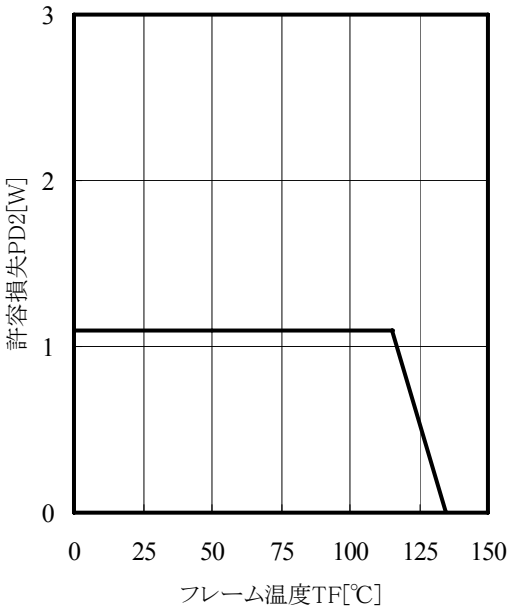
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Fig6. MOSFET Ta-PD1 curve



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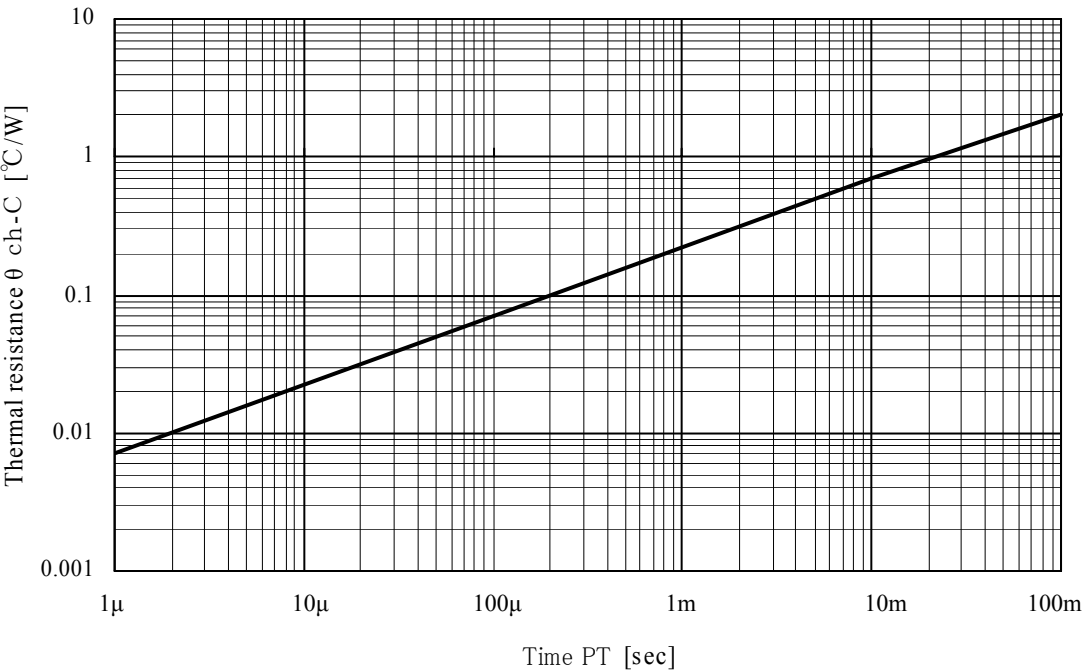
Fig7. MIC TF-PD2 curve



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Fig8. Transient thermal resistance curve



Technical drawings of the PCB layout for the 20-pin connector. The top drawing is a top view showing dimensions: overall width 31.0 ± 0.2 , pin pitch $20 \times P1.43 \pm 0.5 = 28.6 \pm 1$, and various mounting hole and feature dimensions. The bottom drawing is a side view showing the profile of the 20 pins, with dimensions for pin height and spacing. The text indicates that pins 2, 18, and 19 are decuted.

- Material of terminal : Cu
- Treatment of terminal : Ni plating+Solder dip (Pb free)
- Weight : Approx 5.6g

Dimensions : mm

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CAUTION / WARNING

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Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%) and avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust in leads and solderability that have been stored for a long time.

Cautions for characteristic Tests and Handling

When characteristic tests are carried out during inspection testing and other standard tests periods, protect the devices from surge of power from the testing device, shorts between the devices and the heatsink.

Remarks in using silicone grease for a heatsink

When silicone grease is used in mounting this product on a heatsink, it shall be applied evenly and thinly. If more silicone grease than required is applied, it may produce forced stress.

Volatile type silicone grease may produce cracks after elapse of long term, resulting in reducing heat radiation effect. Silicone grease with low consistency (hard grease) may cause cracks in the mold resin when screwing the product to a heatsink.

Recommended operating temperature

Inner frame temperature in operation TF=105 (°C)MAX.

Recommended Screw Torque

0.588 to 0.785[N·m] (6~8[kgf·cm])

Soldering Temperature

When soldering the products, please be sure to minimize the working time, within the following conditions.

- 260±5°C 10sec.
- 350±5°C 3sec. (Soldering iron)

Considerations to protect the Products from Electrostatic Discharge

- When handling the devices, operator must be grounded. Grounded wrist straps be worn and should have at least 1MΩ of resistance near operators to ground to prevent shock hazard.
- Workbenches where the devices are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should also be grounded.
- When soldering the devices, the head of a soldering iron or a solder bath must be grounded in other to prevent leak voltage generated by them from being applied to the devices.
- The devices should always be stored and transported in our shipping containers or conductive containers, or be wrapped up in aluminum foil.

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