

Vishay General Semiconductor

Surface Mount Schottky Barrier Rectifier



SMC (DO-214AB)

PRIMARY CHARACTERISTICS						
I _{F(AV)} 3.0 A						
V _{RRM}	20 V, 30 V, 40 V, 50 V, 60 V					
I _{FSM}	100 A					
EAS	20 mJ					
V _F	0.5 V, 0.75 V					
T _J max.	150 °C					
Package	SMC (DO-214AB)					
Diode variations	Single					

FEATURES

- Low profile package
- · Ideal for automated placement
- · Guardring for overvoltage protection
- Low power losses, high efficiency
- Low forward voltage drop
- · High surge capability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- AEC-Q101 qualified available
 Automotive ordering code: base P/NHE3 or P/NHM3
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

TYPICAL APPLICATIONS

For use in low voltage high frequency inverters, freewheeling, DC/DC converters, and polarity protection applications.

MECHANICAL DATA

Case: SMC (DO-214AB)

Molding compound meets UL 94 V-0 flammability rating Base P/N-E3 - RoHS-compliant, commercial grade Base P/N-M3 - halogen-free, RoHS-compliant, commercial grade

Base P/NHE3_X - RoHS-compliant and AEC-Q101 qualified Base P/NHM3_X - halogen-free, RoHS-compliant, and AEC-Q101 qualified

("_X" denotes revision code e.g. A, B,)

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

E3, M3, HE3, and HM3 suffix meets JESD 201 class 2 whisker test

Polarity: color band denotes the cathode end

MAXIMUM RATINGS ($T_A = 25$ °C unless otherwise noted)							
PARAMETER	SYMBOL	SS32	SS33	SS34	SS35	SS36	UNIT
Device marking code		S2	S3	S4	S5	S6	
Maximum repetitive peak reverse voltage	V _{RRM}	20	30	40	50	60	V
Maximum RMS voltage	V _{RMS}	14	21	28	35	42	V
Maximum DC blocking voltage	V _{DC}	20	30	40	50	60	V
Maximum average forward rectified current at T_L (fig. 1)	I _{F(AV)}	3.0				А	
Peak forward surge current 8.3 ms single half sine-wave superimposed on rated load	I _{FSM}	100				А	
Non-repetitive avalanche energy at $T_A = 25$ °C, $I_{AS} = 2.0$ A, L = 10 mH	E _{AS}	20				mJ	
Voltage rate of change (rated V _R)	dV/dt	10 000 V				V/µs	
Operating junction temperature range	TJ	-55 to +150 °C				°C	
Storage temperature range	T _{STG}	-55 to +150 °C			°C		

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1

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HALOGEN

FREE





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ELECTRICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$ unless otherwise noted)									
PARAMETER	TEST C	ONDITIONS	SYMBOL	SS32	SS33	SS34	SS35	SS36	UNIT
Maximum instantaneous forward voltage ⁽¹⁾	3.0 A		V _F		0.5		0.	75	V
Maximum DC reverse current		T _A = 25 °C	L_	0.5				mA	
at rated DC blocking voltage ⁽¹⁾		T _A = 100 °C	IR		20		1	0	ШA

Note

 $^{(1)}\,$ Pulse test: 300 μs pulse width, 1 % duty cycle

THERMAL CHARACTERISTICS ($T_A = 25 \text{ °C}$ unless otherwise noted)							
PARAMETER	SYMBOL	SS32	SS33	SS34	SS35	SS36	UNIT
Typical thermal resistance ⁽¹⁾	$R_{\theta JA}$	55					°C/W
	$R_{\theta JL}$	17					0/10

Note

 $^{(1)}\,$ PCB mounted with 0.55" x 0.55" (14 mm x 14 mm) copper pad areas

ORDERING INFORMATION (Example)								
PREFERRED P/N	UNIT WEIGHT (g)	PREFERRED PACKAGE CODE	BASE QUANTITY	DELIVERY MODE				
SS36-E3/57T	0.235	57T	850	7" diameter plastic tape and reel				
SS36-E3/9AT	0.235	9AT	3500	13" diameter plastic tape and reel				
SS36HE3_A/H (1)	0.235	Н	850	7" diameter plastic tape and reel				
SS36HE3_A/I (1)	0.235	I	3500	13" diameter plastic tape and reel				
SS36-M3/57T	0.235	57T	850	7" diameter plastic tape and reel				
SS36-M3/9AT	0.235	9AT	3500	13" diameter plastic tape and reel				
SS36HM3_A/H ⁽¹⁾	0.235	Н	850	7" diameter plastic tape and reel				
SS36HM3_A/I ⁽¹⁾	0.235	I	3500	13" diameter plastic tape and reel				

Note

⁽¹⁾ AEC-Q101 qualified

RATINGS AND CHARACTERISTICS CURVES ($T_A = 25$ °C unless otherwise noted)

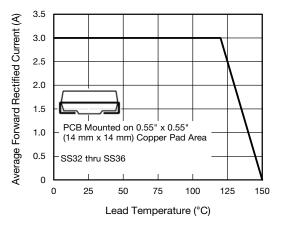


Fig. 1 - Forward Current Derating Curve

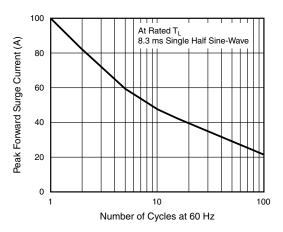


Fig. 2 - Maximum Non-Repetitive Peak Forward Surge Current

Revision: 21-Jul-17

2

Document Number: 88751

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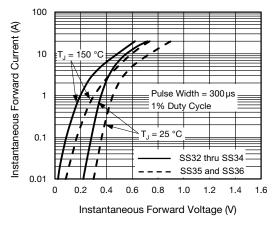


Fig. 3 - Typical Instantaneous Forward Characteristics

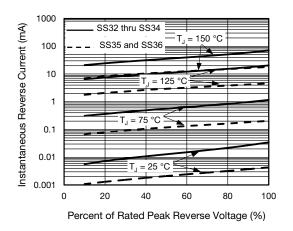
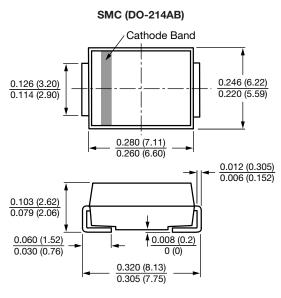


Fig. 4 - Typical Reverse Current Characteristics





SS32, SS33, SS34, SS35, SS36

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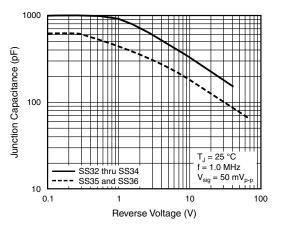


Fig. 5 - Typical Junction Capacitance

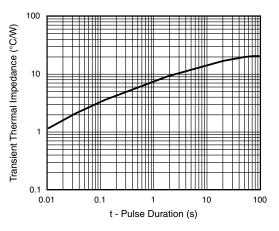
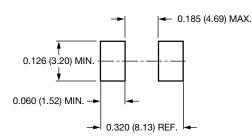


Fig. 6 - Typical Transient Thermal Impedance

Mounting Pad Layout



Revision: 21-Jul-17

3

Document Number: 88751

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