

NCP4300A

Dual Operational Amplifier and Voltage Reference

The NCP4300A is a monolithic integrated circuit specifically designed to control the output current and voltage levels of switch mode battery chargers and power supplies. This device contains a precision 2.6 V shunt reference and two operational amplifiers. Op-Amp 1 is designed to perform voltage control and has its non-inverting input internally connected to the reference. Op-Amp 2 is designed for current control and has both inputs uncommitted. The NCP4300A offers the power converter designer a control solution that features increased precision with a corresponding reduction in system complexity and cost. This device is available in an 8-lead surface mount package.

Features

- This is a Pb-Free Device

Operational Amplifier

- Low Input Offset Voltage: 0.5 mV
- Input Common Mode Voltage Range Includes Ground
- Low Supply Current: 210 μ A/Op-Amp (@ $V_{CC} = 5.0$ V)
- Medium Unity Gain Bandwidth: 0.7 MHz
- Large Output Voltage Swing: 0 V to $V_{CC} - 1.5$ V
- Wide Power Supply Voltage Range: 3.0 V to 35 V

Voltage Reference

- Fixed Output Voltage Reference: 2.60 V
- High Precision Over Temperature: 1.0%
- Wide Sink Current Range: 80 μ A to 80 mA

Typical Applications

- Battery Charger
- Switch Mode Power Supply

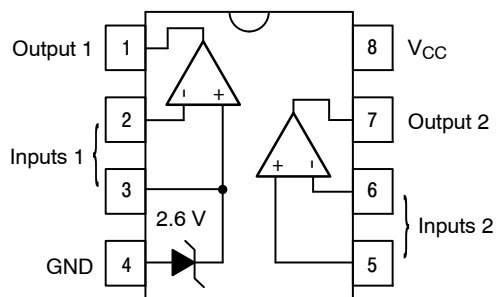


Figure 1. Functional Block Diagram



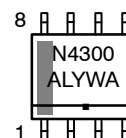
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MARKING DIAGRAM

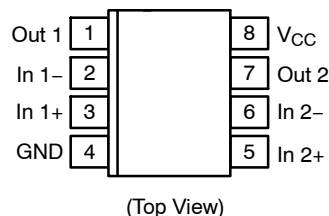


SOIC-8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
A = Option Code
▪ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|------------------|------------------|
| NCP4300ADG | SOIC-8 (Pb-Free) | 98 Units / Rail |
| NCP4300ADR2G | SOIC-8 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP4300A

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-----------|------------------------|------|
| Supply Voltage (V_{CC} to GND) | V_{CC} | 36 | V |
| ESD Protection Voltage at any Pin (Human Body Model) | V_{ESD} | 2.0 K (min) | V |
| Op-Amp 1 and 2 Input Voltage Range (Pins 2, 5, 6) | V_{IR} | -0.6 to $V_{CC} + 0.6$ | V |
| Op-Amp 2 Input Differential Voltage Range (Pins 5, 6) | V_{IDR} | V_{CC} to GND | V |
| Voltage Reference Cathode Current (Pin 3) | I_K | 100 | mA |
| Maximum Junction Temperature | T_J | 150 | °C |
| Operating Ambient Temperature Range | T_A | 0 to 105 | °C |
| Storage Temperature Range | T_{stg} | -55 to 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 155 | °C/W |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 45 | °C/W |

TYPICAL ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------|-----|------|-----|------|
| Total Supply Current, excluding Current in the Voltage Reference $V_{CC} = 5.0$ V, no load; $0^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ | I_{CC} | - | 0.42 | 0.8 | mA |

Op-Amp 1 (Op-amp with non-inverting input connected to the internal Vref)

($V_{CC} = 5.0$ V, $V_{out} = 1.4$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted)

| | | | | | |
|--|--------------------------|----------|----------|--------------|------------------------------|
| Input Offset Voltage $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 105°C | V_{IO} | - - | 0.5 - | 2.0 3.0 | mV |
| Input Offset Voltage Temperature Coefficient $T_A = 0^\circ\text{C}$ to 105°C | $\Delta V_{IO}/\Delta T$ | - | 7.0 | - | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current (Inverting input only) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 105°C | I_{IB} | - - | -50 - | -150 -150 | nA |
| Large Signal Voltage Gain ($V_{CC} = 15$ V, $R_L = 2.0$ k Ω , $V_{out} = 1.4$ V to 11.4 V) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 105°C | A_{VOL} | 50 25 | 100 - | - - | V/mV |
| Power Supply Rejection ($V_{CC} = 5.0$ V to 30 V) | PSRR | 40 | 90 | - | dB |
| Output Source Current ($V_{CC} = 15$ V, $V_{out} = 2.0$ V, $V_{ID} = +1.0$ V) | I_{O+} | 10 | 16 | - | mA |
| Output Sink Current ($V_{CC} = 15$ V, $V_{out} = 2.0$ V, $V_{ID} = -1.0$ V) | I_{O-} | 10 | 25 | - | mA |
| Output Voltage Swing, High ($V_{CC} = 30$ V, $R_L = 10$ k Ω , $V_{ID} = +1.0$ V) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 105°C | V_{OH} | 27 27 | 28 - | - - | V |
| Output Voltage Swing, Low ($R_L = 10$ k Ω , $V_{ID} = -1.0$ V) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to 105°C | V_{OL} | - - | 17 - | 100 100 | mV |
| Slew Rate ($V_{in} = 0.5$ to 2.0 V, $V_{CC} = 15$ V, $R_L = 2.0$ k Ω , $A_v = 1.0$, $C_L = 100$ pF) | SR | 0.3 | 0.5 | - | V/ μs |
| Unity Gain Bandwidth ($V_{CC} = 30$ V, $R_L = 2.0$ k Ω , $C_L = 100$ pF, $V_{in} = 0.5$ Vpp @ $f = 70$ kHz) | BW | 0.3 | 0.7 | - | MHz |
| Total Harmonic Distortion ($f = 1.0$ kHz, $A_v = 10$, $R_L = 2.0$ k Ω , $V_{CC} = 30$ V, $V_{out} = 2.0$ Vpp) | THD | - | 0.02 | - | % |

NCP4300A

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|--------------------------|----------|------------------------|--------------|------------------------------|
| Op-Amp 2 (Independent op-amp) ($V_{CC} = 5.0\text{ V}$, $V_{out} = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted) | | | | | |
| Input Offset Voltage $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | V_{IO} | – – | 0.5 – | 2.0 3.0 | mV |
| Input Offset Voltage Temperature Coefficient $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | $\Delta V_{IO}/\Delta T$ | – | 7.0 | – | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | I_{IO} | – – | 2.0 – | 30 30 | nA |
| Input Bias Current $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | I_{IB} | – – | –50 – | –150 –150 | nA |
| Input Common Mode Voltage Range ($V_{CC} = 0\text{ V to } 35\text{ V}$) | V_{ICR} | – | 0 to $V_{CC} - 1.5$ | – | V |
| Large Signal Voltage Gain ($V_{CC} = 15\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $V_{out} = 1.4\text{ V to } 11.4\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | A_{VOL} | 50 25 | 100 – | – – | V/mV |
| Power Supply Rejection ($V_{CC} = 5.0\text{ V to } 30\text{ V}$) | PSRR | 40 | 90 | – | dB |
| Common Mode Rejection ($V_{CM} = 0\text{ V to } 3.5\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | CMRR | 40 30 | 60 – | – – | dB |
| Output Source Current ($V_{CC} = 15\text{ V}$, $V_{out} = 2.0\text{ V}$, $V_{ID} = +1.0\text{ V}$) | I_{O+} | 10 | 16 | – | mA |
| Output Sink Current ($V_{CC} = 15\text{ V}$, $V_{out} = 2.0\text{ V}$, $V_{ID} = -1.0\text{ V}$) | I_{O-} | 10 | 25 | – | mA |
| Output Voltage Swing, High ($V_{CC} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$, $V_{ID} = +1.0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | V_{OH} | 27 27 | 28 – | – – | V |
| Output Voltage Swing, Low ($R_L = 10\text{ k}\Omega$, $V_{ID} = -1.0\text{ V}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | V_{OL} | – – | 17 – | 100 100 | mV |
| Slew Rate ($V_{in} = 0.5\text{ to } 3.0\text{ V}$, $V_{CC} = 15\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $A_v = 1.0$, $C_L = 100\text{ pF}$) | SR | 0.3 | 0.5 | – | V/ μs |
| Unity Gain Bandwidth ($V_{CC} = 30\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{in} = 0.5\text{ V}_{pp}$ @ $f = 70\text{ kHz}$) | BW | 0.3 | 0.7 | – | MHz |
| Total Harmonic Distortion ($f = 1.0\text{ KHz}$, $A_v = 10$, $R_L = 2.0\text{ k}\Omega$, $V_{CC} = 30\text{ V}$, $V_{out} = 2.0\text{ V}_{PP}$) | THD | – | 0.02 | – | % |

Voltage Reference

| | | | | | |
|---|------------------|------------|--------------|------------|---------------|
| Reference Voltage ($I_K = 10\text{ mA}$) $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C to } 105^\circ\text{C}$ | V_{ref} | – 2.574 | 2.60 2.60 | – 2.626 | V |
| Reference Input Voltage Deviation Over Full Temperature Range ($I_K = 10\text{ mA}$, $T_A = 0^\circ\text{C to } 105^\circ\text{C}$) | ΔV_{ref} | – | 5.0 | 22 | mV |
| Minimum Cathode Current for Regulation | $I_{K(min)}$ | – | 55 | 80 | μA |
| Dynamic Impedance $T_A = 25^\circ\text{C}$, $I_K = 1.0\text{ to } 80\text{ mA}$, $f < 1.0\text{ KHz}$ $T_A = 0^\circ\text{C to } 125^\circ\text{C}$, $I_K = 1.0\text{ mA to } 60\text{ mA}$, $f < 1.0\text{ KHz}$ | $ Z_{KA} $ | – – | 0.3 – | 0.5 0.6 | Ω |

NCP4300A

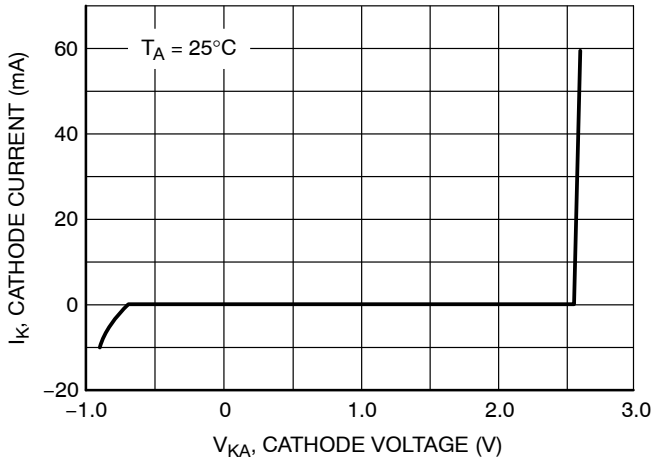


Figure 2. Reference Cathode Current vs. Cathode Voltage

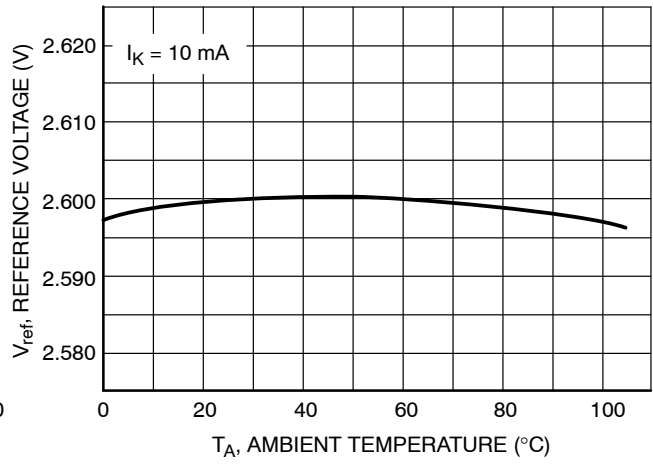


Figure 3. Reference Voltage vs. Ambient Temperature

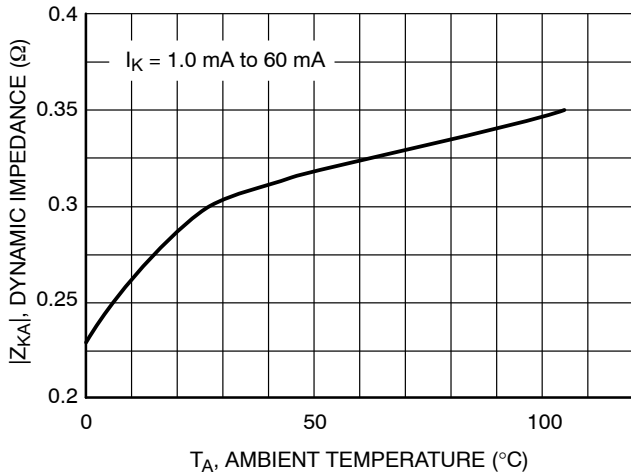


Figure 4. Reference Dynamic Impedance vs. Ambient Temperature

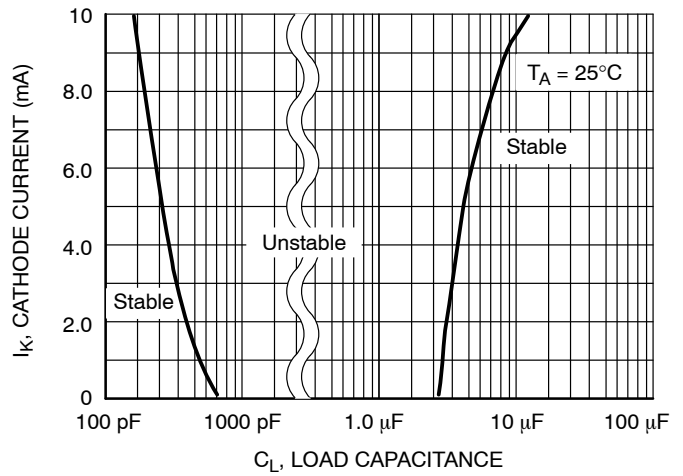


Figure 5. Reference Stability vs. Load Capacitance

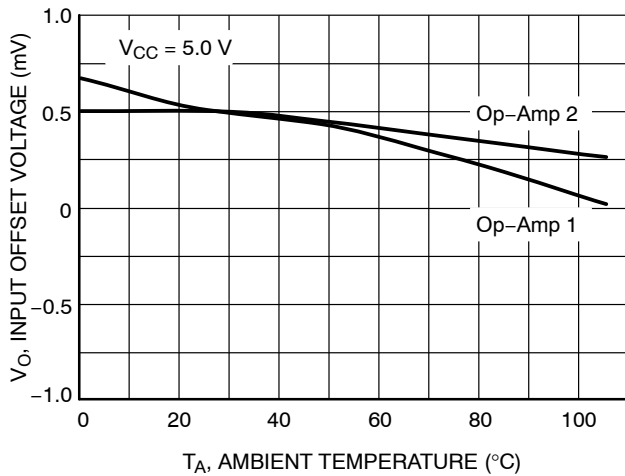


Figure 6. Input Offset Voltage vs. Ambient Temperature

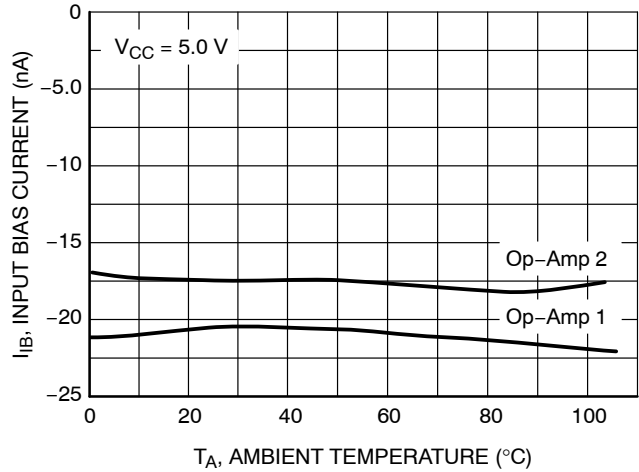


Figure 7. Input Bias Current vs. Ambient Temperature

NCP4300A

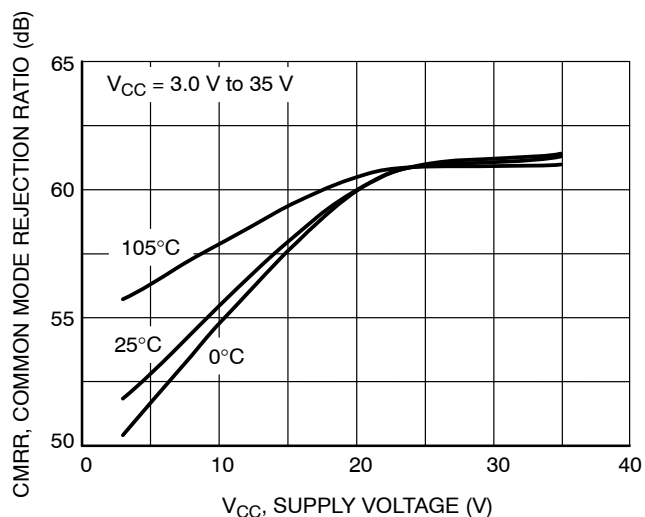


Figure 8. Common Mode Rejection Ratio vs. Supply Voltage

DETAILED OPERATING DESCRIPTION

INTRODUCTION

Power supplies and battery chargers require precise control of output voltage and current in order to prevent catastrophic damage to the system connected. Many present day power sources contain a wide assortment of building blocks and glue devices to perform the required sensing for proper regulation. Typical feedback loop circuits may consist of a voltage and current amplifier, summing circuitry and a reference. The NCP4300A contains all of these basic functions in a manner that is easily adaptable to many of the various power source-load configurations.

OPERATING DESCRIPTION

The NCP4300A is an analog regulation control circuit that is designed to simultaneously close the voltage and current feedback loops in power supply and battery charger applications. This device can control the feedback loop in either constant-voltage (CV) or constant-current (CC) mode with smooth crossover. A concise description of the integrated circuit blocks is given in below. The functional block diagram of the IC is shown in Figure 1.

Internal Reference

An internal precision band gap reference is used to set the 2.6 V voltage threshold and current threshold setting. The

reference is initially trimmed to a $\pm 0.5\%$ tolerance at $T_A = 25^\circ\text{C}$ and is guaranteed to be within $\pm 1.0\%$ over an ambient temperature range of 0°C to 105°C .

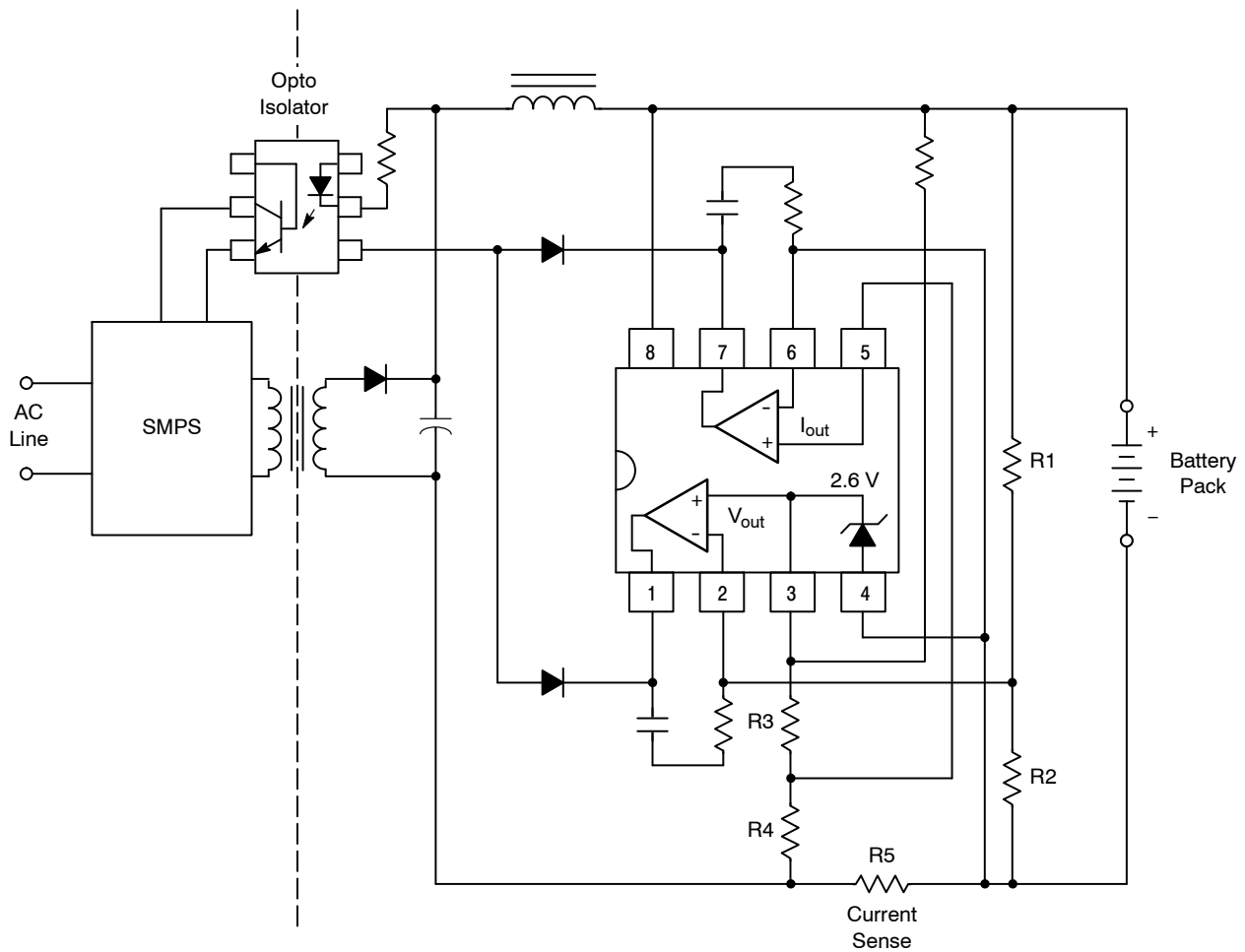
Voltage Sensing Operational Amplifier (Op-Amp 1)

The internal Op-Amp 1 is designed to perform the voltage control function. The non-inverting input of the op-amp is connected to the precision voltage reference internally. The inverting input of the op-amp monitors the voltage information derived from the system output. As the control threshold is internally connected to the voltage reference, the voltage regulation threshold is fixed at 2.6 V. For any output voltage from 2.6 V up to the maximum limit can be configured with an external resistor divider. The output terminal of Op-Amp 1 (pin 1) provides the error signal for output voltage control. The output pin also provides a means for external compensation.

Independent Operational Amplifier (Op-Amp 2)

The internal Op-Amp 2 is configured as a general purpose op-amp with all terminals available for the user. With the low offset voltage provided, 0.5 mV, this op-amp can be used for current sensing in a constant current regulator.

NCP4300A



The above circuit demonstrates the use of the NCP4300A in a constant-current constant-voltage switch mode battery charger application. The charging current level is set by resistors R3, R4, and R5. The reference voltage is divided down by resistors R3 and R4 to create an offset voltage at pin 6. This results in a high state at the op amp output, pin 7. As the battery pack charge current increases, a proportional increasing voltage is developed across R5 that will eventually cancel out the pin 6 offset voltage. This will cause the op amp output to sink current from the opto isolator diode, and control the SMPS block in a constant-current mode. Resistors R1 and R2 divide the battery pack voltage down to the 2.6 V reference level. As the battery pack voltage exceeds the desired programmed level, the voltage at pin 2 will become slightly greater than pin 3. This will cause the op amp output to sink current from the opto isolator diode, and control the SMPS block in a constant-voltage mode. The formulas for programming the output current and voltage are given below.

$$I_{\text{out}} = \frac{V_{\text{ref}}}{\left(\frac{R3}{R4} + 1\right) R5}$$

$$V_{\text{out}} = \left(\frac{R1}{R2} + 1\right) V_{\text{ref}}$$

$$\begin{aligned} \text{With : } R3 &= 30 \text{ k} \\ R4 &= 1.2 \text{ k} \\ R5 &= 0.1 \\ I_{\text{out}} &= 1.0 \text{ A} \end{aligned}$$

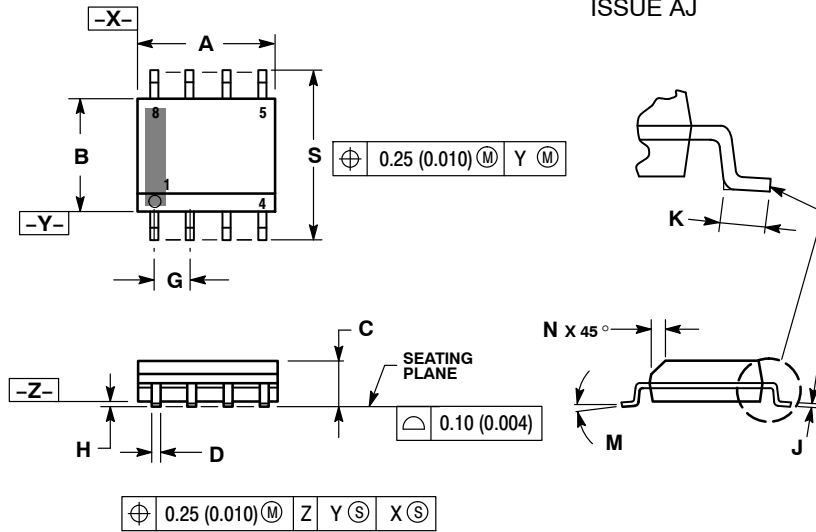
$$\begin{aligned} \text{With : } R1 &= 4.7 \text{ k} \\ R2 &= 3.6 \text{ k} \\ V_{\text{out}} &= 6.0 \text{ V} \end{aligned}$$

Figure 9. Constant-Current Constant-Voltage Switch Mode Battery Charger

NCP4300A

PACKAGE DIMENSIONS

SOIC-8 D SUFFIX CASE 751-07 ISSUE AJ

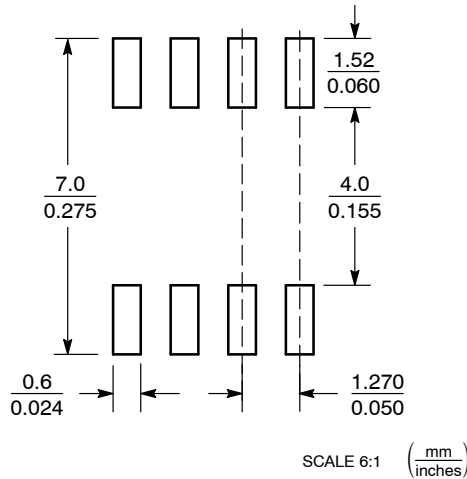


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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