TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIII)

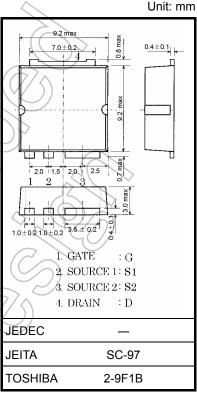
2SK3842

Switching Regulator Applications, DC-DC Converter and Motor Drive Applications

- Low drain-source ON resistance: RDS (ON) =4.6 m Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 93 \text{ S (typ.)}$
- Low leakage current: $I_{DSS} = 100 \mu A \text{ (max) (V}_{DS} = 60 \text{ V)}$
- Enhancement model: $V_{th} = 2.0 \text{ to } 4.0 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 1 \text{ mA})$

Absolute Maximum Ratings (Ta = 25°C)

Character	istics	Symbol	Rating	Unit
Drain-source voltage		V _{DSS}	60	$(\nearrow \land)$
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	60	V
Gate-source voltage		V _{GSS}	±20	y
Drain current	DC (Note 1)	I _D	75	
	Pulse($t \le 1 \text{ ms}$) (Note 1)	I _{DP}	300	Α
Drain power dissipation	on (Tc = 25°C)	PD	125	W
Single pulse avalanch	ne energy (Note 2)	Eas	322	Z Z
Avalanche current		I _{AR})) 75	Α
Repetitive avalanche	energy (Note 3)	EAR	12.5	mJ
Channel temperature		(1ch)	150)°¢
Storage temperature	range	Tstg	-55 to150	/~e>



Weight: 0.74 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	Rth (ch-c)	1.0	°C/W

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: $V_{DD}=25$ V, $T_{ch}=25$ °C (initial), L=78 μH , $R_{G}=25$ Ω , $I_{AR}=75$ A

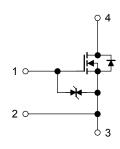
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Please handle with caution.

Circuit Configuration

Notice:

Please use the S1 pin for gate input signal return. Make sure that the main current flows into S2 pin.





Electrical Characteristics (Note 4) (Ta = 25°C)

Char	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage cui	rent	I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±10	μΑ	
Drain cut-OFF cเ	ırrent	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	_	_	100	μΑ	
Drain-source breakdown voltage		V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	60	_	_	V	
		V (BR) DSX	$I_D = 10$ mA, $V_{GS} = -20$ V	35	_	_	V	
Gate threshold ve	oltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0) /_	4.0	V	
Drain-source ON	resistance	R _{DS} (ON)	V _{GS} = 10 V, I _D = 38 A) <u> </u>	4.6	5.8	mΩ	
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 38 A	46	93	_	S	
Input capacitance	e	C _{iss}			12400	_		
Reverse transfer capacitance		C _{rss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	700	_	pF	
Output capacitance		Coss		_	1100	_		
Switching time	Rise time	t _r	V _{GS}	- /	18	<u> </u>		
	Turn-ON time	t _{on}		_((45) –		
	Fall time	t _f	44	77	35	_	ns	
	Turn-OFF time	t _{off}	Duty $\leq 1\%$, $t_W = 10 \mu s$		200	_		
Total gate charge (gate-source plus		Qg) _	196	_		
Gate-source charge		Qgs	$V_{DD} \simeq 48 \text{ V}, V_{GS} \neq 10 \text{ V}, I_D = 75 \text{ A}$	_	148	_	nC	
Gate-drain ("miller") charge		Q _{gd}		_	48	_		

Note 4: Connect the S1 and S2 pins together, and ground them except during switching time measurement.

Source-Drain Ratings and Characteristics (Note 5) (Ta = 25°C)

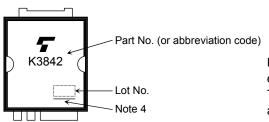
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1, Note 5)	I _{DR} 1	<u> </u>	_	_	75	Α
Pulse drain reverse current (Note 1,Note 5)	I _{DRP} 1	· –	_	_	300	Α
Continuous drain reverse current (Note 1, Note 5)	I _{DR} 2	_	_	_	1	Α
Pulse drain reverse current (Note 1,Note 5)	I _{DRP} 2	_	_	_	4	Α
Forward voltage (diode)	V _{DS2F}	I _{DR} 1 = 75 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 75 A, V _{GS} = 0 V,	_	70	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 50 A/μs	_	77	_	nC

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Note 5: Current flowing between the drain and the S1 pin, when open the S2 pin is left open.

Unless otherwise specified, connect the S1 and S2 pins together, and ground them.

Marking



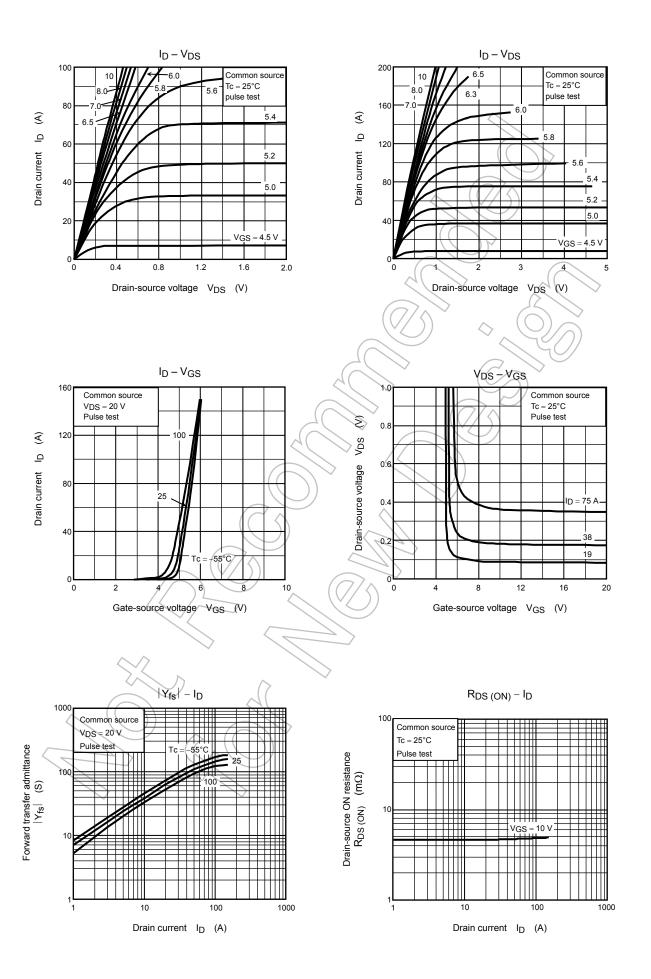
Note 4: A line under a Lot No. identifies the indication of product

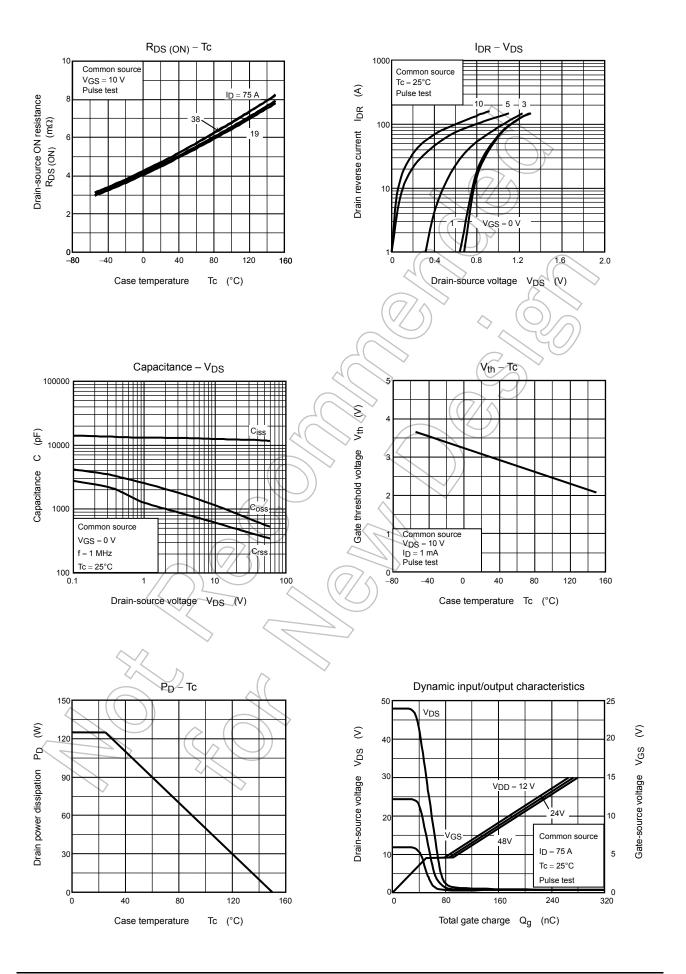
Not underlined: [[Pb]]/INCLUDES > MCV

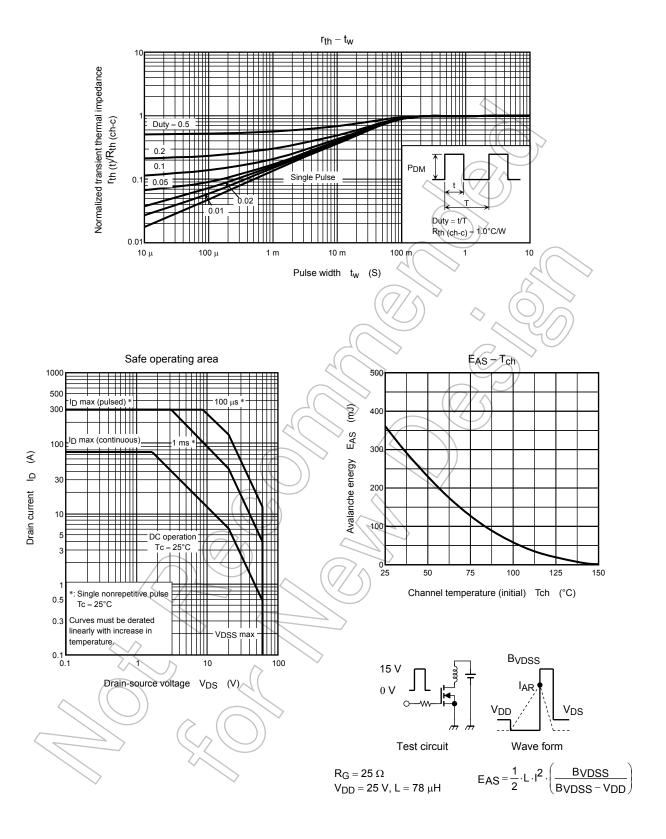
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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2009-09-29







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