TLE 7263E

Integrated HS-CAN, LIN, LDO and HS Switch

System Basis Chip

Automotive Power

Never stop thinking.

Integrated HS-CAN, LIN, LDO and HS Switch System Basis Chip **TLE 7263E**

1 Overview

PG-DSO-36-53

Features

- Two Low Drop Voltage Regulators
- Window watchdog
- Standard 16-bit SPI-interface
- Supports µController Stop Mode
- Sleep Mode (50µA)
- V_{BAT} Monitoring and fail-safe output
- Overtemperature and short circuit protection
- Power on and undervoltage reset generator
- High side switch, 150 mA
- 4 Monitoring / wake-up inputs
- Exposed Pad Package
- AEC Qualified
- Green (RoHS Compliant) product

HS CAN Transceiver

- CAN data transmission rate up to 1 MBaud
- Low power mode management
- Supports sleep and receive-only modes
- Bus wake-up capability via CAN message
- Bus pins are short circuit proof to ground and battery voltage

LIN Transceiver

- Single-wire transceiver
- Transmission rate up to 20 kBaud
- Compatible to LIN specification 1.3, 2.0, 2.1 and SAE J2602-2
- Very low current consumption in Sleep Mode
- Short circuit proof to GND and battery

Type	Package	Marking
TLE 7263E	PG-DSO-36-53	

Dual-Voltage Regulator

- Low-dropout voltage regulator, dual voltage-supply
- V1, 150 mA, 5 V ±2% for external devices, e.g. microcontrollers
- V2, 150 mA, 5 V ±2% for internal CAN module and external devices.

Description

The TLE 7263E is a monolithic integrated circuit in an enhanced power package. The IC is designed for CAN-LIN gateway applications.

To support these applications the TLE 7263E covers smart power functions such as HS-CAN transceiver and LIN transceiver for data transmission, dual low dropout voltage regulator (LDO) for external 5 V supply, and high-side switch as well as a 16-bit SPI (serial peripheral interface) to control and monitor the IC. There is also a window watchdog circuit with a reset feature, a fail-safe output, a voltage sensing input and a undervoltage reset feature implemented.

The device offer low power modes in order to support modules directly connected to the battery (KL. 30). A wake-up from the low power mode is possible via a message on the bus or via the bi level sensitive monitoring/wake-up inputs. The integrated High-Side switch can also be used to periodically supply an external wake-up circuitry in the low power mode, by choosing a special function. The integrated bus transceivers offer a receive-only mode for software diagnosis functions.

The IC is designed to withstand the severe conditions of automotive applications.

2 Pin Configuration

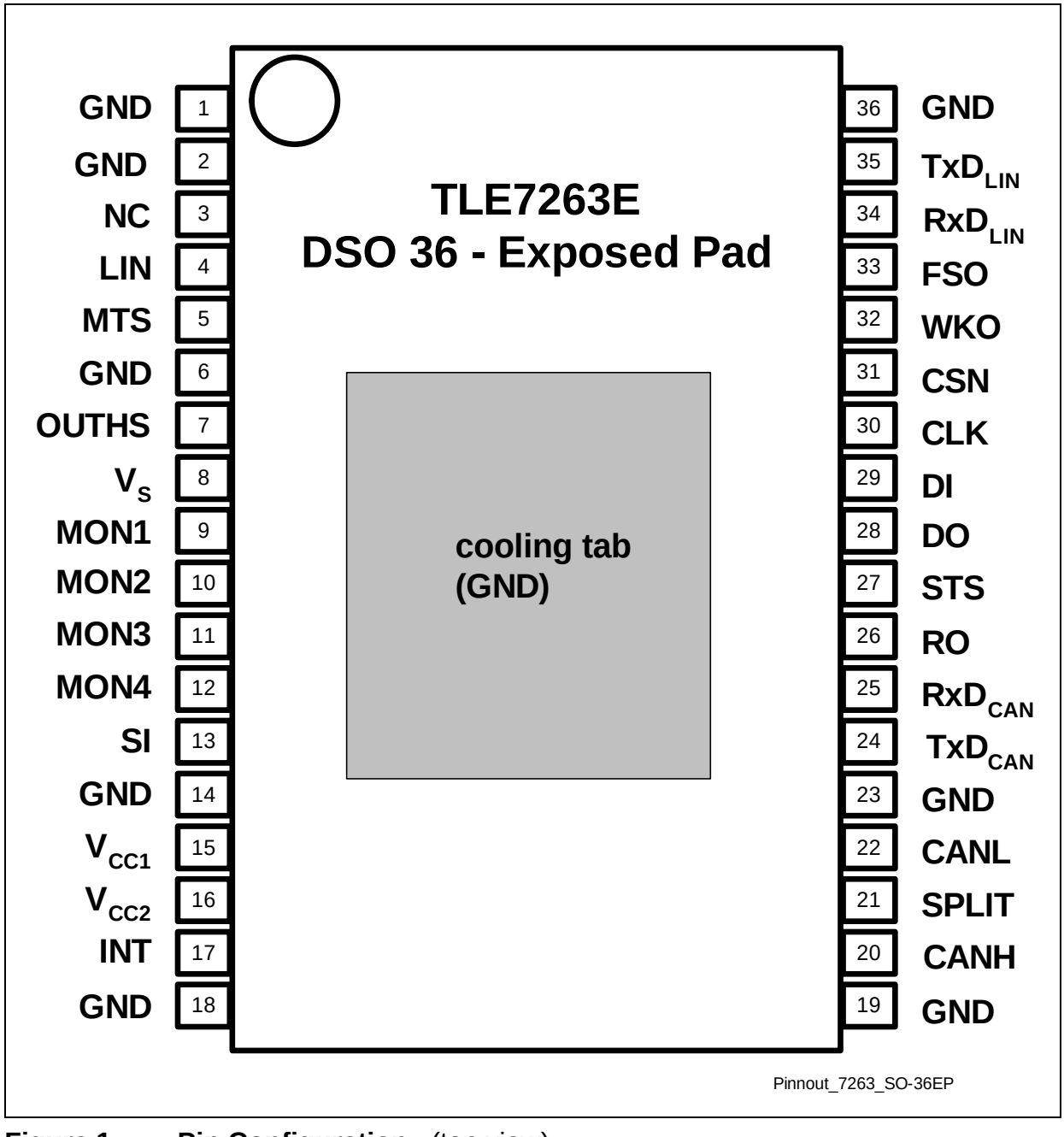

Figure 1 Pin Configuration (top view)

Table 1 Pin Definitions and Functions

Pin	Symbol	Function
9 10 11 12	MON1, MON2, MON3, MON4	**Monitoring / Wake-Up Inputs;** bi level sensitive inputs used to monitor signals coming from, for example, an external switch panel; also used as wake-up input during cyclic sensing in low power modes (MON4 is exempted from “cyclic sense” as this input is permanently active)
8	V_S	**Power Supply Input;** block to GND directly at the IC with ceramic capacitor; (ferrite recommended for better EMC behavior)
15	V_{CC1}	**Voltage Regulator Output (V1);** 5 V supply; to stabilize block to GND with an external capacitor $C_Q \geq 10$ µF, ESR < 6 Ω
16	V_{CC2}	**Voltage Regulator Output (V2);** 5 V supply; to stabilize block to GND with an external capacitor $C_Q \geq 10$ µF, ESR < 6 Ω
32	WKO	**Wake-Up Event Output;** indicates wake up via monitoring inputs, CAN or LIN during Sleep or Stop Mode; active low; wake up sets device to Standby Mode
33	FSO	**Fail Safe Output;** to supervise and control critical applications, high when watchdog is correctly served, low at any reset condition; active low
26	RO	**Reset Output;** open drain output, integrated pull-up, active low
13	SI	**Sense Comparator Input;** for monitoring of external voltages, to program the detection level connect external voltage divider
17	INT	**Interrupt Output;** output to monitor sense comparator input condition; input for enabling the Flash Programming Mode (voltage to be applied > 7 V)
5	MTS	**Master Termination Switch;** output used to turn-on the termination/pull-up resistor of a LIN master
34	RxD_{LIN}	**LIN Transceiver Data Output;** according to the ISO 9141 and LIN specification 1.3 and 2.0; push-pull output; LOW in dominant state
35	TxD_{LIN}	**LIN Transceiver Data Input;** according to ISO 9141 and LIN specification 1.3 and 2.0

Table 1 Pin Definitions and Functions (cont'd)

Pin	Symbol	Function
4	LIN	**LIN Bus;** Bus Line for the LIN interface, according to ISO 9141 and LIN specification 1.3 and 2.0
29	DI_{SPI}	**SPI Data Input;** receives serial data from the control device; serial data transmitted to DI is a 16-bit control word with the Least Significant Bit (LSB) transferred first: the input has a pull-down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal
28	DO_{SPI}	**SPI Data Output;** this tri-state output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN)
30	CLK_{SPI}	**SPI Clock Input;** clock input for shift register; CLK has an internal pull-down and requires CMOS logic level inputs
31	CSN_{SPI}	**SPI Chip Select Not Input;** CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal pull-up and requires CMOS logic level inputs
7	OUTHS	**High Side Switch Output;** controlled via SPI, in SBC Sleep Mode controlled by internal cyclic sense function when selected
24	TxD_{CAN}	**CAN Transmit Data Input;** integrated pull-up
25	RxD_{CAN}	**CAN Receive Data Output**
21	SPLIT	**CAN Termination Output;** to support the recessive voltage level of the bus lines
20	CANH	**CAN High Line Output**
22	CANL	**CAN Low Line Input**
27	STS	**Send-to-Sleep;** to switch the SBC back into low current mode during cyclic wake
1, 2, 6,14, 18,19, 23,36	GND	**Ground**
3	NC	**Not Connected Internally;** leave open or connect to GND
EP	EP	**Exposed Pad;** internally connected to GND; connect to GND on board

3 Block Diagram

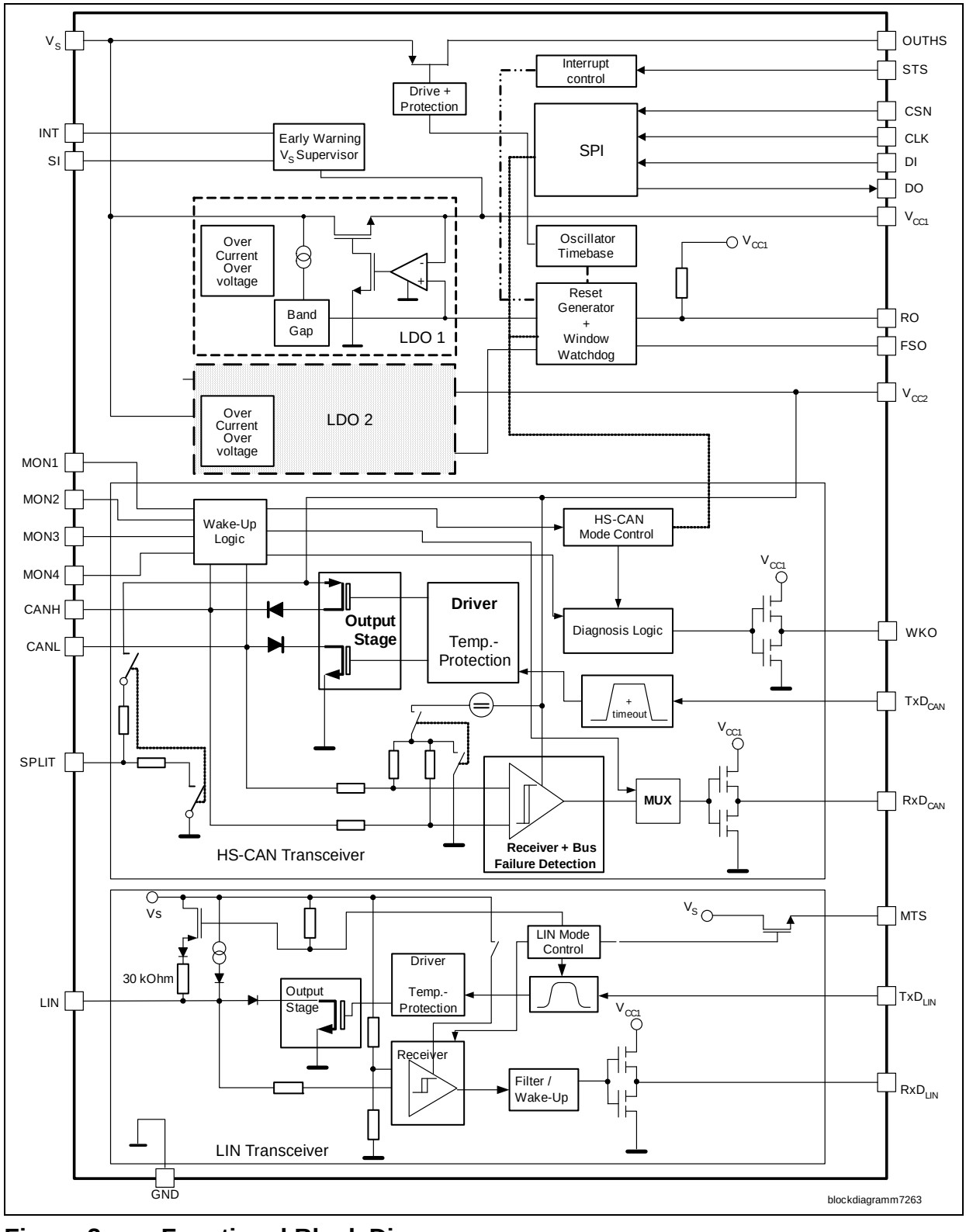

Figure 2 Functional Block Diagram

4 Features

The TLE 7263E incorporates a lot of features, that are listed in **Table 2** below. A short description of the features is given in **“Operation Modes” on Page 9**.

Table 2 Truth Table of the TLE 7263E

Feature	SBC Active Mode	SBC Standby Mode	SBC Stop Mode	SBC Sleep Mode	CAN RxD-only Mode
V_{CC}, V1, 5 V	ON	ON	ON	OFF	ON
V_{CC}, V2, 5 V	ON	ON/OFF	ON/OFF	OFF[1)]	ON
Reset RO	ON	ON	ON	OFF	ON
Window Watchdog	ON	ON	ON/OFF	OFF/[ON]	ON
Fail Safe Output	ON	ON	ON	OFF	ON
Sense input	ON	ON	ON	OFF	ON
Monitoring pins	ON	ON	ON	ON	ON
HS-switch	ON	ON	ON	OFF	ON
HS-cyclic-sense	OFF	OFF	ON	ON	OFF
16-bit SPI	ON	ON	ON	OFF	ON
CAN/LIN wake-up via bus message	OFF/“Sleep”	ON	ON	ON	OFF
CAN Transmit	ON/“Sleep”	OFF	OFF	OFF	OFF
CAN Receive	ON/“Sleep”	OFF	OFF	OFF	ON
LIN Transmit	ON/“Sleep”	OFF	OFF	OFF	ON
LIN Receive	ON/“Sleep”	OFF	OFF	OFF	ON
RxD_{LIN}	L/H	active low wake-up interrupt	active low wake-up interrupt	low	L/H
RxD_{CAN}	L/H	active low wake-up interrupt	active low wake-up interrupt	low	L/H
INT output	active low early warning	active low early warning	active low early warning	low	active low early warning
WKO output	OFF	active low wake-up	active low wake-up	low	OFF

1) In Sleep Mode the Vcc2 should be switched off. This is the default setting at the SPI

4.1 Operation Modes

This System Basis Chip (SBC) offers five main operation modes that are controlled via three mode select bits MS1, MS2 and MS3 within the SPI: SBC Active, Standby, Sleep and Stop mode, as well as CAN Receive-Only mode. After powering-up the SBC, it starts-up in **SBC Standby Mode**, waiting for the microcontroller to finish its startup and initialization sequences. From this transition mode the SBC can be switched via SPI command into the desired operating mode (The device should not be switched directly from Standby Mode to Sleep or Stop Mode). All modes are selected via SPI bits or certain operation conditions, e.g. external wake-up events.

The **SBC Active Mode**, that is used in order to transmit and receive CAN and LIN messages, supports two additional sub-modes, “CAN Sleep” and “LIN Sleep”. During these sub-modes the SBC remains its voltage regulators running in order to supply external devices. Also, the line termination of the “sleeping” bus transceiver is turned-off respectively.

During **SBC Sleep Mode**, the lowest power consumption is achieved, by having its main voltage regulator switched-off. As the microcontroller can not be supplied, the integrated window watchdog might be disabled in Sleep Mode via SPI bit. However, it can be turned-on for periodically waking-up the system, e.g. ECU, by generating a reset.

In case an external microcontroller needs to be supplied with its quiescent current, the **SBC Stop Mode** can be chosen. In this mode the main voltage regulator remains active. Optionally, the second voltage regulator can be turned-on or off via the SPI prior to entering one of the respective power saving modes. The integrated window watchdog remains active until the microcontroller enters its power saving mode (“Stop Mode”). This power saving mode is assumed to be reached once the current consumption is below a certain threshold (see **Watchdog current threshold**, **Table** and **“Window Watchdog, Reset” on Page 26**).

In both low power modes the internal bus transceivers, including the line termination, are turned off while the wake-up capabilities via bus message or monitoring pins are still active. The SBC offers Sleep and Stop Mode in conjunction **with** or **without** the Cyclic Sense/Wake feature. If the Cyclic Sense/Wake feature is selected, two possible states can be entered during Sleep/Stop Mode: **HS-On** and **HS-Off** (see text and respective state diagram).

The **Cyclic Sense** feature can be used to supply an external wake-up circuitry periodically, and is entered upon activation via SPI command. In cyclic sense HS-On state, the High-Side switch is activated for a certain “on-time” and provides supply voltage at its OUTHS pin. Within this on-time the SBC starts sampling of the monitoring/wake-up lines. On-time as well as time period are programmable via the SPI control word. A wake-up at the monitoring / wake-up pins during the on-time as well as a message at the CAN or LIN bus lines automatically sets the TLE 7263E into SBC Standby mode, and turns-on the main voltage regulator V_{CC1}. The digital RxD_{CAN}/RxD_{LIN} lines, that are monitored by the microcontroller during power saving, are pulled low with

respect to the wake-up source (CAN or LIN). Furthermore, the wake-up source is indicated within the SPI status word. Additionally, the wake-up capabilities of the monitoring / wake-up pins can be configured via SPI.

If **Cyclic Wake** is entered upon SPI command, the High-Side switch is turned-on immediately (HS-On state), providing supply voltage at the OUTHS pin. Once the HS-On state is entered, a transition to the HS-Off state can be triggered by a pulse with a minimum width at the STS pin (see **STS pulse width**, **Table**). The microcontroller fully controls the signal level at the STS pin, and this way determines the duration of the HS-On state. As of now the HS-Off state is automatically terminated according to the Cyclic Wake period selected via SPI, or by a CAN or LIN message.

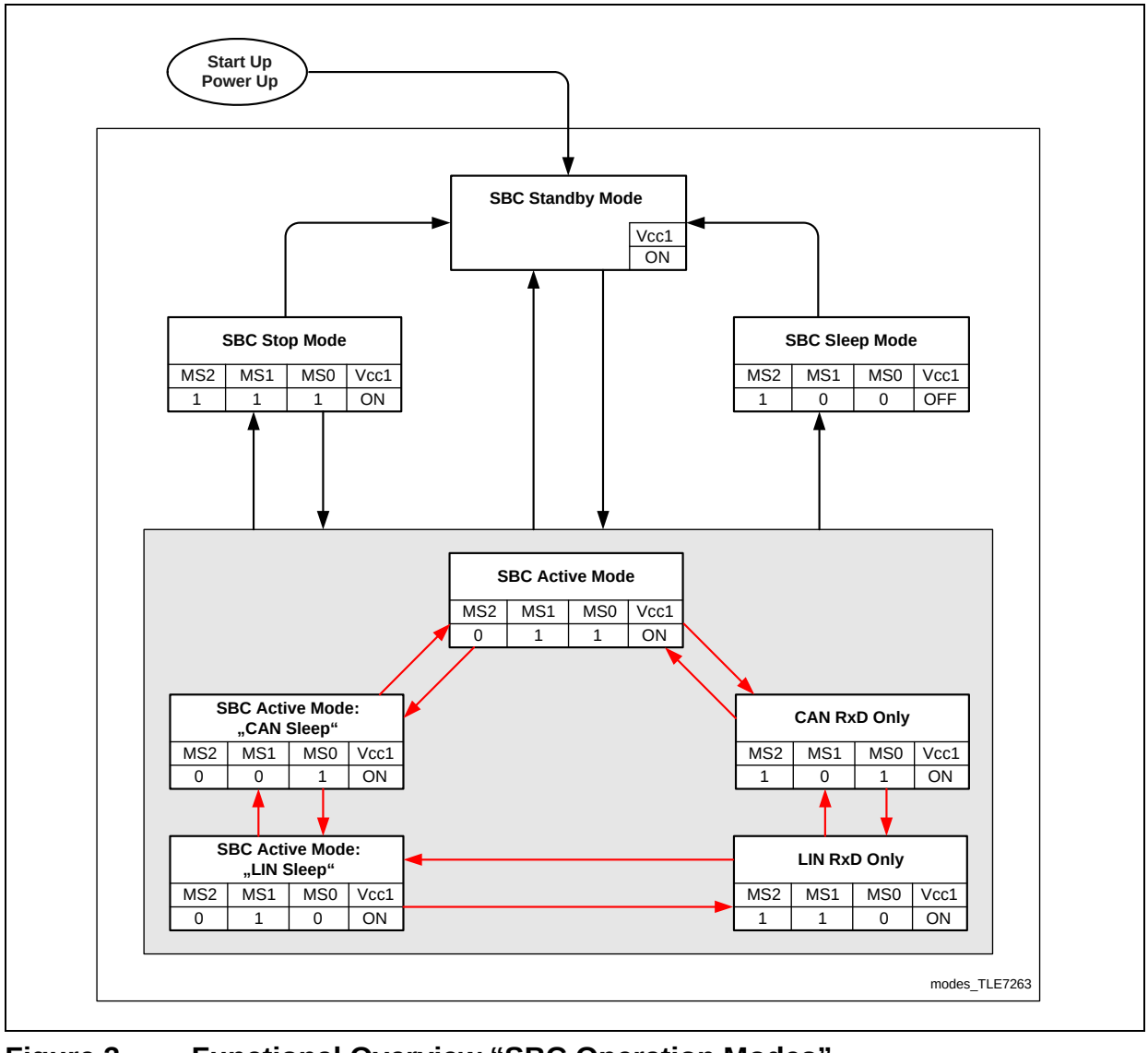

Figure 3 Functional Overview “SBC Operation Modes”

4.2 SBC Sleep Mode without Cyclic Sense

In order to reduce the current consumption to a minimum, the SBC offers a Sleep Mode without Cyclic Sense (see **Figure 4**). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, main voltage regulator as well as the High-Side switch. Upon a voltage level change at the monitoring/wake-up pins or by a CAN or LIN message the SBC Sleep Mode will be terminated and the SBC Standby Mode will automatically be entered.

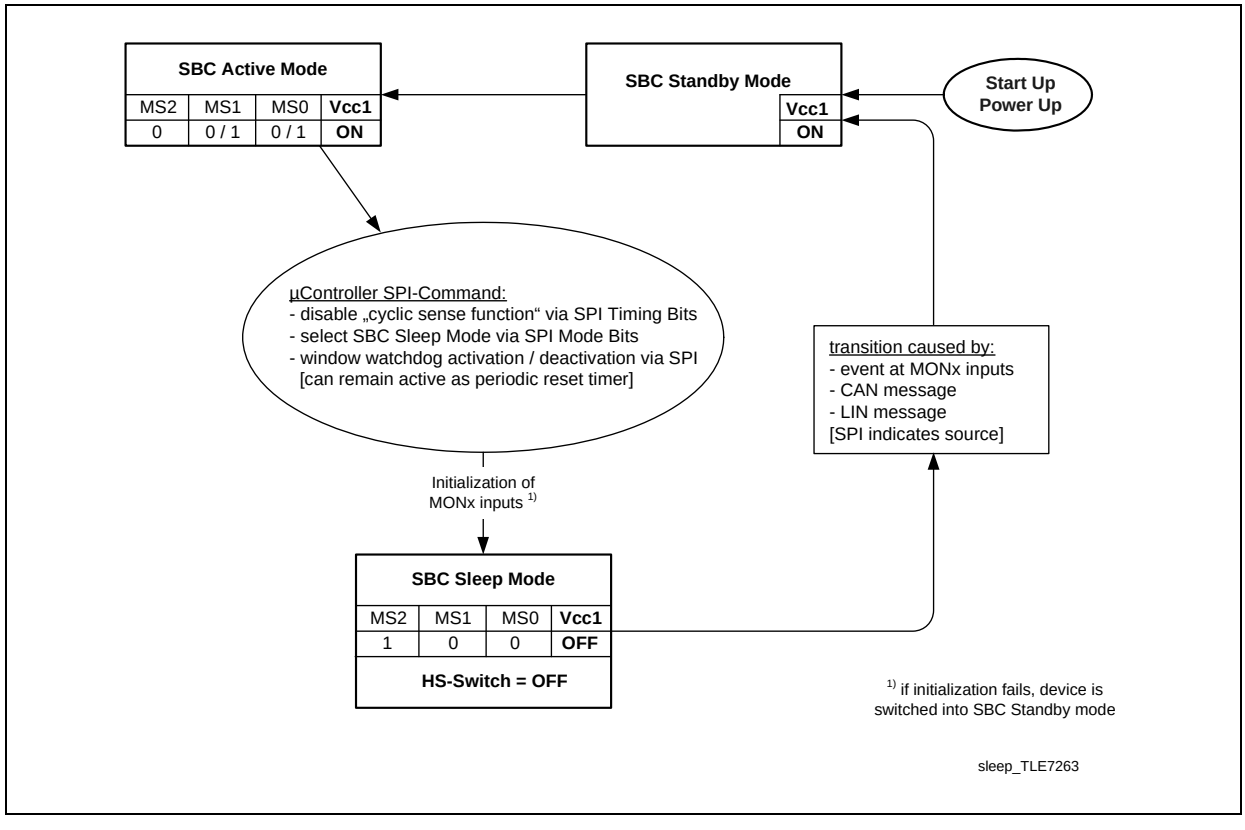

Figure 4 State Diagram “SBC Sleep Mode without Cyclic Sense”

Note: To switch into Low Power Mode from Standby Mode the device should be switched into Normal Mode first. This is required to reset the CAN and LIN transceiver to ensure correct wakeup as well as to ensure the correct function of the RO pin when going to Sleep Mode. The time the device is in Normal Mode before going to Low Power Mode should be long enough that the Vcc2 is up. This can be released by a wait time or by reading the status of Vcc2 via SPI (bit13).

4.3 SBC Sleep Mode with Cyclic Sense

In order to reduce the current consumption to a minimum, but still supply a wake-up circuit periodically, the SBC offers a Sleep Mode with Cyclic Sense (see **Figure 5**). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, as well as the main voltage regulator. The High-Side switch is turned-on according to the SPI timings setting for cyclic sense, as there is the cyclic sense period and the on-time. Upon a voltage level change at the monitoring/wake-up pins or by a CAN or LIN message the SBC Sleep Mode will be terminated and the SBC Standby Mode will automatically be entered. The respective RxD pin of the transceiver that generated the wake-up will be pulled low.

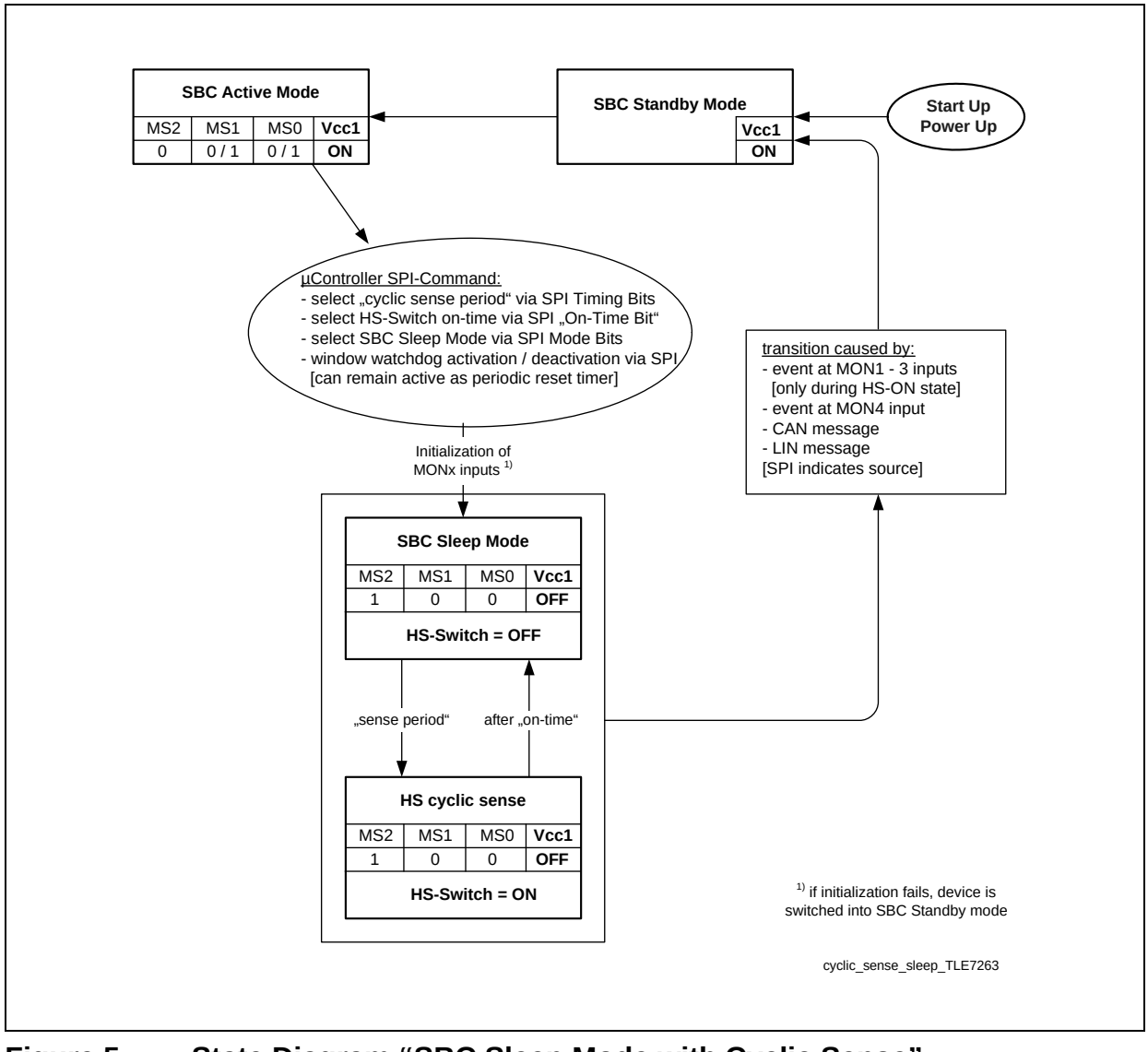

Figure 5 State Diagram “SBC Sleep Mode with Cyclic Sense”

4.4 SBC Sleep Mode with Cyclic Wake

The SBC Sleep Mode has the advantage of reducing the current consumption to a minimum. During this mode the integrated voltage regulator for external supply is turned off. In case the connected microcontroller needs to get activated periodically, the Cyclic Wake feature in combination with the SBC Sleep Mode can be activated (see **Figure 6**).

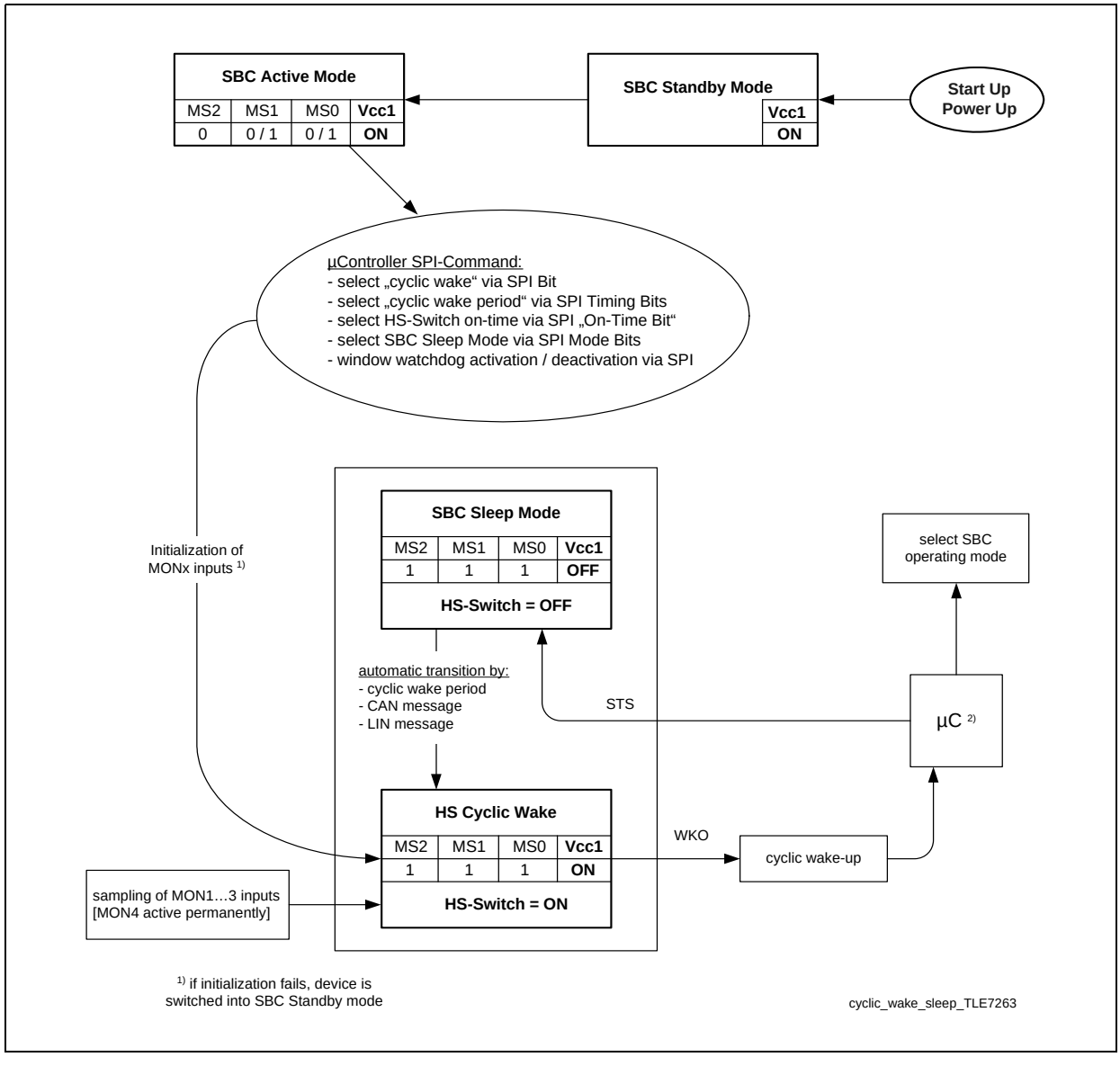

Figure 6 State Diagram “SBC Sleep Mode with Cyclic Wake”

4.5 SBC Stop Mode without Cyclic Sense

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the main voltage regulator remains active.

A voltage level change at the monitoring / wake-up pins will, in contrast to the behavior in Sleep Mode, generate a pulse at the WKO pin that is monitored by the microcontroller, e.g. at an external interrupt input. In case the wake-up event was a CAN or LIN message, the respective RxD pin will be pulled low. (The microcontroller itself has to take care of switching SBC modes after a wake-up event notification (see **Figure 7**).)

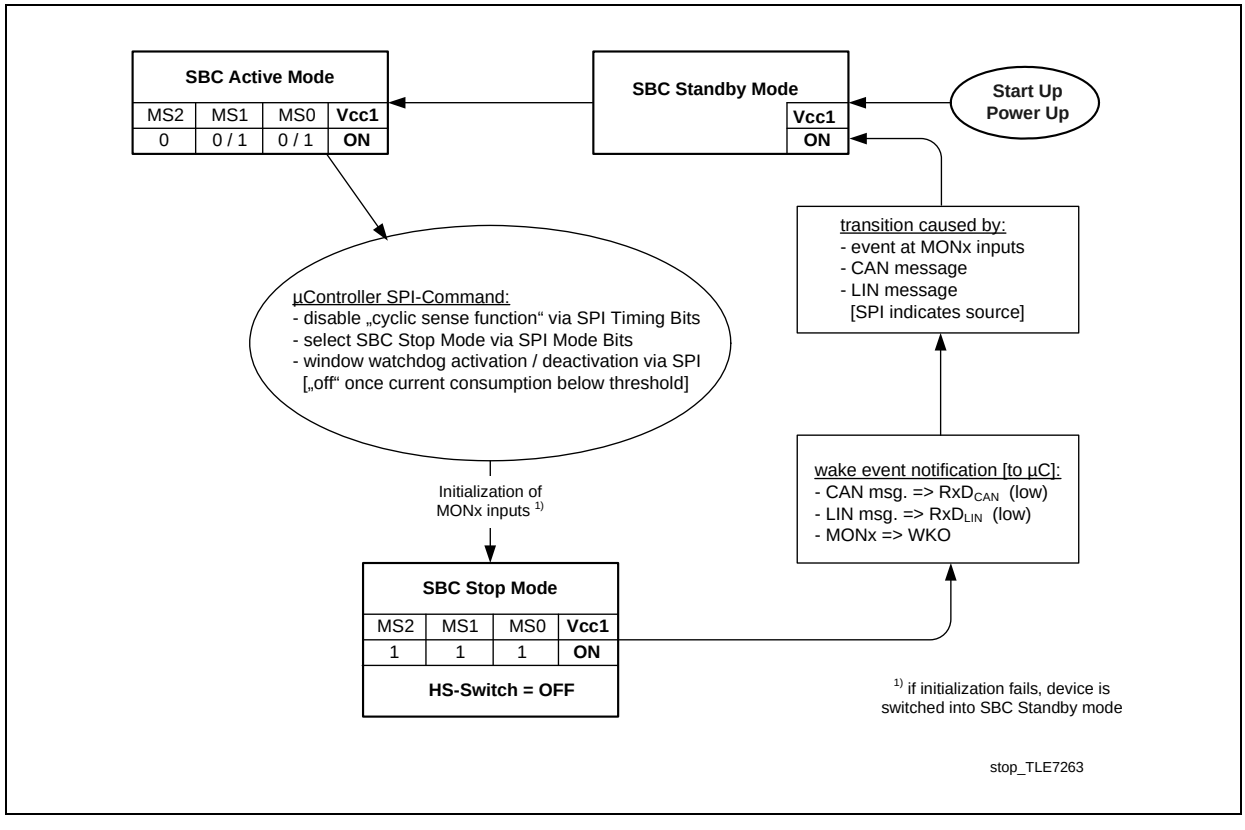

Figure 7 State Diagram “SBC Stop Mode without Cyclic Sense”

4.6 SBC Stop Mode with Cyclic Sense

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the main voltage regulator remains active. The High-Side switch is turned-on according to the SPI timings setting for cyclic sense, as there is the cyclic sense period and the on-time. A voltage level change at the monitoring/wake-up pins will, in contrast to the behavior in Sleep Mode, generate a pulse at the WKO pin that is monitored by the microcontroller, e.g. at an external interrupt input. In case the wake-up event was a CAN or LIN message, the respective RxD pin will be pulled low. (The microcontroller itself has to take care of switching SBC modes after a wake-up event notification (see **Figure 8**).)

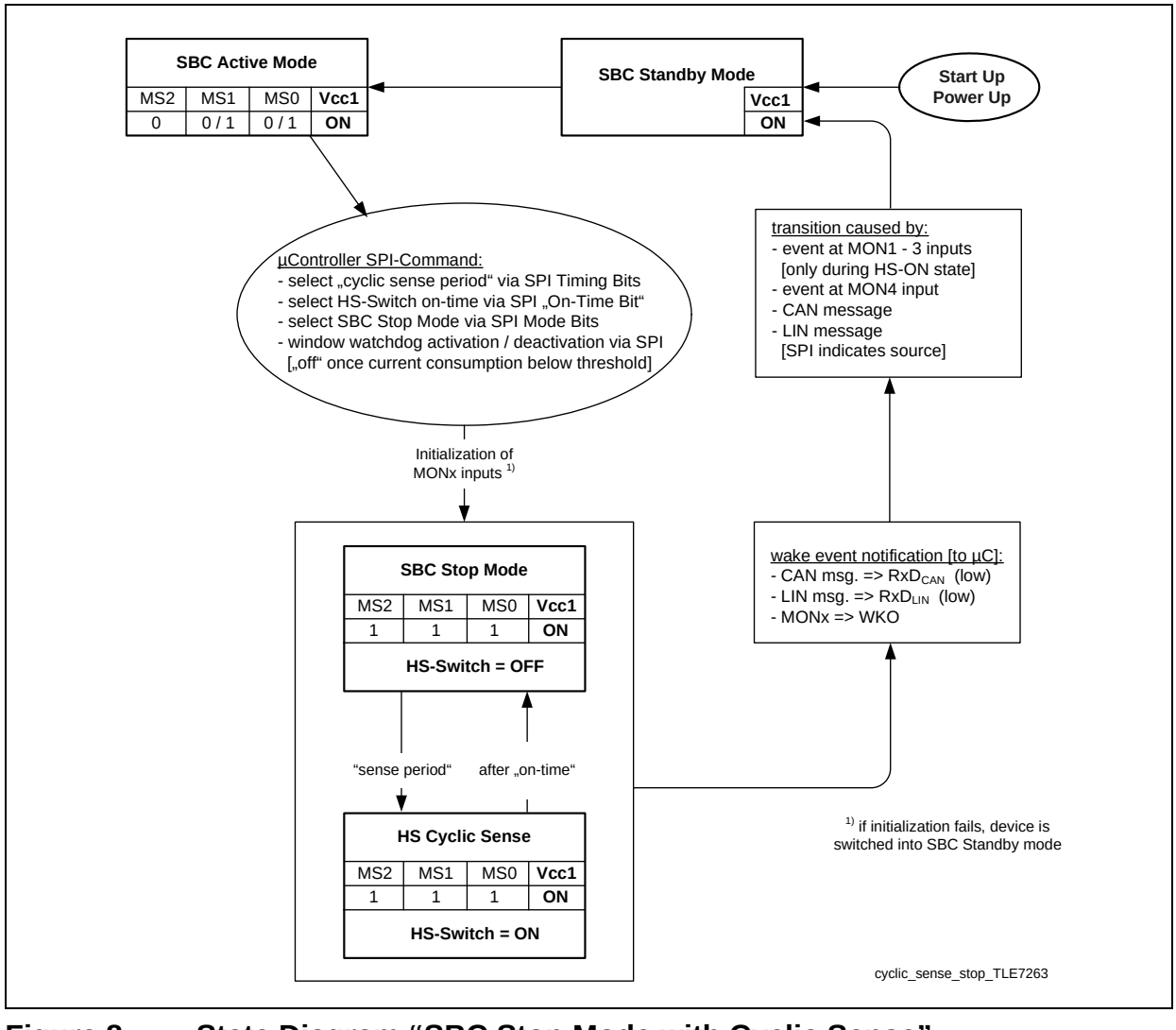

Figure 8 State Diagram “SBC Stop Mode with Cyclic Sense”

4.7 SBC Stop Mode with Cyclic Wake

The SBC Stop Mode has the advantage of reducing the current consumption to a minimum, while supplying the microcontroller with its quiescent current during its power saving mode (“Stop”). This mode is entered via SPI command, and turns-off the integrated bus transceivers and respective termination, but the main voltage regulator remains active. In contrast to Cyclic Sense the HS-On state is entered once Cyclic Wake is selected, immediately providing supply voltage at the OUTHS pin. The microcontroller determines the duration of the HS-On state via the STS input pin (see **Figure 9**). Further transitions from that HS-Off into the HS-On state are done by the selected cyclic wake period or by a bus message. The microcontroller is notified by the WKO (Wake-Up Output) that the HS-On state has been entered. Further notification is done in the same way as for Cyclic Sense in Stop Mode.

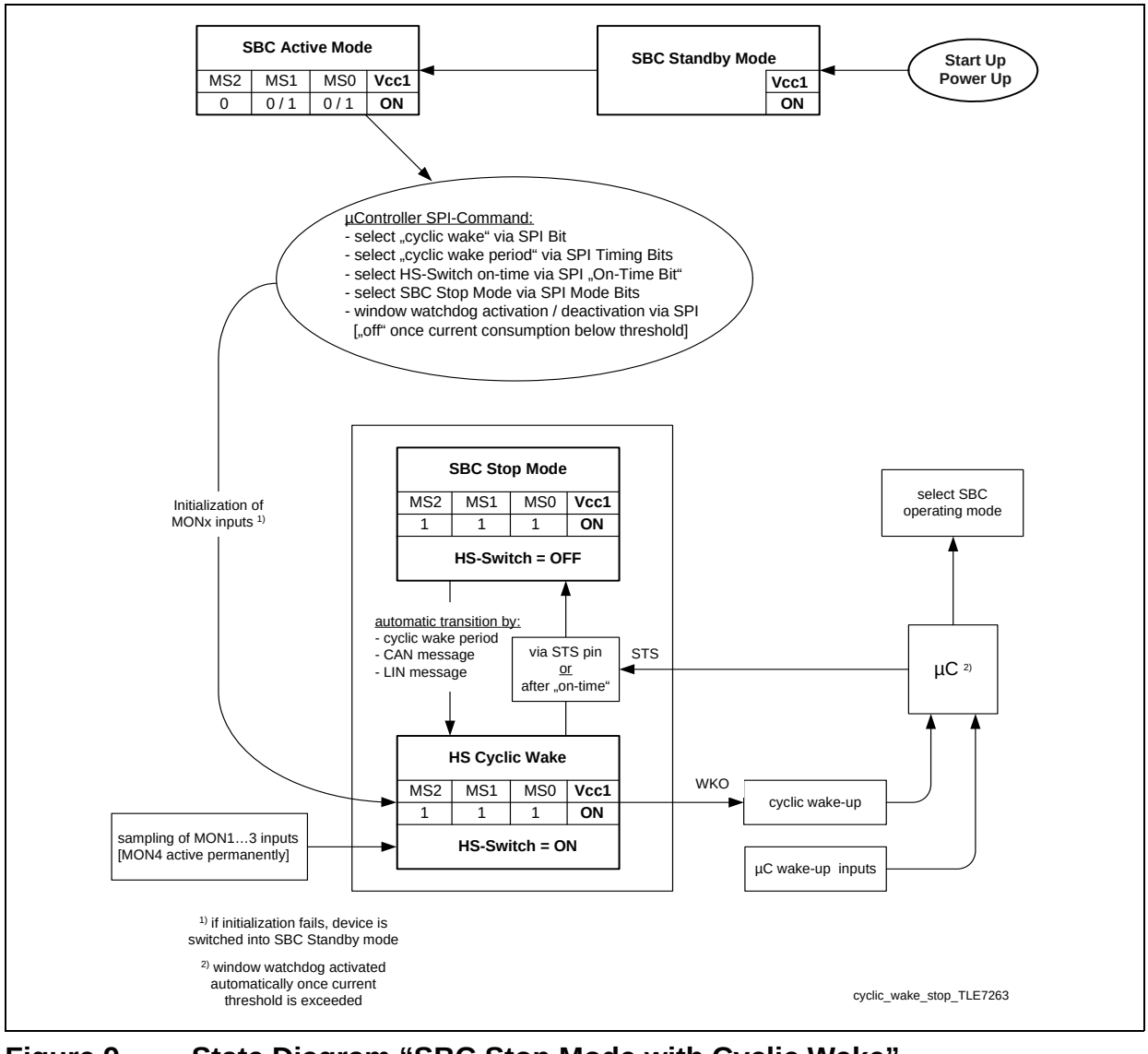

Figure 9 State Diagram “SBC Stop Mode with Cyclic Wake”

Continuous Timer Mode (CTM) for “Cyclic Wake Timer”

Upon start of the “cyclic wake timer” in Cyclic Wake Mode the operating mode might be changed to “SBC Active Mode” by the microcontroller, e.g. in order to transmit data via the CAN or LIN transceiver. In this case the timer continues running with the selected period started in Cyclic Wake Mode. This behavior guarantees the periodic generation of a wake-up signal at the WKO pin, even in case of a mode switch. However, this provides that the time spent in SBC Active Mode is not exceeding the selected period.

Should a time-out (end of selected period) occur in SBC Active Mode before the Cyclic Wake Mode is re-entered, the SBC will generate an interrupt signal at its WKO pin if the CTM feature is enabled via the respective SPI bit (see **Figure 11**).

When the CTM feature is set in the SPI, a wake-up event at the CAN bus in “SBC Active CAN Sleep” mode or at the LIN bus in the “SBC Active LIN Sleep” mode results in switching WKO “low” in addition to switching the RxD to “low”.

4.8 Dual Low Dropout Voltage Regulator

The dual low dropout voltage regulator integrated in the TLE 7263E is able to drive external as well as internal loads, e.g. CAN-circuit supplied via V_{CC2}, even in case of a bus short circuit. Its output voltage tolerance is better than ±2%. The maximum output current for external loads is limited to 150 mA (V_{CC1}), e.g. for microcontroller supply, and 150 mA (V_{CC2}) for internal CAN module and, e.g. for external sensor supply. The two voltage regulator outputs are protected against overload and overtemperature. The thermal pre-warning flag might be used by the microcontroller to reduce the power dissipation of the TLE 7263E by switching off functions of minor priority until the temperature threshold of the thermal shutdown is reached.

An external reverse current protection is required at the pin V_S to prevent the output capacitor from being discharged by negative transients or low input voltage.

A capacitor of 10 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting power down conditions in case of negative transients on the supply line. Stability of the output voltage is guaranteed for output capacitors $C_Q \geq 100$ nF, nevertheless it is recommended to use capacitors $C_Q \geq 10$ µF to buffer the output voltage and therefore improve the reset behavior at input voltage transients.

4.9 CAN Transceiver

The TLE 7263E is optimized for high speed data transmission up to 1 MBaud in automotive applications and is compatible to the ISO 11898 standard. It works as an interface between the CAN protocol controller and the physical bus lines.

This HS-CAN module also supports extended bus error detection via a general error flag as well as individual notification flags, e.g. temperature shutdown and TxD time-out flag, within the SPI.

To reduce EMI the dynamic slopes of the CANL and CANH signals both are limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus.

Furthermore there is implemented a time-out feature to prevent the bus from being blocked by a permanently dominant TxD input signal. Both, the CANL and CANH output stage are automatically disabled after the delay time t_{TxD}.

In order to protect the transceiver output stages from being damaged by shorts on the bus lines, current limiting circuits are integrated. The CANL and CANH output stage respectively are protected by an additional temperature sensor, that disables them as soon as the junction temperature exceeds the maximum value. During the temperature shut-down condition of the CAN output stages receiving messages from the bus lines is still possible.

Wake-Up Indication: A bus wake-up via a CAN message (minimum dominant time $t > t_{WU}$) from low power mode sets the RxD pin and the WKO pin to low. In addition, the V_{cc2}, which supplies the CAN output stage is switched ON.The CAN transceiver has to be enabled to reset the wake-up capability after a bus wake event and after power-up.

Bus Failure Flag: signalizes a bus line short circuit condition to GND, V_S or V_{CCx} via SPI bit 11 in the SPI Output Data “CAN Bus Failure”.

Remarks: Flag is set after four consecutive recessive to dominant cycles on pin TxD when trying to drive the bus dominant. The bus failure flag is cleared upon 4 recessive to dominant edges at TxD without failure condition.

Local Failure Flag: signalizes the local failure conditions listed in the text below via SPI bit 10 in the SPI Output Data “CAN Local Failure”.

Remark: Flag is cleared upon dominant level at RxD while TxD is recessive.

General: release of the transmitter stage only after transition into CAN RxD Only mode and transition back into SBC Active Mode.

TxD Dominant Failure Detection

At permanent dominant signal for $t > t_{TxD}$ at TxD the local failure flag is set and the transmitter stage is turned off.

Remarks: none

RxD Permanent Recessive Clamping

Internal RxD signal does not match signal at RxD pin because the RxD pin is pulled to HIGH (permanent HIGH). This results in setting the local failure flag and disabling of the receiver stage

Remark: the flag is cleared when RxD signal gets dominant.

TxD to RxD Short Circuit

Caused by a short circuit between RxD and TxD. The local failure flag is set and the transmitter stage is disabled.

Remark: the flag is cleared once the short circuit condition is removed.

Bus Dominant Clamping

At a permanent dominant signal at the CAN bus for $t > t_{BUS}$ the local failure flag is set.

Remark: none

Over Temperature Detection

Once the maximum junction temperature at the driving stages exceeded, the local failure flag is set and the transmitter stage is disabled.

Remark: the flag is cleared once RxD gets dominant. Bus only released after the next dominant bit in TxD.

Split Circuit

The split circuitry is activated during SBC Active and RxD Only Mode and deactivated (SPLIT pin high omic) during SBC Sleep, Stop and Standby Mode. The SPLIT pin is used to stabilize the recessive common mode signal in SBC Active Mode and RxD Only mode. This is realized with a stabilized voltage of 0.5 V_{CC2} at the SPLIT pin.

A correct application of the SPLIT pin is shown in **Figure 10**. The split termination for the left and right node is realized with two 60 Ohm resistances and one 10nF capacitor. The center node in this example is a stub node and the recommended value for the split resistances is 1.5 kOhm.

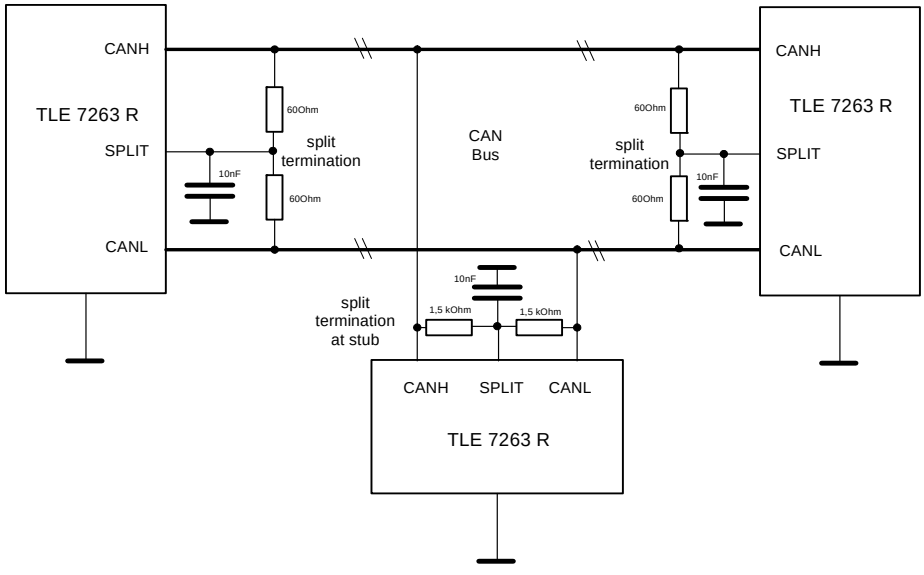

Figure 10 Application of the SPLIT pin for normal nodes and one stub node

4.10 LIN Transceiver

The TLE 7263E offers a transceiver, which is compatible to ISO 9141 and LIN specification 2.0. For fail safe reasons the transceiver already has a pull-up resistor of 30 kΩ implemented. In order to achieve the required timing for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is required, when the LIN node is used as a master. This termination resistor will automatically be turned off via the “Master Termination Switch” pin (MTS) once the LIN module enters LIN Sleep Mode or when the SBC enters Sleep Mode. The transceiver is protected against short to battery and short to GND.

For LIN automotive applications in the United States a dedicated mode by the name “Low Slope Mode” can be used. This mode limits the maximum data transmission rate to 10.4 kBaud by switching to a different slew rate. Operating with the default slew rate at up to 20 kBaud may cause interferences with the AM radio band.

A bus wake-up via a LIN message (minimum dominant time $t > t_{wake}$) from low power mode sets the RxD pin and the WKO pin to low. in addition the MTS is switched ON. The LIN transceiver has to be enabled to reset the wake-up capability after a bus wake event and after power-up.

In case of a “TxD dominant time out failure” or a “transmitter thermal shutdown” the SPI bit 9 is set. After a SPI read-out this bit will be reset unless one of the failure conditions is still present.

Note: In case of a short to GND on the LIN bus a RxD dominant signal is generated by the SBC. In the case that RxD is dominant the device can not go into low power mode from normal mode.

4.11 SPI (Serial Peripheral Interface)

The 16-bit wide Programming or Input Word (see **Table 3**) is read in via the data input DI, which is synchronized with the clock input CLK supplied by the µC. The Diagnosis or Output Word appears synchronously at the data output DO (see **Figure 10**).

The transmission cycle begins when the chip is selected by the Chip Select Not input CSN (“low” active). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus for other usage.

The state of DI is shifted into the input register with every falling edge on CLK. The state of DO is shifted out of the output register after every rising edge on CLK. The number of received input clocks is supervised by a modulo-16 operation and the Input / Control Word is discarded in case of a mismatch. This error is flagged by the WKO set to “low” and in the following SPI output by a “high” at the data output (DO pin) before the first rising edge of the clock is received.

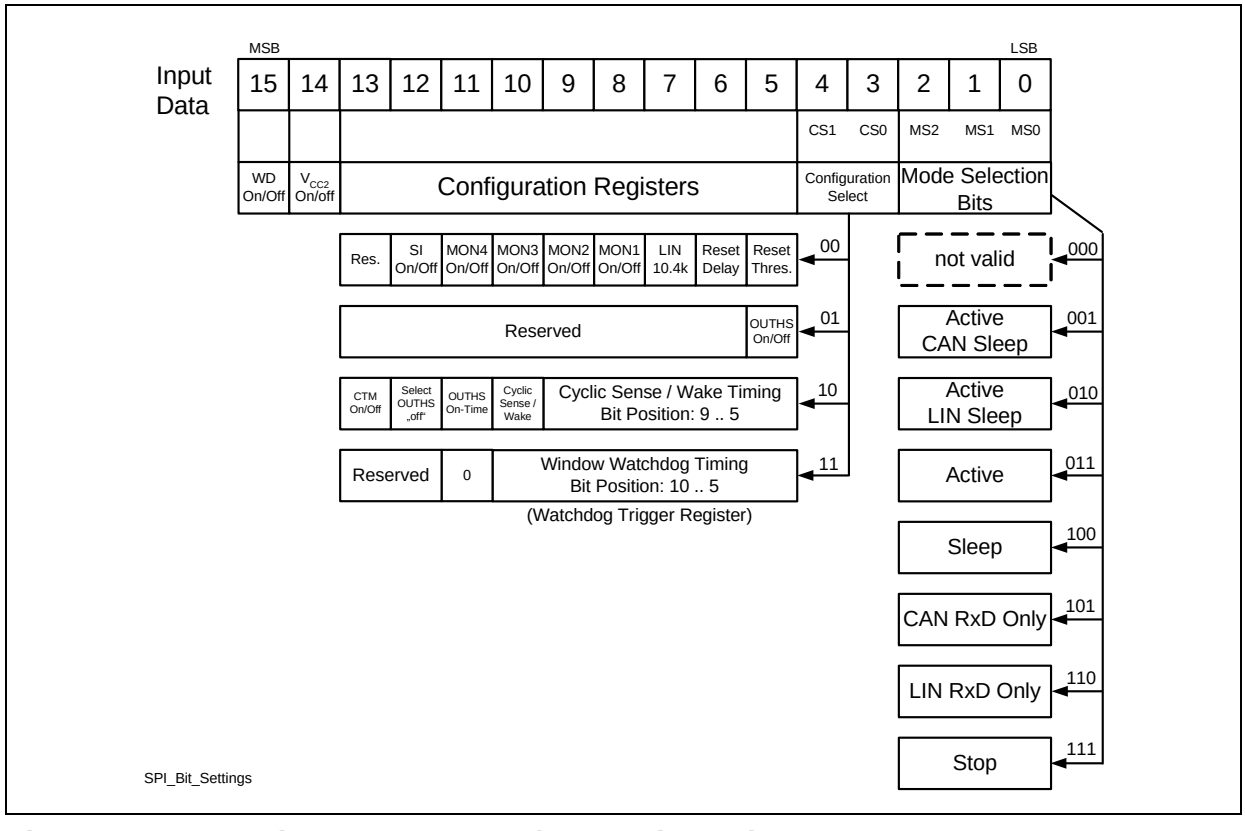

Figure 11 16-Bit SPI Input Data / Control Word

Table 3 SPI Input Data Bits

IBIT	Input Data
0 … 2	Mode Selection
3 … 4	Configuration Selection (determine meaning of “Configuration Setting Bits”)
5 … 13	Configuration Settings (meaning based on “Configuration Selection Bits”)
14	V_{CC2} Activation (power saving modes only)
15	Window Watchdog “on”/“off” (power saving modes only)

Table 4 Mode Selection Bits

MS2	MS1	MS0	Mode Selection: SBC Mode
0	0	0	“reserved” / not valid
0	0	1	SBC Active Mode: “CAN Sleep”
0	1	0	SBC Active Mode: “LIN Sleep”
0	1	1	SBC Active Mode (CAN & LIN “on”)
1	0	0	SBC Sleep (CAN, LIN & VReg “off”)
1	0	1	SBC Active mode : CAN Transceiver: RxD-Only
1	1	0	SBC Active mode : LIN Transceiver: RxD-Only
1	1	1	SBC Stop Mode (CAN & LIN “off”)

Table 5 Configuration Selection Bits

CS1	CS0	Configuration Selection
0	0	General Configuration
0	1	Integrated Switch Configuration
1	0	Cyclic Sense / Wake Configuration
1	1	Window Watchdog Configuration

Table 6 General & Integrated Switch Configuration

Pos.	General Configuration[1)]	Integrated Switch Configuration[2)]
5	Reset Threshold (see **Table** : “Reset Generator”, “0” = V_{RT1} / “1” = V_{RT2})	OUTHS “on” / “off”
6	Reset Delay (“0” = 5 ms / “1” = 0.5 ms)	“reserved” / not used
7	LIN “Low Slope Mode” (10.4 kBaud)	“reserved” / not used
8	MON1 Input Wake-Up Capability	“reserved” / not used
9	MON2 Input Wake-Up Capability	“reserved” / not used
10	MON3 Input Wake-Up Capability	“reserved” / not used
11	MON4 Input Wake-Up Capability	“reserved” / not used
12	Sense Input (SI) “on” / “off”	“reserved” / not used
13	“reserved” / not used	“reserved” / not used

1) “1” = ON (enable), “0” = OFF (disable)

2) “1” = ON, “0” = OFF

Table 7 Cyclic Sense / Wake & Window Watchdog Period Settings[1)]

Pos.	Cyclic Sense / Wake Configuration	Window Watchdog Configuration
5	Cyclic Period Bit 0 (T0)	Watchdog Period Bit 0 (T0)
6	Cyclic Period Bit 1 (T1)	Watchdog Period Bit 1 (T1)
7	Cyclic Period Bit 2 (T2)	Watchdog Period Bit 2 (T2)
8	Cyclic Period Bit 3 (T3)	Watchdog Period Bit 3 (T3)
9	Cyclic Period Bit 4 (T4)	Watchdog Period Bit 4 (T4)
10	Cyclic Sense / Wake Selection (“0” = Cyclic Sense / “1” = Cyclic Wake)	Watchdog Period Bit 5 (T5)
11	OUTHS On-Time Selection (“0” = 500 µs / “1” = 100 µs)	“0” [mandatory]
12	Cyclic Wake Mode only: Select OUTHS “off” via STS / On-Time (“0” = via STS / “1” = via HS On-Time)	“reserved” / not used
13	Continuous Timer Mode (incl. WKO) (“0” = “off” / “1” = “on”)	“reserved” / not used

1) “1” = ON, “0” = OFF

Table 8 Cyclic Sense / Wake Period Settings

T4	T3	T2	T1	T0	Cyclic Sense or Cyclic Wake Period
0	0	0	0	0	Cyclic Sense / Wake “off”
0	0	0	0	1	16 ms
0	0	0	1	0	32 ms
0	0	0	1	1	48 ms
0	0	1	0	0	64 ms
0	0	1	0	1	80 ms
0	0	1	1	0	96 ms
…	…	…	…	…	… ms
1	1	1	1	1	496 ms

Table 9 Window Watchdog Reset Period Settings

T5	T4	T3	T2	T1	T0	Window Watchdog Reset Period
0	0	0	0	0	0	“not a valid selection”
0	0	0	0	0	1	16 ms
0	0	0	0	1	0	32 ms
0	0	0	0	1	1	48 ms
0	0	0	1	0	0	64 ms
0	0	0	1	0	1	80 ms
0	0	0	1	1	0	96 ms
0	…	…	…	…	…	… ms
1	1	1	1	1	1	1008 ms

Table 10 SPI Output Data

Pos.	Output Data “active”[1]	Output Data “after wake-up”[2]
0	V_{CC1} Temperature Prewarning	V_{CC1} Temperature Prewarning
1	HS Overcurrent	HS Overcurrent
2	OUTHS UV / Temp. Shut-Down	OUTHS UV / Temp. Shut-Down
3	Window Watchdog Reset	Window Watchdog Reset
4	MON1 Logic Input Level	Wake-Up via MON1
5	MON2 Logic Input Level	Wake-Up via MON2
6	MON3 Logic Input Level	Wake-Up via MON3
7	MON4 Logic Input Level	Wake-Up via MON4
8	MONx Initialization Failure	MONx Initialization Failure
9	LIN Failure	Bus Wake-Up via LIN Msg.
10	CAN Local Failure	Bus Wake-Up via CAN Msg.
11	CAN Bus Failure	End of Cyclic Wake Period
12	V_{CC1} Fail (active low)	V_{CC1} Fail (active low)
13	V_{CC2} Fail (active low)	V_{CC2} Fail (active low)
14	V_{INT} Fail (active low)	V_{INT} Fail (active low)
15	“reserved” / not used	“reserved” / not used

1) “1” = ON (enable), “0” = OFF (disable)

2) “1” = ON, “0” = OFF

4.12 Window Watchdog, Reset

When the output voltage V_{cc1} exceeds the reset threshold voltage the reset output RO is switched HIGH after a delay time of typ. 5 ms. This is necessary for a defined start of the microcontroller when the application is switched on. As soon as an undervoltage condition of the output voltage ($V_{CC1} < V_{RT}$) appears, the reset output RO is switched LOW again. The LOW signal is guaranteed down to an output voltage $V_{CC1} \geq 1$ V. Please refer to **Figure 19**, **Reset Timing Diagram**.

After the above described delayed reset (LOW to HIGH transition of RO) the window watchdog circuit is started by opening a long open window of typ. 64 ms. The long open window allows the microcontroller to run its initialization sequences and then to trigger the watchdog via the SPI. A watchdog trigger is detected as a write access to the “window watchdog period bit field” within the SPI control word. In order to distinguish the watchdog from the cyclic sense/wake timing register the “Configuration Select Bits” needs to be set accordingly (see **“SPI (Serial Peripheral Interface)” on Page 21**). The trigger is accepted when the CSN input becomes HIGH after the transmission of the SPI word.

A correct watchdog trigger results in starting the window watchdog by opening a closed window with a width of 50% of the selected window watchdog reset period. This period, selected via the window watchdog timing bit field, is in the range between 16 ms and 1008 ms. This closed window is followed by a open window, with a width of 50% of the selected period. From now on the microcontroller has to service the watchdog by periodically writing to the window watchdog timing bit field. This write access has to meet the open window. A correct watchdog service immediately results in starting the next closed window (see **Figure 17 "Watchdog Time-Out Definitions" on Page 54**, safe trigger area).

Should the trigger signal not meet the open window a watchdog reset is created by setting the reset output RO low (see **Reset delay time** t_{RD}). Then the watchdog again starts by opening a long open window. In addition, a “window watchdog reset flag” is set within the SPI until the next successful watchdog trigger to monitor a watchdog reset. For fail safe reasons the TLE 7263E is automatically switched in SBC Standby mode if a watchdog trigger failure occurs. This minimizes the power consumption in case of a permanent faulty microcontroller.

In case of a watchdog reset the watchdog immediately starts with a long open window in SBC Standby Mode.

When entering a low power mode the watchdog can be requested to be disabled via an SPI bit (see **“SPI (Serial Peripheral Interface)” on Page 21**). Upon this request the watchdog is only turned off once the current consumption at V_{CC1} falls below the “watchdog current threshold”.

4.13 Sense Comparator using Sense Input SI and Interrupt Output INT

The sense comparator (early warning function) compares a voltage defined by the user to an internal reference voltage. Therefore the voltage to be supervised has to be scaled down by a voltage divider in order to compare it to the internal sense threshold V_{Slth}. This feature can be used e.g. to supervise the battery voltage in front of the reverse protection diode. The microcontroller is given a prewarning before an undervoltage reset due to low input voltage occurs. The prewarning is flagged by setting the interrupt output INT low in SBC Active, Standby, and Stop, as well as in CAN Receive - Only Mode, when activated by SPI. In SBC Sleep Mode the sense function is inactive.

Calculation of the voltage divider can be easily done since the sense input current can be neglected. An internal blanking time prevents from false triggering due to line transients. Further improvement is possible by the use of an external ceramic capacitor at the SI pin (see **Figure 22**, **Application Circuit**).

4.14 V_{INT}/V_{CC} Fail Detection via SPI Bit

Should the internal supply voltage become lower than the internal threshold $V_{INT, th}$ (typ. 2.5 V) the V_{INT}-Fail, threshold SPI bit will be reset in order to indicate the low voltage condition. All other SPI settings are also reset by this condition. The V_{INT} Fail feature can also be used to give an indication when the ECU has been changed and therefore a pre-setting routine of the microcontroller has to be started.

Further there is also a V_{CC} monitor implemented, where the V_{CCx} is compared to the threshold voltage $V_{CCx\text{-}Fail,\ threshold}$ and the V_{CC} SPI bit is reset accordingly. This monitoring is only available during voltage-regulator operation.

4.15 Monitoring / Wake-Up Inputs MON1/2/3/4 and Wake-Up Output WKO

In addition to a wake-up from SBC Sleep mode via the CAN or LIN bus lines it is also possible to wake-up the TLE 7263E from low power mode via the monitoring/wake-up inputs. These inputs are sensitive to a transition of the voltage level, either from high to low or vice versa. Monitoring is available in Active Mode and indicates the voltage level of the inputs.

A positive or negative voltage edge at MONx in SBC Sleep or Stop Mode results in setting the output WKO low to signal a wake-up. After a wake-up via MONx the first transmission of the SPI diagnosis word in SBC Standby mode indicates the wake-up source. Further SPI status word transmissions show the logic level of the monitoring inputs.

When switching the TLE 7263E into SBC Sleep mode (cyclic sense feature activated) the voltage level at the wake-up inputs is sensed 2 times to initialize the reference voltage. Should this initialization fail (2 samples are unequal) the device is automatically

set in SBC Standby mode and the initialization error is shown indicated in the SPI status word.

To have a defined level at a floating MONx pin a hold current is implemented. For high level at MONx a pull up current $I_{PU,MON}$ is driven out of the MONx pin, for low level at MONx a pull down current $I_{PD,MON}$ is drawn into the MONx pin.

4.16 High Side Switch

The high side output OUTHS is able to switch loads up to 150 mA. Its on-resistance is 2.5 Ω typ. @ 25 °C. In SBC Active, Standby, as well as in CAN and LIN Receive-Only mode the high side output is switched on and off, respectively via an SPI input bit.

To supply external wake-up circuits in SBC Sleep Mode the output OUTHS can be periodically switched on by the TLE 7263E itself. How Cyclic Sense works and how it is activated is described in detail in **“Operation Modes” on Page 9**. Beside the cyclic sense period can the on-time of the OUTHS be programmed to either 500 µs (default setting) or 100 µs via SPI input bit. OUTHS undervoltage, temperature shutdown, overcurrent as well as a temperature pre-warning is indicated by the SPI status word.

The OUTHS is protected against short circuit and overload. As soon as the undervoltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switch is automatically disabled by the undervoltage lockout circuit. Moreover the switch is automatically disabled when a reset or watchdog reset occurs.

4.17 Fail Safe Feature

The output FSO becomes HIGH when the watchdog is correctly serviced by the microcontroller for the fourth time. As soon as either an undervoltage reset or watchdog reset occurs, it is set LOW again. This feature is very useful to control critical applications independent of the microcontroller e.g. to disable the power supply in case of a microcontroller failure.

4.18 Send to Sleep Input STS

During Cyclic Wake the STS input is used to switch the SBC back to a low current mode (High-Side switch “off”) when the microcontroller has completed its tasks during the periodic wake-up phase, and before it enters its power saving mode (“Stop”) again.

4.19 Flash Program Mode

For flash programming it is useful to disable the window watchdog function. This can be done by applying a voltage of V_{INT} > 7.0 V at pin INT. This is useful e.g. if the flash-memory of the micro has to be programmed and therefore a regular watchdog triggering is not possible.

Additionally, the transmission rate of the integrated LIN transceiver will be changed to maximal 150 kBaud.

The Sense Comparator using Sense Input and Interrupt Output INT can not be used with Flash Program Mode. The Sense Input feature must be switched off via SPI.

Hints for Unused Pins

- SI: connect to GND
- OUTHS: leave open
- MON1/2/3/4: connect to GND
- INT / WKO: leave open
- RO / FSO: leave open

5 General Product Characteristics

5.1 Maximum Ratings

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Voltages					
Supply voltage	V_S	-0.3	40	V	–
Regulator output voltage	V_{CC1}, V_{CC2}	-0.3	5.5	V	–
CAN bus voltage (CANH, CANL)	$V_{CANH/L}$	-27	40	V	–
Input voltage at SPLIT	V_{SPLIT}	-27	40	V	–
Input voltage at MONx and SI	$V_{WK/SI}$	-27	40	V	–
Output voltage at OUTHS and MTS	V_O	-27	V_S + 0.3	V	–
Logic input voltages (DI, CLK, CSN, STS, TxD)	V_I	-0.3	V_{CC} + 0.3	V	0 V<V_S<24V 0 V<V_{CC}<5.5V
Logic output voltage (DO, RO, INT, RxD, FSO, WKO)	$V_{DRI,RD}$	-0.3	V_{CC} + 0.3	V	0 V<V_S<24V 0 V<V_{CC}<5.5V
Input voltage at Pin INT	V_{INT}	-27	40	V	Sense Input off
LIN line bus input voltages	V_{bus}	-27	40	V	–
ESD resistivity					
ESD at RxD pin versus GND	$V_{ESD,RxD}$	-2	1.5	kV	HBM[1)]
ESD all other pins. versus GND	V_{ESD1}	-2	2	kV	HBM[1)]
ESD at pin CANH, CANL, SPLIT, LIN, MONx versus GND	V_{ESD1}	-6	6	kV	HBM[1)]
Temperatures					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) ESD susceptibility HBM according to EIA/JESD 22-A 114B.

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

5.2 Operating Range

Table 12 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Supply voltage	V_S	$V_{UV\ OFF}$	27	V	After V_S rising above $V_{UV\ ON}$
Supply voltage	V_S	$V_{UV\ OFF}$	40	V	40 V load dump
Supply voltage slew rate	dV_S/dt	-0.5	5	V/µs	–
Logic input voltage (DI, CLK, CSN, TxD, STS)	V_I	-0.3	V_{CC1}	V	–
Output capacitor	$C_{CC1/2}$	100	–	nF	ESR < 6 Ω @ f = 10 kHz
SPI clock frequency	f_{clk}	–	4	MHz	–
Junction temperature	T_j	-40	150	°C	–

5.3 Thermal Resistance

Parameter	Symbol	Limit Values			Unit	Remarks
		Min.	Typ.	Max.		
Junction to Case[1)]	R_{thjC}	–	1	5	K/W	
Junction to Ambient[1)]	R_{thjA}	–	25	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on 2s2p board for 1W. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (70µm thick)., with thermal via array under the exposed pad contacted the first inner copper layer

6 Electrical Characteristics

Table 13 Electrical Characteristics

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Quiescent Current; Pin V_S						
Current consumption	I_Q	–	6	8	mA	SBC Active Mode
			1.2	2	mA	Active [CAN Sleep]
			1.7	3	mA	=> LIN dominant; without R_L
			4	6	mA	Active [LIN Sleep]
Current consumption	I_Q	–	68	80	µA	stand-by mode; T_j = 25 °C; V_{CC2} “off”
	I_Q	–	580	900	µA	stand-by mode; T_j = 25 °C; V_{CC2} “off”; after LIN wake-up / power-up
Current consumption	I_Q	–	68	80	µA	stop mode; T_j = 25 °C; V_{CC2} “off”; without cyclic sense
Current consumption	I_Q	–	76	88	µA	stop mode; T_j = 85 °C; V_{CC2} “off”; without cyclic sense
Current consumption	I_Q	–	49	60	µA	sleep mode; T_j = 25 °C; V_{CC2} “off”; without cyclic sense
Current consumption	I_Q	–	53	65	µA	sleep mode; T_j = 85°C; V_{CC2} “off”; without cyclic sense
Current consumption	I_Q	–	220	300	µA	sleep mode, during HS-On phase; T_j = 25 °C; V_{CC2} “off”

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Current consumption	I_Q	–	240	330	µA	sleep mode, during HS-On phase; T_j = 85°C; V_{CC2} "off"
Voltage Regulator; Pin $V_{CC1/2}$						
Output voltage	$V_{CC1/2}$	4.9	5.0	5.1	V	1 mA<$I_{CC1/2}$<100 mA; 6 V < V_S < 20 V
Line regulation	$\Delta V_{CC1/2}$	–	–	20	mV	6 V < V_S < 16 V; I_{CC} = 1 mA
Load regulation	$\Delta V_{CC1/2}$	–	–	50	mV	5 mA<$I_{CC1/2}$<100 mA; V_S = 6 V
Power supply ripple rejection	$PSRR$	–	40	–	dB	V_r = 1 Vpp; f_r = 100 Hz; specified by design; not subject to production test
Output current limit	$I_{CC1/2max}$	200	–	500	mA	$V_{CC1/2}$ = 4.5 V; power transistor thermally monitored; 150 mA for external load
Drop voltage	V_{DR}	–	–	0.5	V	$I_{CC1/2}$ = 150 mA; internal modules not supplied; 4.5V < V_S < 5.4V

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Oscillator						
Oscillating frequency	f_{OSC}	–	256	–	kHz	–
Internal cycling time (1/128 × f_{OSC})	t_{CYL}	400	500	600	µs	–
Reset Generator; Pin RO						
Reset threshold voltage	V_{RT1}	4.5	4.65	4.8	V	default SPI setting
	V_{RT2}	3.2	3.35	3.5	V	SPI option; $V_S \geq 4$ V
Reset threshold hysteresis	$V_{RT,hys}$	–	100	–	mV	–
Reset low output voltage	V_{RO}	–	0.2	0.4	V	I_{RESET} = 1 mA for $V_{CC1} = V_{RT1/2}$; I_{RESET} = 200 µA for $V_{RT1/2} > V_{CC}1 \geq 1$ V
Reset high output voltage	V_{RO}	0.7 x V_{CC1}	–	V_{CC1} + 0.1	V	–
Reset pull-up current	I_{RO}	20	150	500	µA	V_{RO} = 0 V
Reset reaction time	t_{RR}	4	10	26	µs	$V_{CC1} < V_{RT1/2}$ to RO = L
Reset delay time	t_{RD1}	4.0	5.0	6.0	ms	default SPI setting; after Power-On-Reset
	t_{RD2}	0.4	0.5	0.6	ms	SPI setting option
Fail Safe Output; Pin FSO						
Watchdog edge count difference to set HIGH	n_{FS}	–	4	–	–	–
Fail Safe low output voltage	V_{FS}	–	0.2	0.4	V	I_{FSO} = 1 mA for $V_{CC1} = V_{RT1/2}$ or I_{FSO} = 200 µA for $V_{CC1} \geq 1$ V
Fail Safe high output voltage	V_{FS}	V_{CC}- 0.6	–	V_{CC} + 0.1	V	I_{FSO} = -1 mA for $V_{CC1} \geq V_{RT1/2}$

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Sense Input (Early Warning) SI, V_{CCx}-Fail, Interrupt Output INT						
Sense In threshold voltage	$V_{SI,th}$	1.8	2.3	2.8	V	V_{SI} decreasing
		2.1	2.3	2.5	V	measured at 25°C, V_{SI} decreasing
Sense In threshold hysteresis	$V_{SI,hys}$	100	200	300	mV	–
Sense reaction time	$t_{S,r}$	5	10	20	µs	V_{SI} < $V_{SI,th}$ to INT = low
Interrupt Out high voltage	$V_{INThigh}$	0.7 × V_{CC1}	–	V_{CC1}	V	I_0 = -20 µA
Interrupt Out low voltage	V_{INTlow}	0	–	1.2	V	I_0 = 1.25 mA
Interrupt pull-up current	I_{INT}	20	150	500	µA	V_{INT} = 0 V
Input voltage for Flash Programming Mode at pin INT	V_{INT}	7	–	–	V	
V_{CC1}-Fail threshold voltage	$V_{VCC1,th}$	2.1	2.6	3.1	V	–
V_{CC1}-Fail reaction time	$t_{VCC1,r}$	10	20	30	µs	–
Watchdog Generator						
Long open window (128 cyl.)	t_{LW}	51	64	77	ms	–
Watchdog reset-pulse	t_{WDR1}	3.6	5.0	6.0	ms	default SPI setting
	t_{WDR2}	0.012	0.5	0.6	ms	SPI setting option
Watchdog current threshold	$I_{WD,th}$	0.5	–	8	mA	–
Monitoring Inputs MONx						
MONx input threshold voltage	V_{MONxth}	2	3	4	V	–

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Input hysteresis	$V_{I, hys.}$	0.1	–	0.7	V	
Pull up current	$I_{PU,MON}$	-30	-10	-3	µA	V_{MON} = 3.8V
Pull down current	$I_{PD,MON}$	3	10	30	µA	V_{MON} = 2V
MONx filter time	$t_{MONx, f}$	10	–	20	µs	–
Input current	I_{MONx}	-2	–	2	µA	V_{MONx} = 0 V; V_{MONx} > 5V
High Side Output OUTHS						
Static Drain-Source ON-Resistance; I_{OUTH} = -150 mA	$R_{DSON HS}$	–	2.5	3.5	Ω	T_j = 25 °C
		–	–	6.0	Ω	–
Active Zener voltage	V_{OUTHS}	–	V_S-45	–	V	I_{OUTHS} = -0.15 A
Leakage current	I_{QLHS}	-10	–	–	µA	V_{OUTHS} = 0 V
Switch ON delay time	t_{dONHS}	–	–	20	µs	CSN high to OUTHS
Switch OFF delay time	t_{dOFFHS}	–	–	20	µs	CSN high to OUTHS
Overcurrent shutdown threshold	I_{SDHS}	-0.8	-0.4	-0.2	A	–
Shutdown filter time	t_{dSDHS}	10	25	40	µs	–
UV-Switch-ON voltage	$V_{UV ON}$	–	5.35	6.00	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV OFF}$	4.50	4.85	–	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV HY}$	0.1	0.2	–	V	$V_{UV ON}$ - $V_{UV OFF}$
Cyclic sense period	$t_{P CS}$	–	16 to 512	–	ms	selectable via SPI bits; tolerance depending on internal oscillator
Cyclic sense ON time	$t_{CS on1}$	0.4	0.5	0.6	ms	default SPI setting
	$t_{CS on2}$	0.08	0.1	0.12	ms	SPI option

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Send to Sleep Input (STS)						
H-input voltage threshold	V_{IH}	–	–	0.7 × V_{CC1}	V	–
L-input voltage threshold	V_{IL}	0.3 × V_{CC1}	–	–	V	–
Hysteresis of input voltage	V_{IHY}	0.8	–	1.5	V	–
Pull-down resistance at pin STS	R_{ISTS}	20	40	80	kΩ	V_{STS} = 0.2 × V_{CC1}
STS pulse width	t_{STS}	10	–	–	µs	one oscillator period
Wake Event Output WKO						
HIGH level output voltage	$V_{WKO,H}$	0.8 × V_{CC1}	–	–	V	I_{WKO} = -1.6 mA
LOW level output voltage	$V_{WKO,L}$	–	–	0.2 × V_{CC1}	V	I_{WKO} = 1.6 mA
CAN Transceiver Characteristics Receiver Output RxD						
HIGH level output current	$I_{RD,H}$	–	-4	-2	mA	V_{RD} = 0.8 × V_{CC1}; V_{diff} < 0.4 V[1)]
LOW level output current	$I_{RD,L}$	2	4	–	mA	V_{RD} = 0.2 × V_{CC1}; V_{diff} > 1 V[1)]
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TD,H}$	–	0.5 × V_{CC1}	0.7 × V_{CC1}	V	recessive state
TxD input hysteresis	$V_{TD,hys}$	–	0.4	–	V	–
LOW level input voltage threshold	$V_{TD,L}$	0.3 × V_{CC1}	0.5 × V_{CC1}	–	V	dominant state
TxD pull-up resistance	R_{TD}	10	20	40	kΩ	–

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
CAN Bus Receiver						
Differential receiver threshold voltage, recessive to dominant edge	$V_{diff,d}$	–	0.80	0.90	V	V_{diff} = V_{CANH} - V_{CANL} "active mode"
Differential receiver threshold voltage, dominant to recessive edge	$V_{diff,r}$	0.50	0.60	–	V	V_{diff} = V_{CANH} - V_{CANL} "active mode"
Common Mode Range	CMR	-12	–	12	V	–
Differential receiver hysteresis	$V_{diff,hys}$	–	110	–	mV	"active mode"
CANH, CANL input resistance	R_i	10	20	30	kΩ	recessive state
Differential input resistance	R_{diff}	20	40	60	kΩ	recessive state
Wake-up Receiver threshold voltage, recessive to dominant edge	$V_{diff, d}$	–	0.8	1.15	V	"sleep/stop mode"
Wake-up Receiver threshold voltage, dominant to recessive edge	$V_{diff, r}$	0.4	0.7	–	V	"sleep/stop mode"
Wake-up Receiver differential receiver hysteresis	$V_{diff, hys.}$	–	120	–	mV	"sleep/stop mode"

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
CAN Bus Transmitter						
CANL/CANH recessive output voltage	$V_{CANL/H}$	2.0	–	3.0	V	no load
CANH, CANL recessive output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$	V_{diff}	-500	–	50	mV	$V_{TxD} = V_{CC1}$; no load
CANL dominant output voltage	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V; V_{CC2} = 5 V
CANH dominant output voltage	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V; V_{CC2} = 5 V
CANH, CANL dominant output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$	V_{diff}	1.5	–	3.0	V	V_{TxD} = 0 V; V_{CC2} = 5 V
CANH short circuit current	I_{CANHsc}	-200	-80	-50	mA	$V_{CANHshort}$ = 0 V
CANL short circuit current	I_{CANLsc}	50	80	200	mA	$V_{CANLshort}$ = 18 V
Leakage current	$I_{CANH,lk}$ $I_{CANL,lk}$	–	25	–	µA	$V_S = V_{CC2}$ = 0 V; 0 V < $V_{CANH,L}$ < 5 V
Split Termination Output; Pin SPLIT						
Split output voltage	V_{SPLIT}	0.3 × V_{CC2}	0.5 × V_{CC2}	0.7 × V_{CC2}	V	normal mode; -500 µA < I_{SPLIT} < 500 µA
Leakage current	I_{SPLIT}	-5	0	5	µA	standby mode; -22 V < V_{SPLIT} < 35 V
SPLIT output resistance	R_{SPLIT}	–	600	–	Ω	–

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Dynamic CAN-Transceiver Characteristics						
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{d(L),TR}$	–	150	255	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC1/2}$ = 5 V; C_{RxD} = 20 pF
Propagation delay TxD-to-RxD HIGH (dominant to recessive)	$t_{d(H),TR}$	–	150	255	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC1/2}$ = 5 V; C_{RxD} = 20 pF
Propagation delay TxD LOW to bus dominant	$t_{d(L),T}$	–	50	120	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC1/2}$ = 5 V
Propagation delay TxD HIGH to bus recessive	$t_{d(H),T}$	–	50	120	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC1/2}$ = 5 V
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	100	135	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC1/2}$ = 5 V; C_{RxD} = 20 pF
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	100	135	ns	C_L = 47 pF; R_L = 60 Ω; $V_{CC1/2}$ = 5 V; C_{RxD} = 20 pF
Min. dominant time for bus wake-up	t_{WU}	1	3	5	µs	–
TxD permanent dominant disable time	t_{TxD}	0.3	–	1.0	ms	–

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
LIN Transceiver Characteristics						
Receive Output RxD						
HIGH level output voltage	$V_{RxD,H}$	0.8 × V_{CC1}	–	–	V	$I_{RxD(LIN)}$ = -1.6 mA; V_{bus} = V_S
LOW level output voltage	$V_{RxD,L}$	–	–	0.2 × V_{CC1}	V	$I_{RxD(LIN)}$ = 1.6 mA; V_{bus} = 0 V
Transmission Input TxD						
HIGH level input voltage threshold	$V_{TxD,H}$	–	–	0.7 × V_{CC1}	V	recessive state
TxD input hysteresis	$V_{TxD,hys}$	0.8		1.5	V	–
LOW level input voltage threshold	$V_{TxD,L}$	0.3 × V_{CC1}	–	–	V	dominant state
TxD pull-up Resistor	R_{TxD}	20	40	80	kΩ	V_{TxD} = 0 V
Bus Receiver						
Receiver threshold voltage, recessive to dominant edge	$V_{bus,rd}$	0.42 × V_S	0.48 × V_S	–	V	–
Receiver dominant state	V_{busdom}	–	–	0.40 × V_S	V	(LIN Spec 1.3 (2.0); Line 10.1.9 (3.1.9))
Receiver threshold voltage, dominant to recessive edge	$V_{bus,dr}$	–	0.52 × V_S	0.58 × V_S	V	$V_{bus,rec}$ < V_{bus} < 27 V
Receiver recessive state	V_{busrec}	0.6 × V_S	–	–	–	(LIN Spec 1.3 (2.0); Line 10.1.10 (3.1.10))
Receiver center voltage	$V_{buscent}$	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	(LIN Spec 1.3 (2.0); Line 10.1.11 (3.1.11))
Receiver hysteresis	$V_{bus,hys}$	0.02 × V_S		0.175 × V_S	V	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$ (LIN Spec 1.3 (2.0); Line 10.1.12 (3.1.12))

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Wake-up threshold voltage	V_{wake}	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–
Bus Transmitter						
Bus serial diode voltage drop	$V_{serdiode}$	0.4	0.7	1.0	V	V_{TxD} = high Level
Bus dominant output voltage	$V_{bus,dom}$	–	–	1.2	V	V_{TxD} = 0 V; V_S = 7 V; R_L = 500 Ω; (LIN Spec 1.3; Line 10.1.13)
		–	–	2.0	V	V_S = 18 V; R_L = 500 Ω; (LIN Spec 1.3; Line 10.1.14)
Bus dominant output voltage	$V_{bus,dom}$	0.6	–	–	V	V_{TxD} = 0 V; V_S = 7 V; R_L = 1 kΩ; (LIN Spec 1.3; Line 10.1.15)
		0.8	–	–	V	V_S = 18 V; R_L = 1 kΩ; (LIN Spec 1.3; Line 10.1.16)
Bus short circuit current	$I_{bus,sc}$	40	100	150	mA	$V_{bus,short}$ = 18 V (LIN Spec 1.3 (2.0); Line 10.1.4 (3.1.4))

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Leakage current	$I_{bus,lk}$	-1000	–	–	µA	V_S = 0 V; V_{bus} = -12V (LIN Spec 1.3 (2.0); Line 10.1.7 (3.1.7))
		-500	-140		µA	V_S = 0 V; V_{bus} = -8V
		–	10	25	µA	V_S = 0 V; V_{bus} = 18 V (LIN Spec 1.3 (2.0); Line 10.1.8 (3.1.8))
		-1	–	–	mA	V_S = 18 V; V_{bus} = 0 V (LIN Spec 1.3 (2.0); Line 10.1.5(3.1.5))
		–	–	20	µA	V_{BUS} =18V V_S = 8V (LIN Spec 1.3 (2.0); Line 10.1.6 (3.1.6))
Bus pull-up resistance	R_{bus}	20	30	60	kΩ	Active/Standby mode (LIN Spec 1.3 (2.0); Line 10.2.2 (3.2.2))
LIN output current	I_{lin}	5	20	60	µA	Sleep mode;V_{bus} = 0V

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Dynamic Transceiver Characteristics						
Slew rate falling edge	S_{fslope}	-3	–	-1	V/µs	60% > V_{bus} > 40% 1 µs < ($\tau = R_l \times C_{bus}$) < 5 µs; V_S = 18V; Active mode [2] (LIN Spec 1.3; Line 10.3.1)
Slew rate falling edge	S_{fslope}	-3	–	-0.5	V/µs	60% > V_{bus} > 40% 1 µs < ($\tau = R_l \times C_{bus}$) < 5 µs; V_S = 7V; Active mode [2] (LIN Spec 1.3; Line 10.3.2)
Slew rate rising edge	S_{rslope}	1	–	3	V/µs	40% < V_{bus} < 60% 1 µs < ($\tau = R_l \times C_{bus}$) < 5 µs; V_S = 18V; Active mode [2] (LIN Spec 1.3; Line 10.3.1)
Slew rate rising edge	S_{rslope}	0.5	–	3	V/µs	40% < V_{bus} < 60% 1 µs < ($\tau = R_l \times C_{bus}$) < 5 µs; V_S = 7V; Active mode. [2] (LIN Spec 1.3; Line 10.3.2)
Slope symmetry	$t_{slopesym}$	-5	–	5	µs	t_{fslope} - t_{rslope}; V_S = 18.0 V [2] (LIN Spec 1.3; Line 10.3.3)

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Propagation delay TxD LOW to bus	$t_{d(L),T}$	–	1	4	µs	(LIN Spec 1.3; Line 10.3.6)[2)]
Propagation delay TxD HIGH to bus	$t_{d(H),T}$	–	1	4	µs	(LIN Spec 1.3; Line 10.3.6)[2)]
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	–	1	6	µs	C_{RxD} = 20 pF; (LIN Spec 1.3; Line 10.3.7)
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	–	1	6	µs	C_{RxD} = 20 pF; (LIN Spec 1.3; Line 10.3.7)
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$ (LIN Spec 1.3; Line 10.3.8)
Transmitter delay symmetry	$t_{sym,T}$	-2	–	2	µs	$t_{sym,T} = t_{d(L),T} - t_{d(H),T}$ (LIN Spec 1.3; Line 10.3.9)[2)]
Wake-up delay time	t_{wake}	30	100	150	µs	$T_j \leq 125$ °C
		–	–	170	µs	$T_j \leq 150$ °C
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V
TxD dominant time out recovery time	t_{torec}	–	10	–	µs	V_{TxD} = 5 V Not subject to production test. Specified by design

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Transfer Rate 20 kBit/s; 1 µs < τ = $R_L \times C_{bus}$ < 5 µs						
Duty cycle D1	D1	0.396	–	–		duty cycle 1: $TH_{Rec(max)}$ = 0.744 × V_S; $TH_{Dom(max)}$ = 0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/[2 t_{bit}] (LIN Spec 2.0; line 3.3.1)
Duty cycle D2	D2	–	–	0.581		duty cycle 2: $TH_{Rec(min)}$ = 0.422 × V_S; $TH_{Dom(min)}$ = 0.284 × V_S; V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/[2 t_{bit}] (LIN Spec 2.0; line 3.3.2)
Transfer Rate 10.4 kBit/s; 1 µs < τ = $R_L \times C_{bus}$ < 5 µs						
Duty cycle D3	D3	0.417	–	–		duty cycle 3 $TH_{Rec(max)}$ = 0.778 × V_S; $TH_{Dom(max)}$ = 0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/[2 t_{bit}] (LIN Spec 2.0; line 3.4.1)

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Duty cycle D4	D4	–	–	0.590		duty cycle 4 $TH_{Rec(min)}$ = 0.389 × V_S; $TH_{Dom(min)}$ = 0.251 × V_S; V_S = 7.6 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/[2 t_{bit}] (LIN Spec 2.0; line 3.4.2)
Master Termination Switch Output; Pin MTS						
Ron resistance	R_{onMTS}	–	33	60	Ω	I_{MTS} = -15 mA
Maximum output current	I_{MTS}	40	–	150	mA	V_{MTS} = 0 V
Leakage current	$I_{MTS,lk}$	-5.0	–	5.0	µA	sleep mode; V_{MTS} = 0 V

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
SPI-Interface **Logic Inputs DI, CLK and CSN**						
H-input voltage threshold	V_{IH}	–	–	0.7 × V_{CC1}	V	–
L-input voltage threshold	V_{IL}	0.3 × V_{CC1}	–	–	V	–
Hysteresis of input voltage	V_{IHY}	0.8		1.5	V	–
Pull-up resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	V_{CSN} = 0.7 × V_{CC1}
Pull-down resistance at pin DI and CLK	$R_{ICLK/DI}$	20	40	80	kΩ	$V_{DI/CLK}$ = 0.2 × V_{CC1}
Input capacitance at pin CSN, DI or CLK	C_I	–	10	15	pF	Not subject to production test. Specified by design
Logic Output DO						
H-output voltage level	V_{DOH}	V_{CC1} -0.4	V_{CC1} - 0.2	–	V	I_{DOH} = -1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA
Tri-state leakage current	I_{DOLK}	-10	–	10	µA	V_{CSN} = V_{CC1}; 0 V < V_{DO} < V_{CC1}
Tri-state input capacitance	C_{DO}	–	10	15	pF	Not subject to production test. Specified by design
Data Input Timing Not subject to production test. Specified by design						
Clock period	t_{pCLK}	250	–	–	ns	–
Clock high time	t_{CLKH}	125	–	–	ns	–
Clock low time	t_{CLKL}	125	–	–	ns	–
Clock low before CSN low	t_{bef}	125	–	–	ns	–
CSN setup time	t_{lead}	250	–	–	ns	–

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
CLK setup time	t_{lag}	250	–	–	ns	–
Clock low after CSN high	t_{beh}	125	–	–	ns	–
DI setup time	t_{DISU}	50	–	–	ns	–
DI hold time	t_{DIHO}	50	–	–	ns	–
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	50	ns	–
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	50	ns	–
Delay time for mode change from Normal Mode to Sleep Mode	t_{fIN}	–	–	10	µs	–
CSN high time	$t_{CSN(high)}$	15	–	–	µs	two oscillator periods
Data Output Timing Not subject to production test. Specified by design						
DO rise time	t_{rDO}	–	30	80	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	30	80	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	50	ns	low impedance
DO disable time	t_{DISDO}	–	–	50	ns	high impedance
Thermal Prewarning and Shutdown (junction temperatures) (Not subject to production test. Specified by design)						
V_{CC1} thermal prewarning ON temperature	T_{jPW}	120	145	170	°C	bit 0 of SPI diagnosis word
V_{CC1} thermal prewarning hyst.	ΔT	–	25	–	K	–
$V_{CC1/2}$ thermal shutdown temp.	T_{jSD}	155	185	200	°C	hysteresis 35 K (typ.)
V_{CC1} ratio of SD to PW temp.	T_{jSD}/ T_{jPW}	–	1.20	–	–	–

Table 13 Electrical Characteristics (cont'd)

V_S = 13.5 V; I_{CC1} = 1 mA; 4.9 V < $V_{CC1/2}$ < 5.1 V; SBC Active Mode; all outputs open; -40 °C < T_j < 150 °C (max. 125 °C for CAN circuit characteristics); all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
OUTHS thermal shutdown temp.	T_{jSD}	150	175	200	°C	–
OUTHS thermal shutdown hyst.	ΔT	–	10	–	K	–
CAN Transmitter thermal shutdown temp.	T_{jSD}	150	–	190	°C	–
CAN Transmitter thermal shutdown hyst.	ΔT	–	10	–	K	–
LIN Transmitter thermal shutdown temp.	T_{jSD}	150	–	190	°C	–
LIN Transmitter thermal shutdown hyst.	ΔT	–	10	–	K	–

1) $V_{diff} = V_{CANH} - V_{CANL}$

2) tested at 20kbit/s

Timing Diagrams

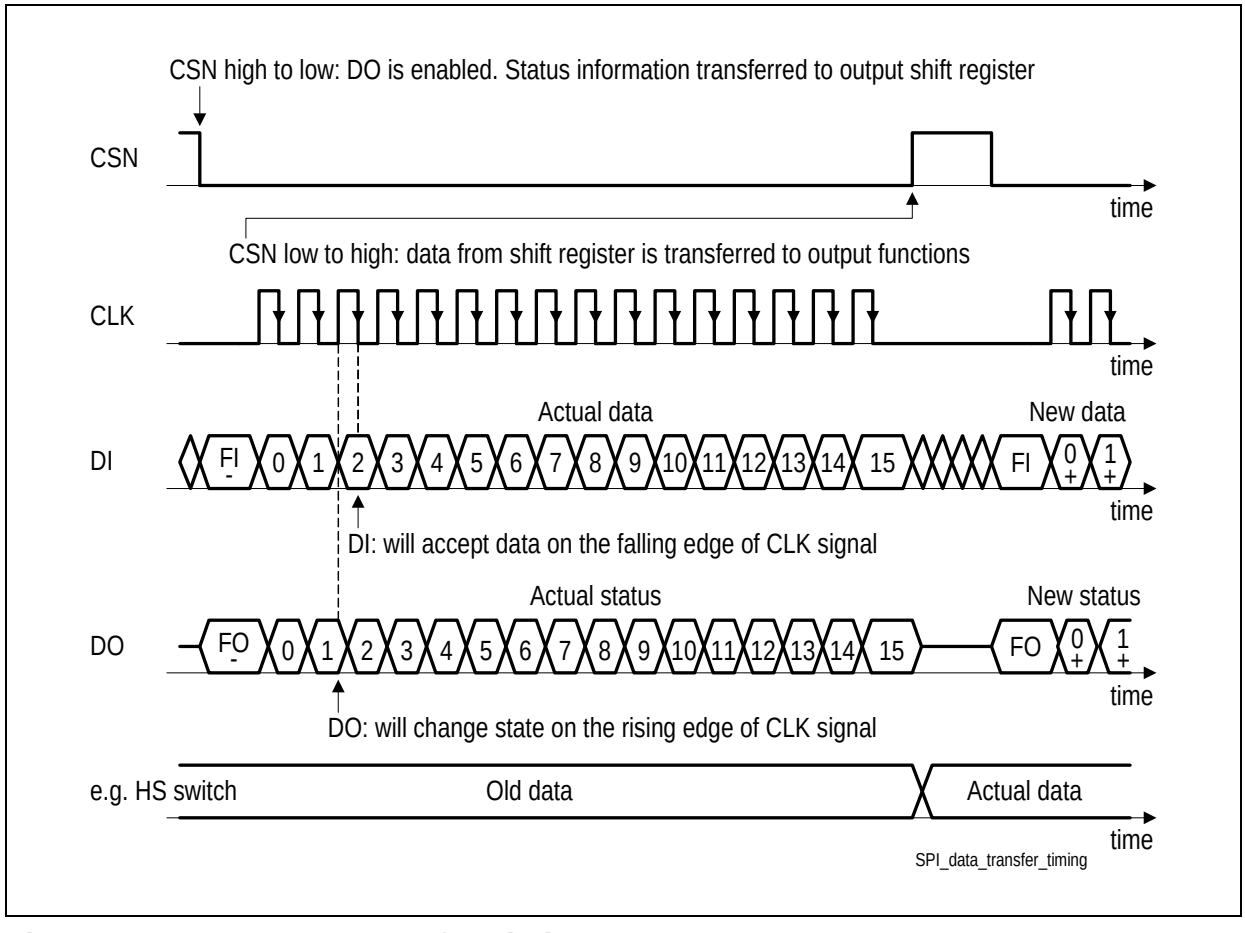

Figure 12 SPI-Data Transfer Timing

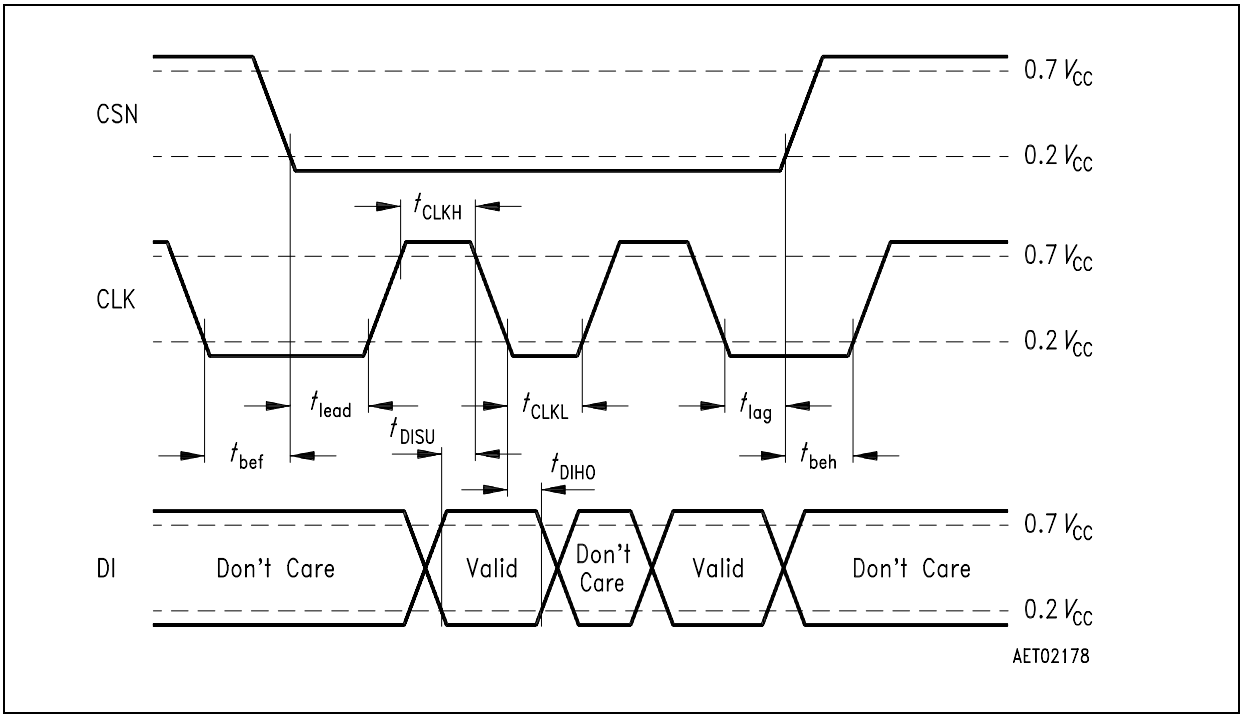

Figure 13 SPI-Input Timing

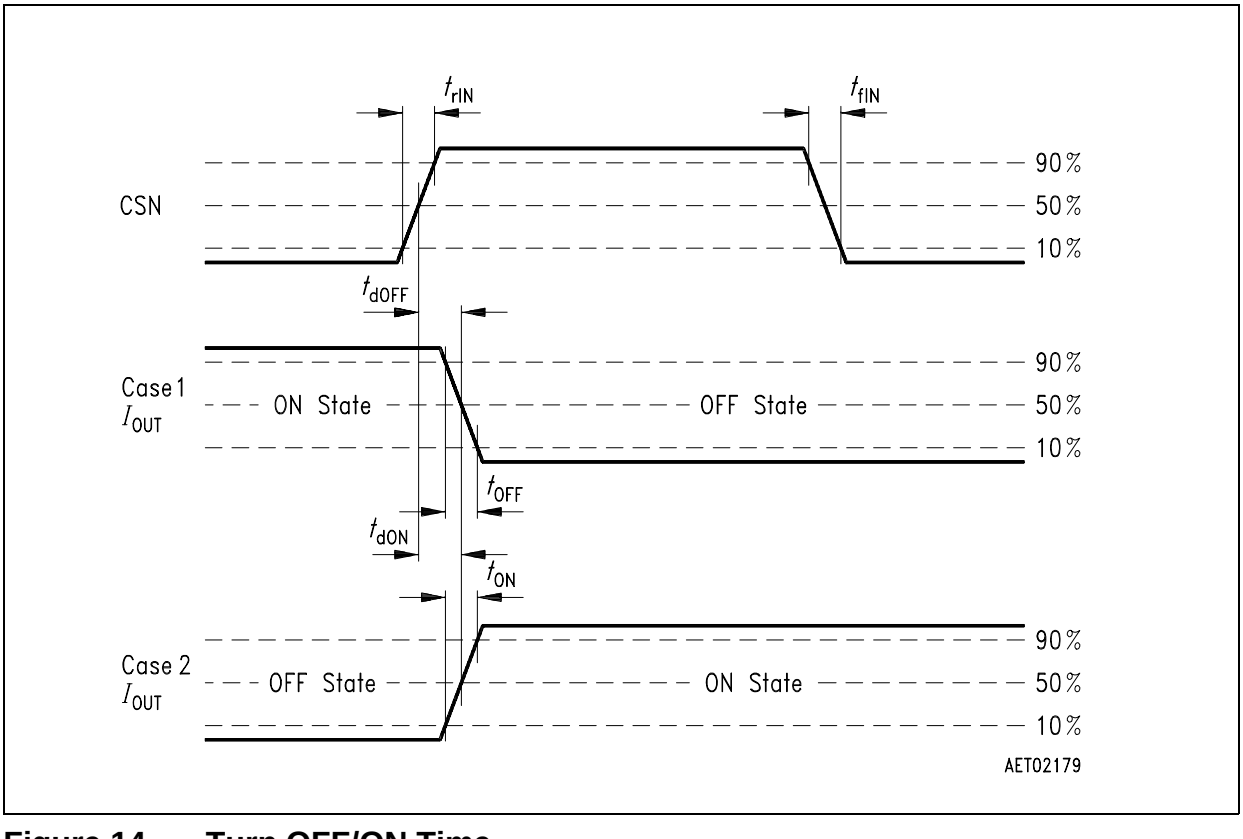

Figure 14 Turn OFF/ON Time

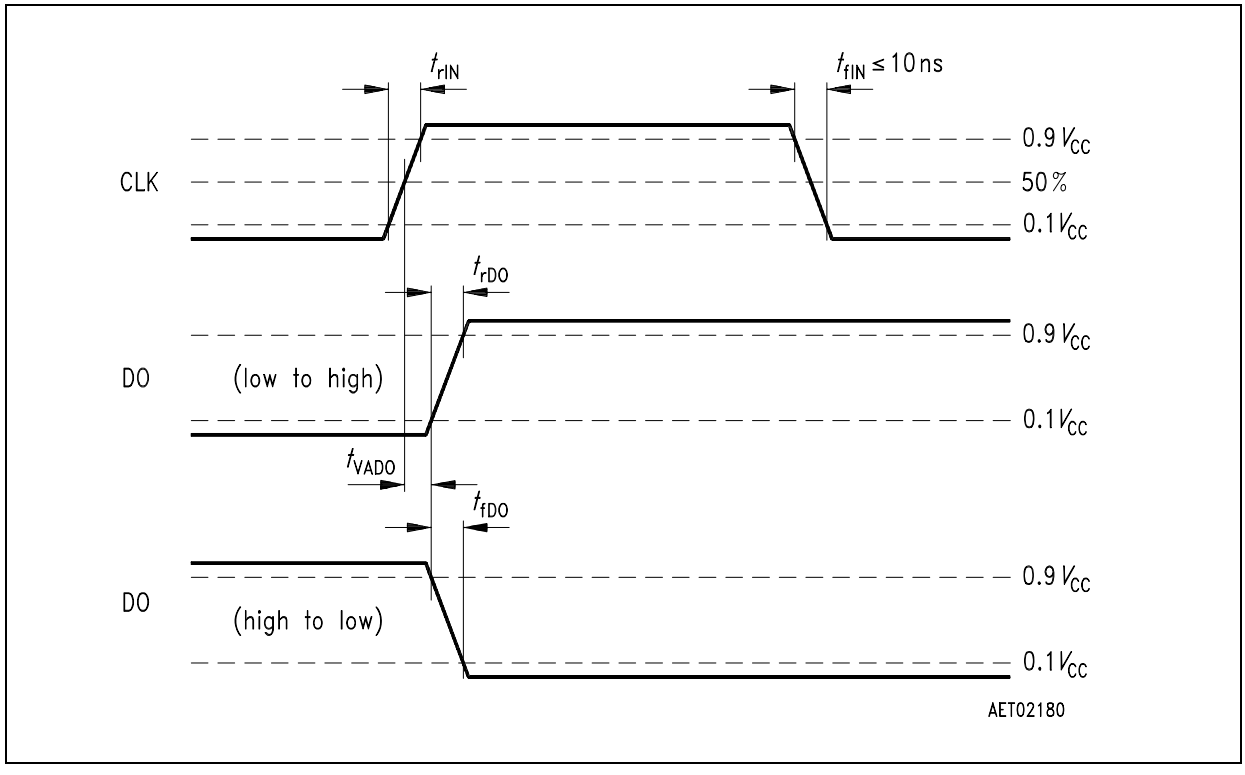

Figure 15 DO Valid Data Delay Time and Valid Time

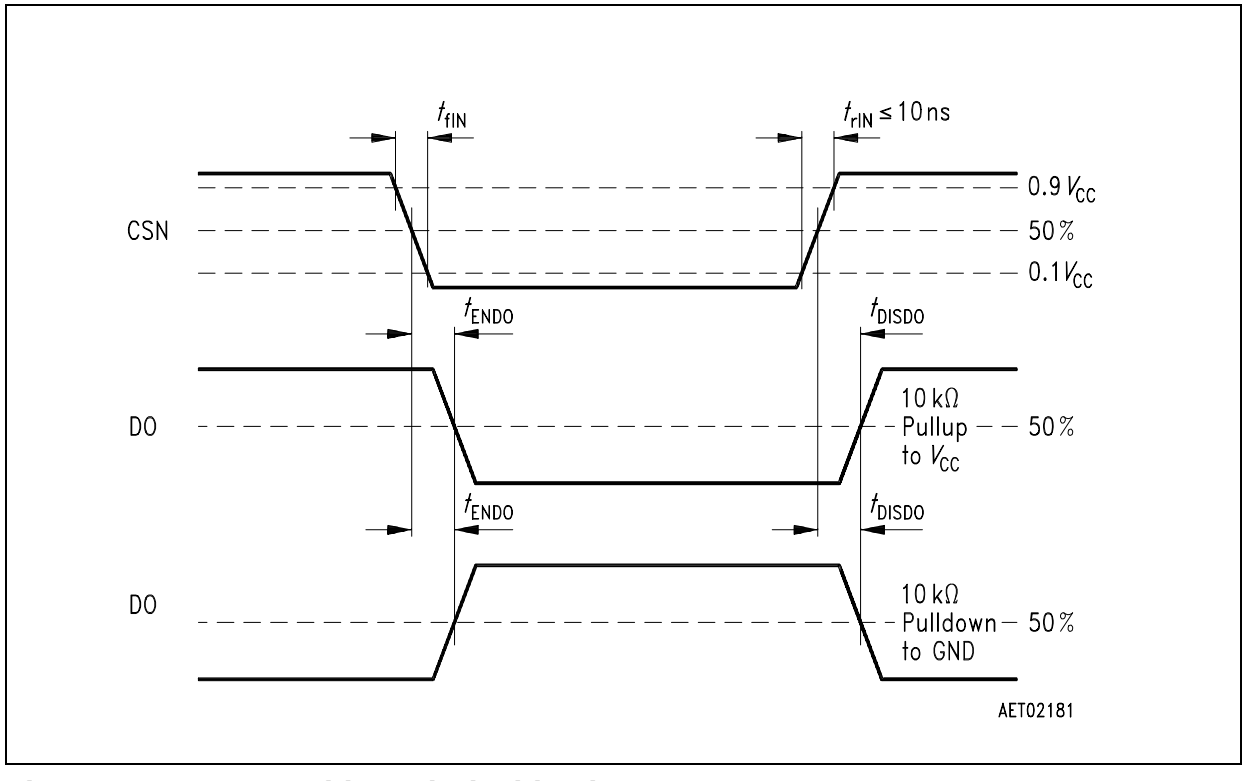

Figure 16 DO Enable and Disable Time

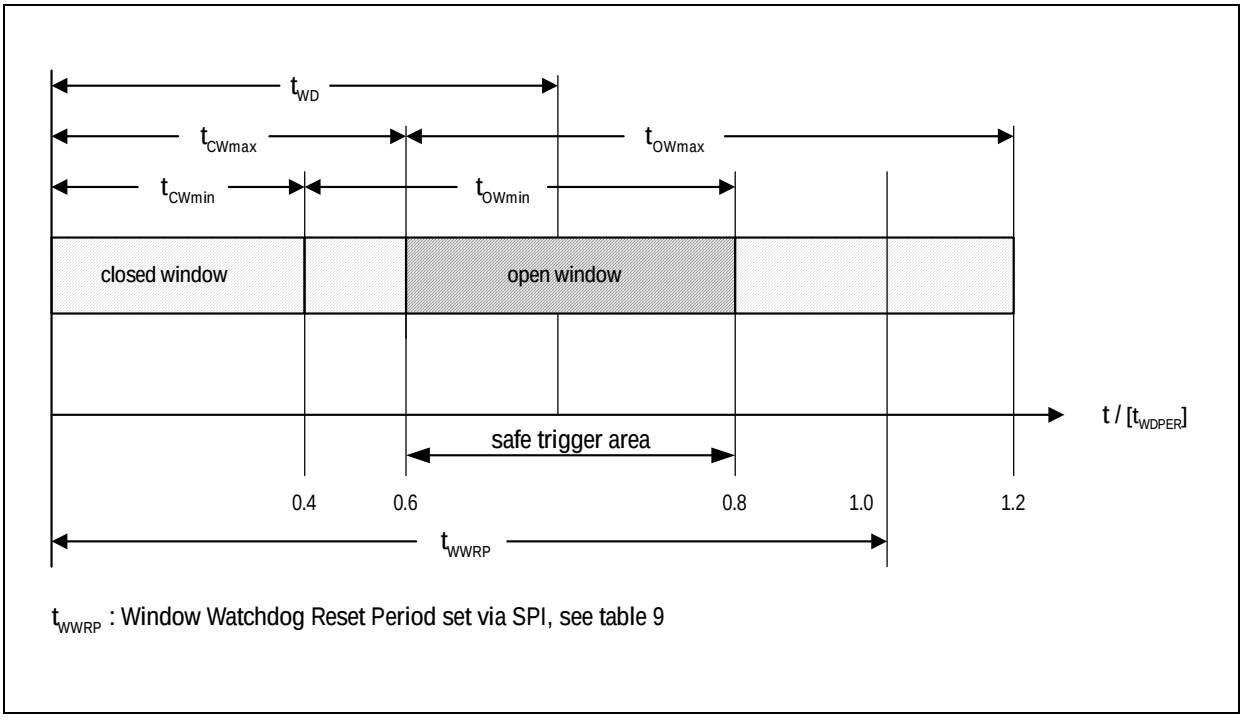

Figure 17 Watchdog Time-Out Definitions

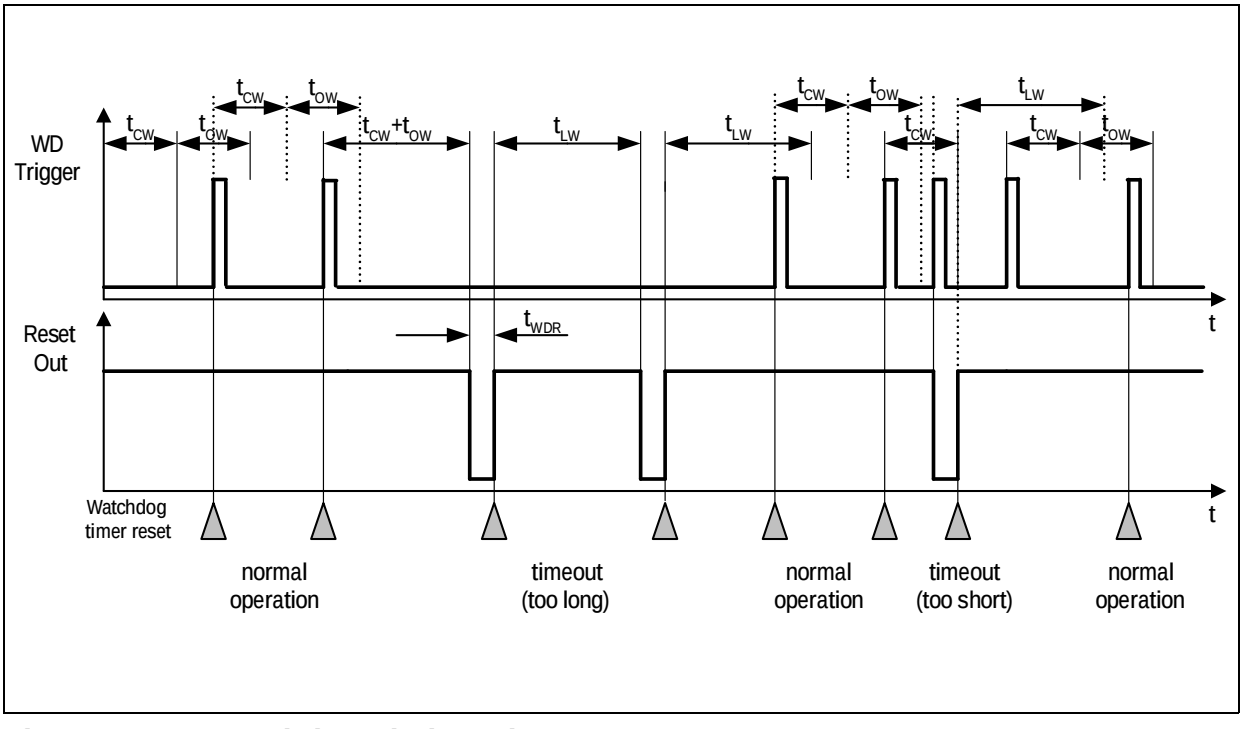

Figure 18 Watchdog Timing Diagram

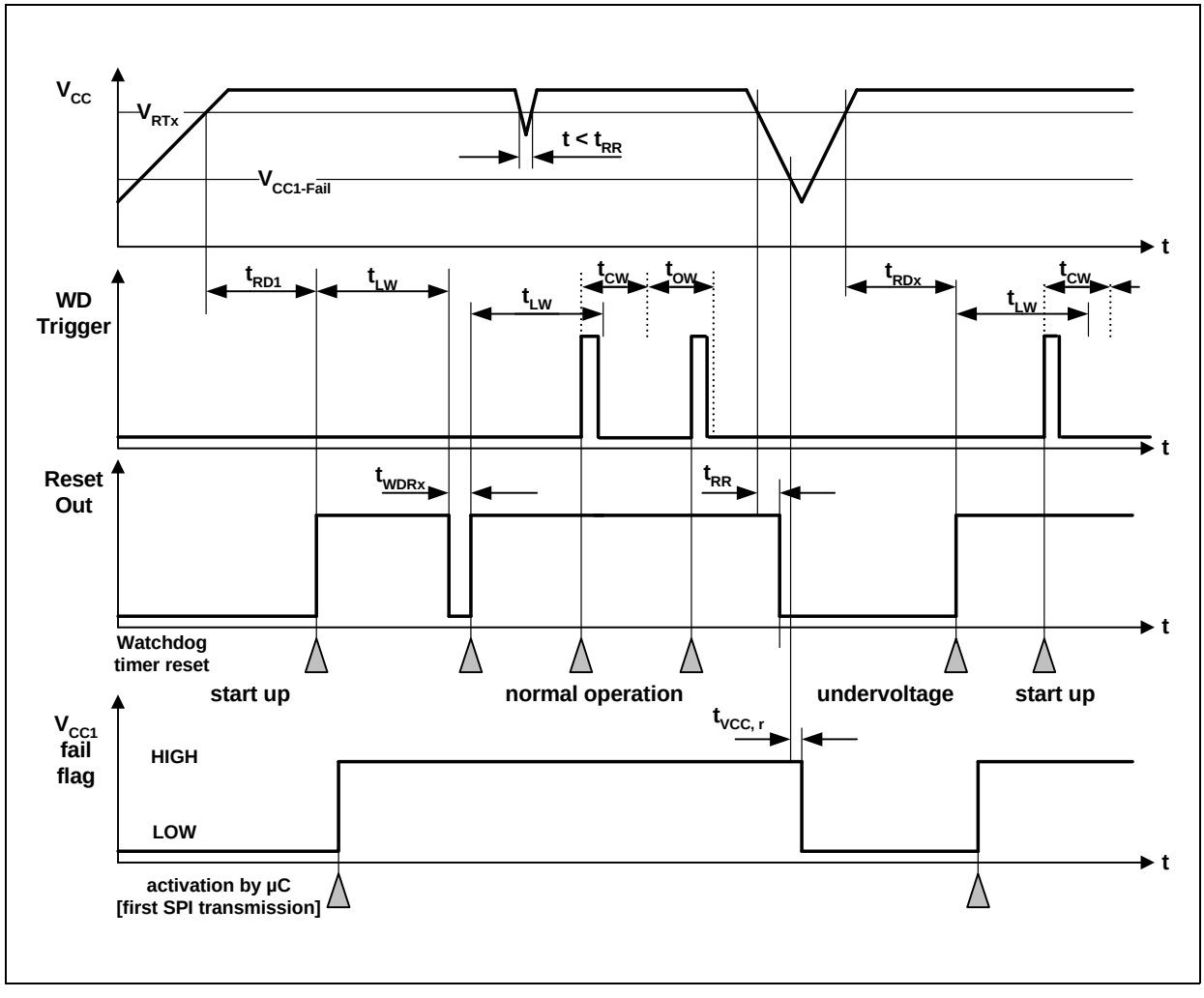

Figure 19 Reset Timing Diagram

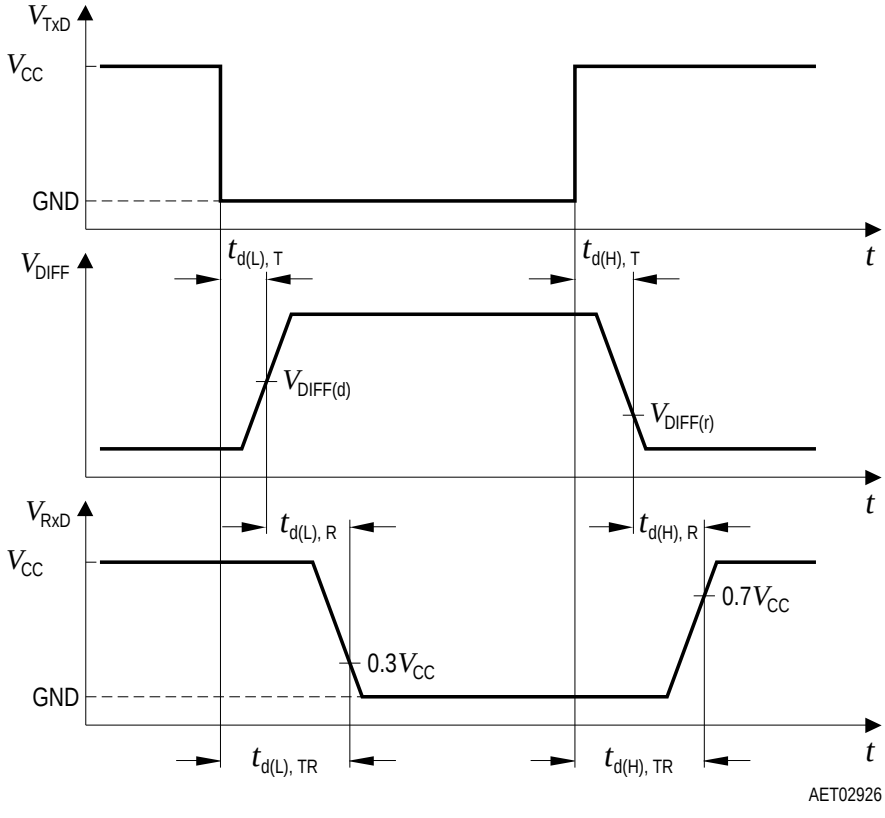

Figure 20 CAN Dynamic Characteristics Timing Diagram

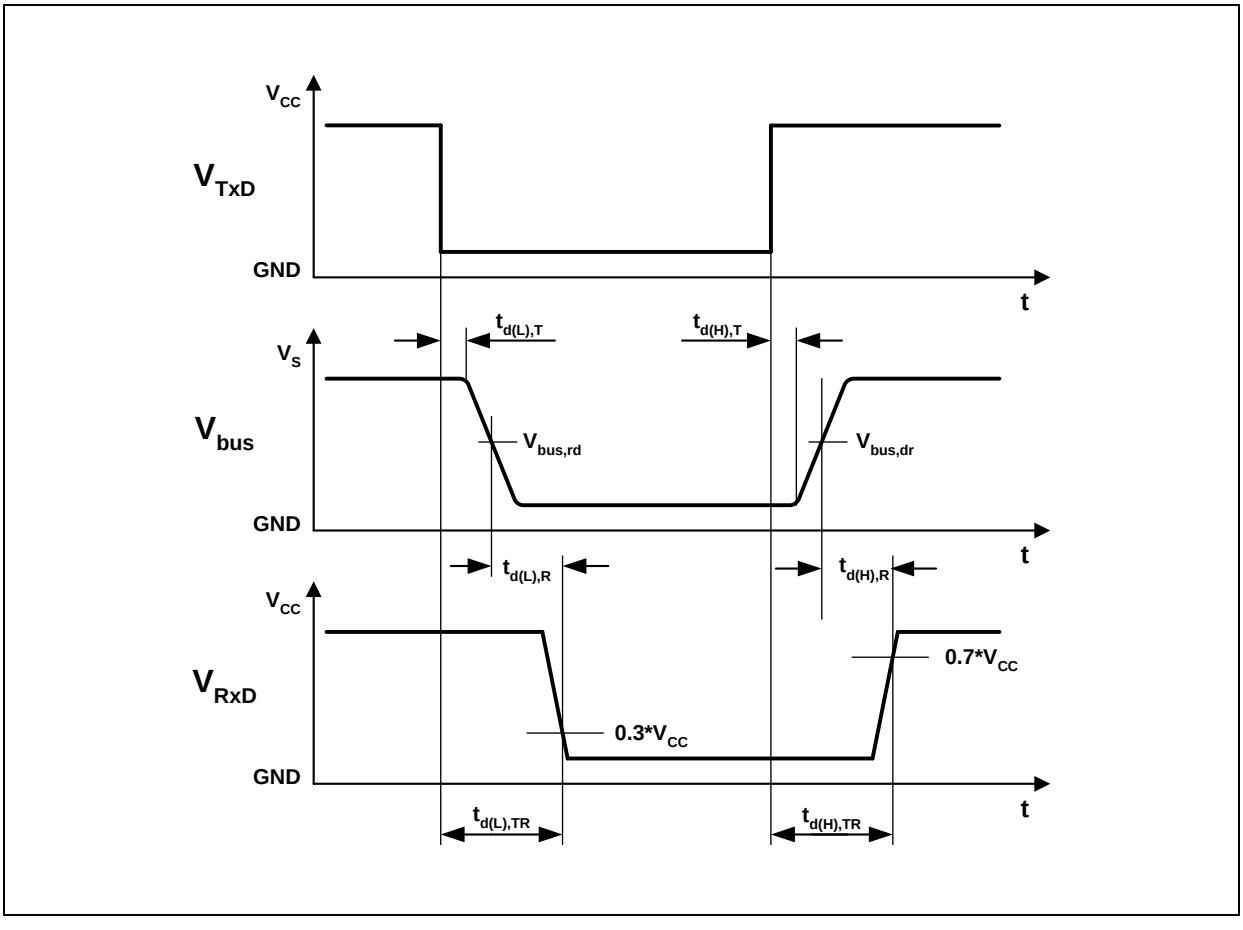

Figure 21 LIN Dynamic Characteristics Timing Diagram

7 Application Information

7.1 ESD Tests

Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) have been performed. The results and test condition are available in a test report.

Table 14 ESD “GUN test”

Performed Test	Result	Unit	Remarks
ESD at pin CANH, CANL, LIN, Vs versus GND	≥ +8	kV	[1)]Positive pulse
ESD at pin CANH, CANL, LIN, Vs versus GND	≤ -8	kV	[1)]Negative pulse

1) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3. (IEC 61000-4-2) - Tested by external test house (IBEE Zwickau, EMC Test report Nr. 11-11-06).

7.2 Application Example

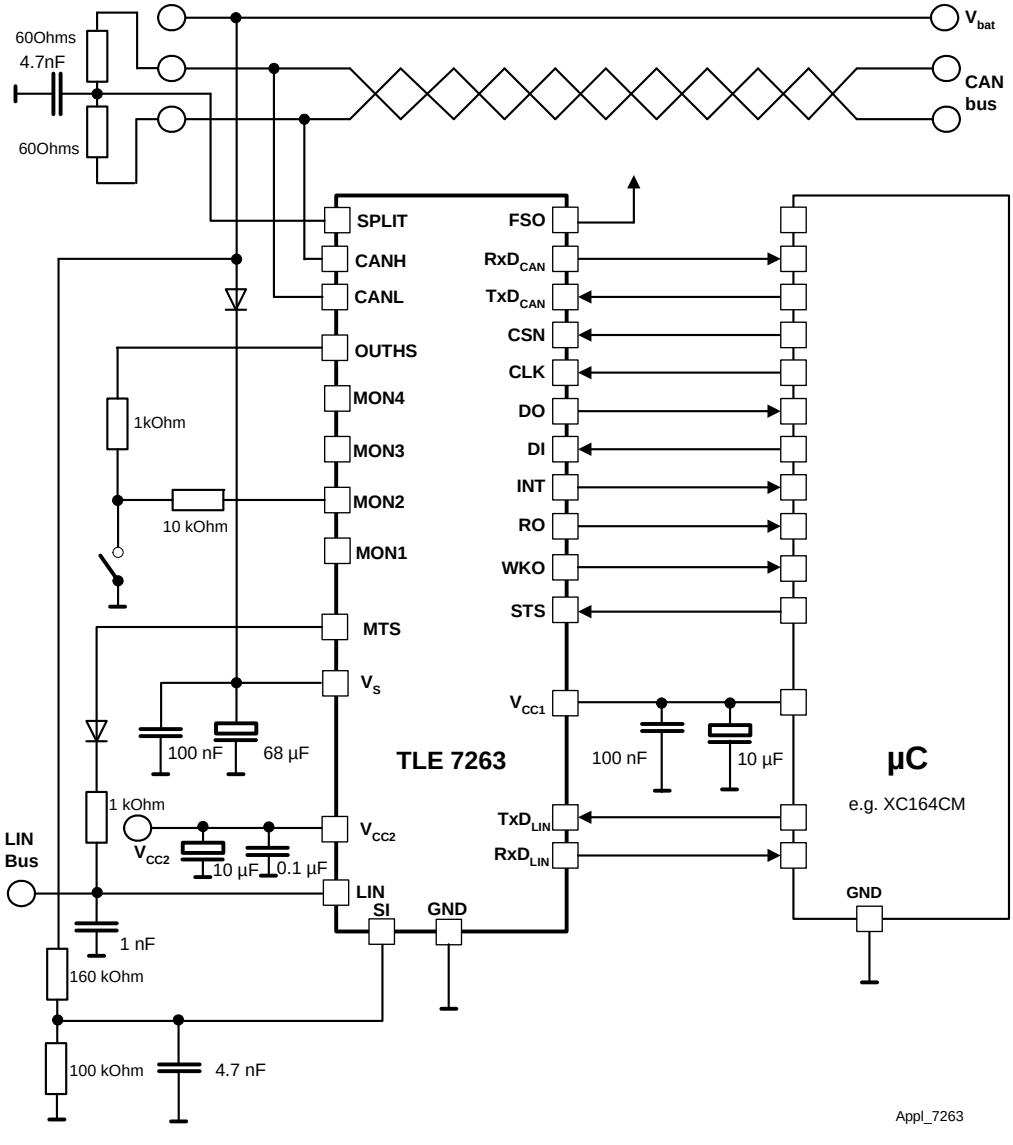

Figure 22 Application Circuit

8 Package Outlines

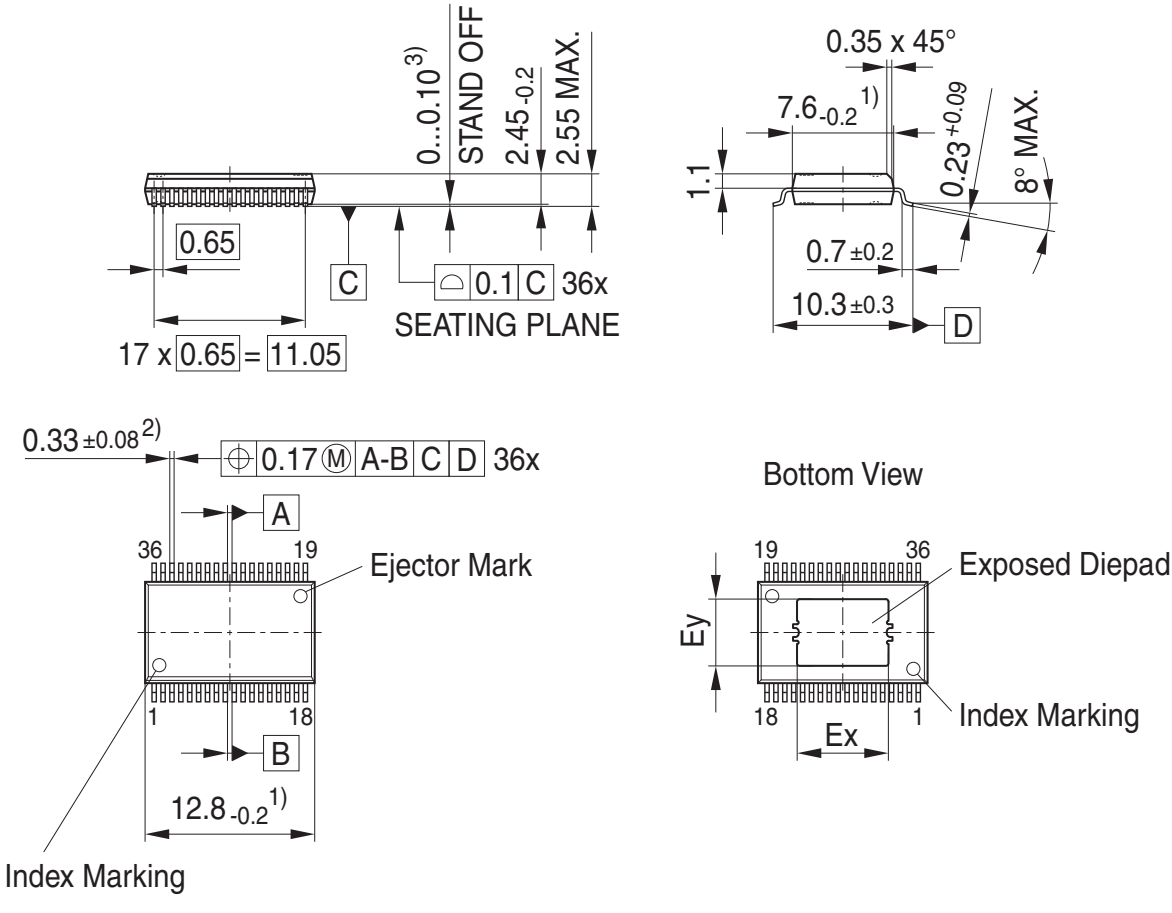

Figure 23 PG-DSO-36-53 (Plastic Dual Small Outline with Exposed Pad)

Green Product (RoHS Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/packages**. Dimensions in mm

9 Revision History

TLE 7263E

Revision History:	**2013-12-05**	Rev. 1.71
Previous Version:	Revision 1.70	
Page	Subjects (major changes since last revision)	
2	New package type: PG-DSO-36-53.	
Previous Version:	Revision 1.51	
Page	Subjects (major changes since last revision)	
2	LIN compatibility to LIN 2.1 and SAE J2602-2 added.	
35	Added additional line for Sense In threshold voltage, measured at 25°C	
41	Receiver Hysteresis: Parameter changed to specification of LIN 1.3	
43	LIN Leakage Current (first line): Test condition and parameter added according to specification of LIN1.3, 2.0 and LIN2.1	
44	Slope Symmetry: Test condition updated to specification LIN1.3.	
44	Slew Rate Falling Edge: Test condition changed to specification LIN1.3	
44	Slew Rate Rising Edge: Test condition changed to specification LIN1.3	
45	Propagation Delay: Test condition changed, tested at 20kbit/s according LIN1.3	
45	Transmitter Delay Symmetry: Test condition changed, tested at 20kbit/s according LIN1.3	
46	Slew Rate Rising and Falling Edge: Parameters for 10.4kBit/s removed	
60	Figure 23: Update of Package Outlines drawing with reduced max. stand-off	

Revision History

Revision History

Edition 2013-12-05

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