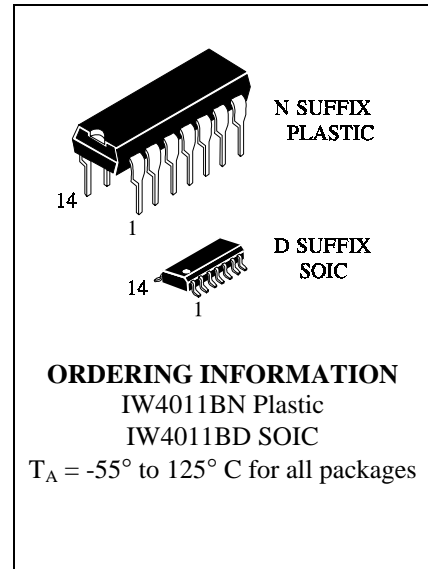


IW4011B

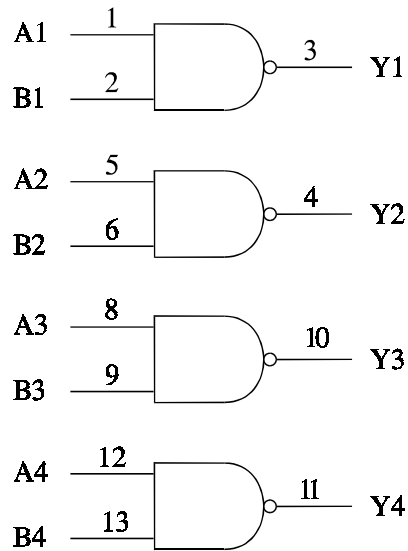
Quad 2-Input NAND Gate
High-Voltage Silicon-Gate CMOS

The IW4011B NAND gates provide the system designer with direct implementation of the NAND function.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

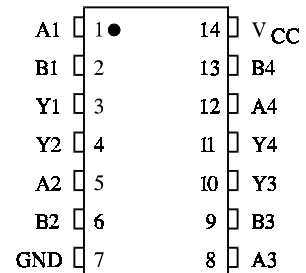


LOGIC DIAGRAM



PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +20 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±10 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| P _D | Power Dissipation per Output Transistor | 100 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 3.0 | 18 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).
Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|-------|------------|------|
| | | | | ≥-55°C | 25°C | ≤125 °C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.5 V or V _{CC} - 0.5 V | 5.0 | 3.5 | 3.5 | 3.5 | V |
| | | V _{OUT} =1.0 V or V _{CC} - 1.0 V | 10 | 7 | 7 | 7 | |
| | | V _{OUT} =1.5 V or V _{CC} - 1.5 V | 15 | 11 | 11 | 11 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} = V _{CC} - 0.5V | 5.0 | 1.5 | 1.5 | 1.5 | V |
| | | V _{OUT} = V _{CC} - 1.0 V | 10 | 3 | 3 | 3 | |
| | | V _{OUT} = V _{CC} - 1.5V | 15 | 4 | 4 | 4 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} =GND or V _{CC} | 5.0 | 4.95 | 4.95 | 4.95 | V |
| | | | 10 | 9.95 | 9.95 | 9.95 | |
| | | | 15 | 14.95 | 14.95 | 14.95 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{CC} | 5.0 | 0.05 | 0.05 | 0.05 | V |
| | | | 10 | 0.05 | 0.05 | 0.05 | |
| | | | 15 | 0.05 | 0.05 | 0.05 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = GND or V _{CC} | 18 | ±0.1 | ±0.1 | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} = GND or V _{CC} | 5.0 | 0.25 | 0.25 | 7.5 | μA |
| | | | 10 | 0.5 | 0.5 | 15 | |
| | | | 15 | 1.0 | 1.0 | 30 | |
| | | | 20 | 5.0 | 5.0 | 150 | |
| I _{OL} | Minimum Output Low (Sink) Current | V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V | 5.0 | 0.64 | 0.51 | 0.36 | mA |
| | | | 10 | 1.6 | 1.3 | 0.9 | |
| | | | 15 | 4.2 | 3.4 | 2.4 | |
| I _{OH} | Minimum Output High (Source) Current | V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V | 5.0 | -2.0 | -1.6 | -1.15 | mA |
| | | | 5.0 | -0.64 | -0.51 | -0.36 | |
| | | | 10 | -1.6 | -1.3 | -0.9 | |
| | | | 15 | -4.2 | -3.4 | -2.4 | |

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------------|--|----------------------|------------------|------------------|-------------------|------|
| | | | ≥-55°C | 25°C | ≤125°C | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Input A or B to Output Y (Figure 1) | 5.0 10 15 | 250 120 90 | 250 120 90 | 500 240 180 | ns |
| t_{TLH} , t_{THL} | Maximum Output Transition Time, Any Output (Figure 1) | 5.0 10 15 | 200 100 80 | 200 100 80 | 400 200 160 | ns |
| C_{IN} | Maximum Input Capacitance | - | | 7.5 | | pF |

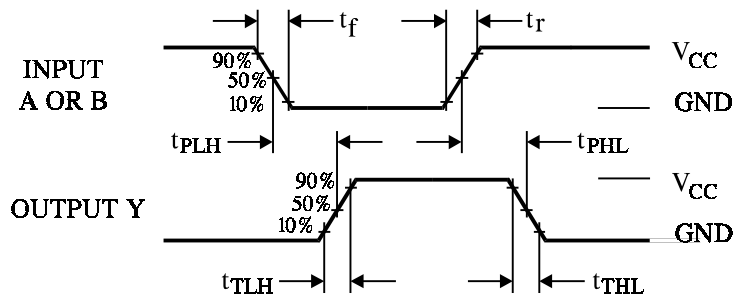
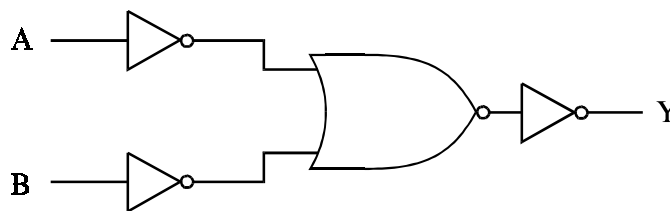


Figure 1. Switching Waveforms

**EXPANDED LOGIC DIAGRAM
(1/4 of the Device)**



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