ETC5064/64-X
ETC5067/67-X

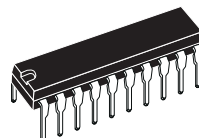## SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filter.
  - μ-law or A-law compatible CODER and DECODER.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
  - Receive push-pull power amplifiers.
- μ-LAW ETC5064
- A-LAW ETC5067
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS.
- ± 5 V OPERATION.
- LOW OPERATING POWER-TYPICALLY 70 mW
- POWER-DOWN STANDBY MODE-TYPICALLY 3 mW
- AUTOMATIC POWER DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- 0°C TO 70°C OPERATION: ETC5064/67
- –40°C TO 85°C OPERATION: ETC5064-X/67-X

DIP20
(Plastic) N

ORDERING NUMBERS:
ETC5064N
ETC5064N-X
ETC5067N
ETC5067N-X

PLCC20
FN

ORDERING NUMBERS:
ETC5064FN
ETC5064FN-X
ETC5067FN
ETC5067FN-X

SO20
D

ORDERING NUMBERS:
ETC5064D
ETC5064D-X
ETC5067D
ETC5067D-X

DESCRIPTION

The ETC5064 (μ-law), ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in the Block Diagrams and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

Similar to the ETC505X family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6 V across a balanced 600Ω load.
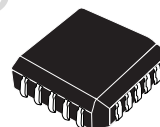
Also included is an Analog Loopback switch and $\overline{TS}_X$ output.

PIN CONNECTIONS (Top views)
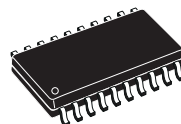
DIP20 & SO20

VPO+	1	20 VBB
GNDA	2	19 VFXI+
VPO-	3	18 VFXI-
VPI	4	17 GSX
VFRO	5	16 ANLB
VCC	6	15 TSX
FSR	7	14 FSX
DR	8	13 DX
BCLKR/CLKSEL	9	12 BCLKX
MCLKR/PDN	10	11 MCLKX

M90ETC50A67-01

PLCC20

Top pins: VPO- (3), GNDA (2), VPO+ (1), VBB (20), VFXI+ (19)

VPI	4	18 VFXI-
VFRO	5	17 GSX
VCC	6	16 ANLB
FSR	7	15 TSX
DR	8	14 FSX

Bottom pins: BCLKR/CLKSEL (9), MCLKR/PDN (10), MCLKX (11), BCLKX (12), DX (13)

M91ETC58A67-06
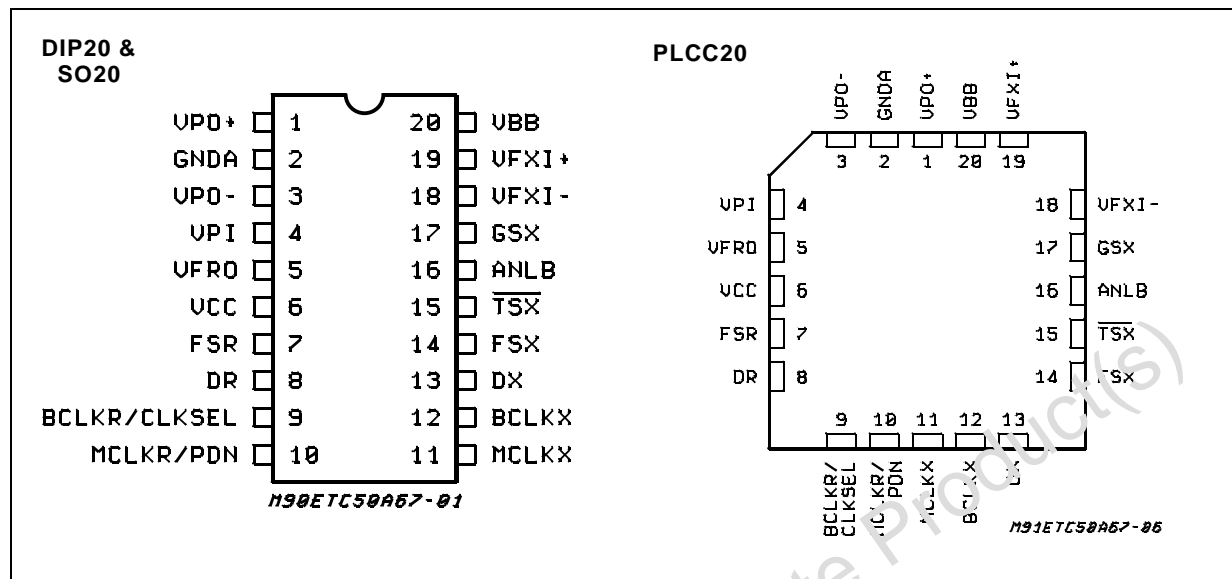
BLOCK DIAGRAM (ETC5064 - ETC5064-X - ETC5067 - ETC5067-X)

M91ETC50A67-02A
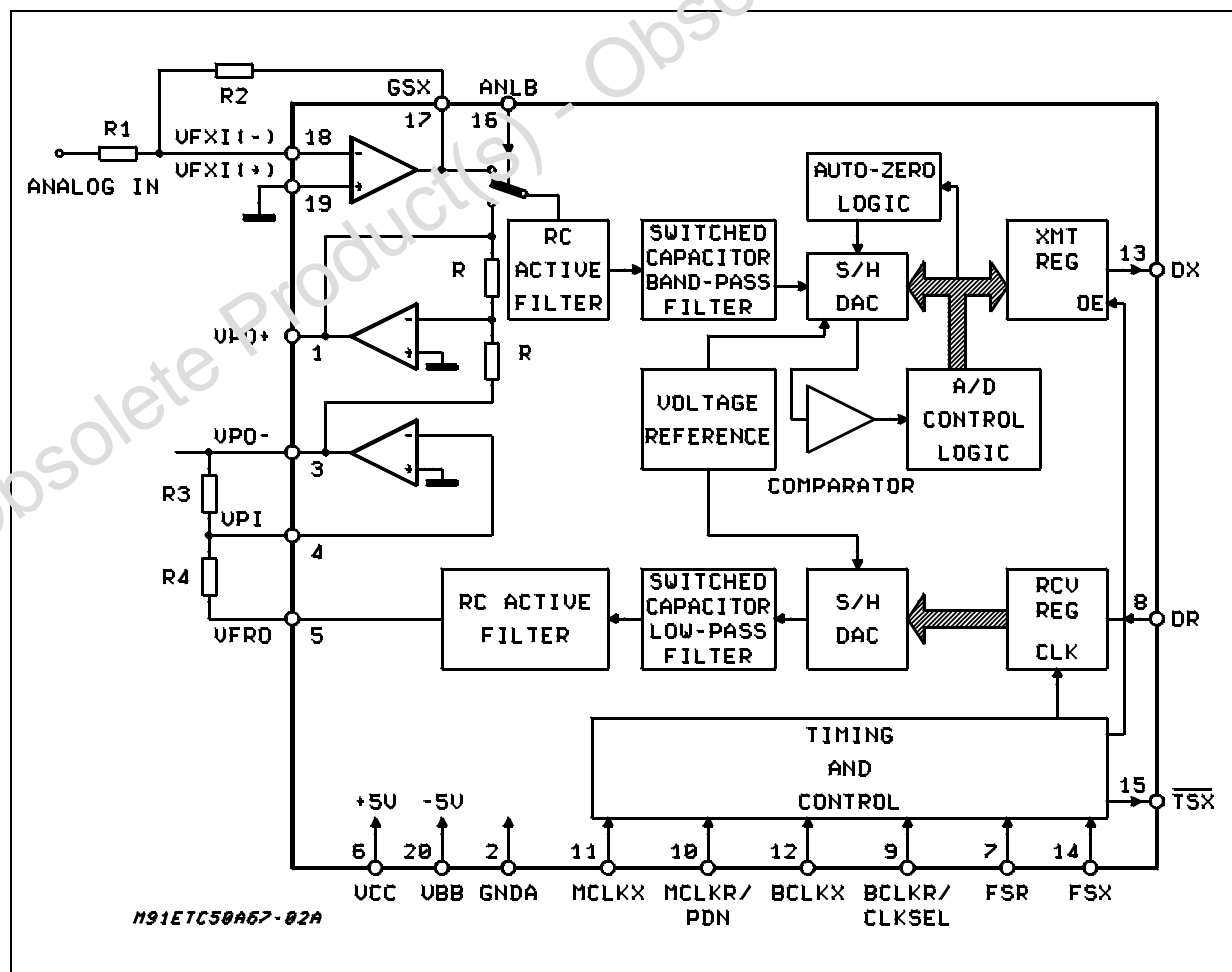
PIN DESCRIPTION

Name	Pin Type (*)	N	Description
VPO$^+$	O	1	The Non-inverting Output of the Receive Power Amplifier
GNDA	GND	2	Analog Ground. All signals are referenced to this pin.
VPO$^-$	O	3	The Inverting Output of the Receive Power Amplifier
VPI	I	4	Inverting Input to the Receive Power Amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF$_R$O	O	5	Analog Output of the Receive Filter.
V$_{CC}$	S	6	Positive Power Supply Pin. V_{CC} = +5V ±5%
FS$_R$	I	7	Receive Frame Sync Pulse which enable BCLK$_R$ to shift PCM data into D$_R$. FS$_R$ is an 8KHz pulse train. See figures 1 and 2 for timing details.
D$_R$	I	8	Receive Data Input. PCM data is shifted into D$_R$ following the FS$_R$ leading edge
BCLK$_R$/CLKSEL	I	9	The bit Clock which shifts data into D$_R$ after the FS$_R$ leading edge. May vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and BCLK$_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
MCKL$_R$/PDN	I	10	Receive Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with MCLK$_X$, but should be synchronous with MCLK$_X$ for best performance. When MCLK$_R$ is connected continuously low, MCLK$_X$ is selected for all internal timing. When MCLK$_R$ is connected continuously high, the device is powered down.
MCLK$_X$	I	11	Transmit Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with MCLK$_R$.
BCLK$_X$	I	12	The bit clock which shifts out the PCM data on D$_X$. May vary from 64KHz to 2.048MHz, but must be synchronous with MCLK$_X$.
D$_X$	O	13	The TRI-STATE®PCM data output which is enabled by FS$_X$.
FS$_X$	I	14	Transmit frame sync pulse input which enables BCLK$_X$ to shift out the PCM data on D$_X$. FS$_X$ is an 8KHz pulse train. See figures 1 and 2 for timing details.
$\overline{TS}_X$	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded if not used.
ANLB	I	16	Analog Loopback Control Input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO$^+$ output of the receive power amplifier.
GS$_X$	O	17	Analog output of the transmit input amplifier. Used to set gain externally.
VF$_X$I$^-$	I	18	Inverting input of the transmit input amplifier.
VF$_X$I$^+$	I	19	Non-inverting input of the transmit input amplifier.
V$_{BB}$	S	20	Negative Power Supply Pin. V_{BB} = -5V ±5%

(*) I: Input, O: Output, S: Power Supply.
TRI-STATE® is a trademark of National Semiconductor Corp.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R/PDN$ pin and FS_X and/or FS_R pulses must be present. Thus 2 power-down control modes are available. The first is to pull the $MCLK_R/PDN$ pin high; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R/PDN$ pin can be used as a power-down control. A low level on $MCLK_R/PDN$ powers up the device and a high level powers down the device. In either case, $MCLKX$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCL_R/CLKSEL$ can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R/CKSEL$ pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R/CLKSEL$. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1: Selection of Master Clock Frequencies.

BCLKR/CLKSEL	Master Clock Frequency Selected	
	ETC5067 ETC5067-X	ETC5064 ETC5064-X
Clocked	2.048MHz	1.536MHz or 1.544MHz
0	1.536MHz or 1.544MHz	2.048MHz
1 (or open circuit)	2.048MHz	1.536MHz or 1.544MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shift out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRISTATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or on $BCKL_R$ if running). FS_X and FS_R must be synchronous with $MCLKX/R$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5067 or 1.536 MHz, 1.544 MHz for the ETC5064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R/PDN$ pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses. FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 2. With FS_X high during a falling edge of $BCLK_R$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on the transmit frame sync FS_X, the device will sense whether short or long frame sync

pulses are being used. For 64 kHz operation, the frame sync pulses must be kept low for a minimum of 160 ns (see Fig 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_x$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 4. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067 and ETC5067-X) or μ-law (ETC5064 and ETC5064-X) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filer output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. the total encoding delay will be approximately 165 μs (due to the transmit filter, plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consist of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256kHz. The decoder is A-law (ETC5067 and ETC5067-X) or μ–law (ETC5064 and ETC5064-X) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600Ω load to a level of 7.2dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCKL_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is about10μs (decoder up-date) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5V peak output signal from the receive filter up ± 3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6dB of signal gain for balanced loads. Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$: 1 turns ratio, as shown in figure 4. A total peak power of 15.6dBm can be delivered to the load plus termination. Both power amplifier can be powered down independently from the PDN input by connecting the VPI input to V_{BB} saving approximately 12 mW of power.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	-7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} +0.3 to V_{BB} -0.3	V
	Voltage at any Digital Input or Output	V_{CC} +0.3 to GNDA -0.3	V
T_{oper}	Operating Temperature Range: **ETC5064/67**	-25 to +125	°C
	ETC5064-X/67-X	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5.0V ±5%, V_{BB} = -5V ±5%, GNDA = 0V, T_A = 0°C to 70°C (ETC5064-X/67-X: T_A = −40°C to 85°), unless otherwise noted; typical characteristics specified at V_{CC} = 5.0V, V_{BB} =-5.0V, T_A = 25°C; all signals are referenced to GNDA.

DIGITAL INTERFACE (All devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage I_L = 3.2 mA I_L = 3.2 mA, Open Drain	D_X TS_X			0.4 0.4	V V
V_{OH}	Output High Voltage IH = 3.2 mA	D_X	2.4			V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL})all digital inputs Except $BCLK_R$		− 10		0	μA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) Except ANLB		− 10		10	μA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
$I_I XA$	Input Leakage Current (− 2.5 V ≤ V ≤ + 2.5 V)	$VFxI^+$ or $VFxI^-$	− 200		200	nA
$R_I XA$	Input Resistance (− 2.5 V ≤ V ≤ + 2.5 V)	$VFxI^+$ or $VFxI^-$	10			MΩ
$R_O XA$	Output Resistance (closed loop, unity gain)			1	3	Ω
$R_L XA$	Load Resistance	GS_X	10			kΩ
$C_L XA$	Load Capacitance	GS_X			50	pF
$V_O XA$	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	− 2.8		+2.8	V
$A_V XA$	Voltage Gain ($VFxI^+$ to GS_X)		5000			V/V
$F_U XA$	Unity Gain Bandwidth		1	2		MHz
$V_{OS} XA$	Offset Voltage		− 20		20	mV
$V_{CM} XA$	Common-mode Voltage		− 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
$R_O RF$	Output Resistance	$VF_R O$		1	3	Ω
$R_L RF$	Load Resistance ($VF_R O$ = ± 2.5 V)		10			kΩ
$C_L RF$	Load Capacitance				25	pF
$VOS_R O$	Output DC Offset Voltage		− 200		200	mV

ELECTRICAL OPERATING CHARACTERISTICS (Continued)

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (-1.0 V $\leq$ VPI ≤ 1.0 V)	-100		100	nA
RIPI	Input Resistance ($-1.0 \leq$ VPI ≤ 1.0 V)	10			MΩ
VIOS	Input Offset Voltage	-25		25	mV
ROP	Output Resistance (inverting unity–gain at VPO$^+$ or VPO$^-$)		1		Ω
F_C	Unity–gain Bandwidth, Open Loop (VPO$^-$)		400		kHz
C_LP	Load Capacitance (VPO$^+$ or VPO$^-$ to GNDA) $R_L \geq 1500$ Ω $R_L = 600$ Ω $R_L = 300$ Ω			100 500 1000	pF
GAp$^+$	Gain VPO$^-$ to VPO$^+$ to GNDA, Level at VPO$^-$ = 1. 77 Vrms (+ 3 dBmO)		-1		V/V
PSRRp	Power Supply Rejection of V_{CC} or V_{BB} (VPO$^-$ connected to VPI) 0 kHz – 4 kHz 0 kHz – 50 kHz	50 36			dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current at **ETC6064/67** **ETC5064-X/67-X**		0.5 0.5	1.5	mA mA
$I_{BB}0$	Power-down Current at **ETC6064/67** **ETC5064-X/67-X**		0.05 0.05	0.3 0.4	mA mA
$I_{CC}1$	Active Current at **ETC6064/67** **ETC5064-X/67-X**		7.0 7.0	10.0 12.0	mA mA
$I_{BB}1$	Active Current at **ETC6064/67** **ETC5064-X/67-X**		7.0 7.0	10.0 12.0	mA mA

ETC5064 - ETC5064-X - ETC5067 - ETC5067-X

All TIMING SPECIFICATIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks MCLK$_X$ and MCLK$_R$ Depends on the device used and the BCLK$_R$/CLKSEL Pin			1.536 2.048 1.544		MHz
t_{WMH}	Width of Master Clock High	MCLK$_X$ and MCLK$_R$	160			ns
t_{WML}	Width of Master Clock Low	MCLK$_X$ and MCLK$_R$	160			ns
t_{RM}	Rise Time of Master Clock	MCLK$_X$ and MCLK$_R$			50	ns
t_{FM}	Fall Time of Master Clock	MCLK$_X$ and MCLK$_R$			50	ns
t_{PB}	Period of Bit Clock		485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)		160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)		160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)				50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)				50	ns
t_{SBFM}	Set-up time from BCLK$_X$ high to MCLK$_X$ falling edge. (first bit clock after the leading edge of FS$_X$)		100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)		0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)		80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS$_X$ or FS$_R$		100			ns
t_{DZF}	Delay Time to valid data from FS$_X$ or BCLK$_X$, whichever comes later and delay time from FSX to data output disabled (C_L = 0 pF to 150 pF)		20		165	ns
t_{DBD}	Delay Time from BCLK$_X$ high to data valid (load = 150 pF plus 2 LSTTL loads)		0		150	ns
t_{DZC}	Delay Time from BCLK$_X$ low to data output disabled		50		165	ns
t_{SDB}	Set-up Time from D$_R$ valid to BCLK$_{R/X}$ low		50			ns
t_{HBD}	Hold Time from BCLK$_{R/X}$ low to D$_R$ invalid		50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)		0			ns
t_{SF}	Set-up Time from FS$_{X/R}$ to BCLK$_{X/R}$ Low (short frame sync pulse) - Note 1		80			ns
t_{HF}	Hold Time from BCLK$_{X/R}$ Low to FS$_{X/R}$ Low (short frame sync pulse) - Note 1		100			ns
t_{XDF}	Delay Time to TS$_X$ low (load = 150 pF plus 2 LSTTI loads)				140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 bit/s operating mode)		160			ns

Note : 1.For short frame sync timing. FS$_X$ and FS$_R$ must go high while their respective bit clocks are high.

Figure 1 : 64 k bits/s TIMING DIAGRAM. (see next page for complete timing)
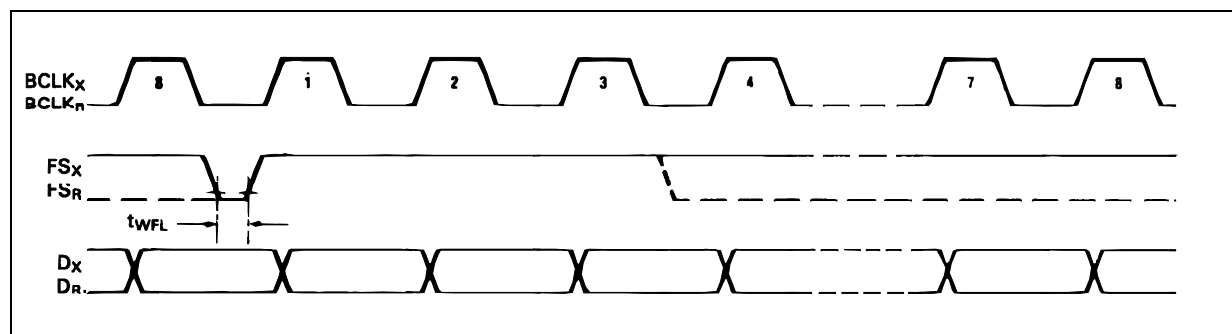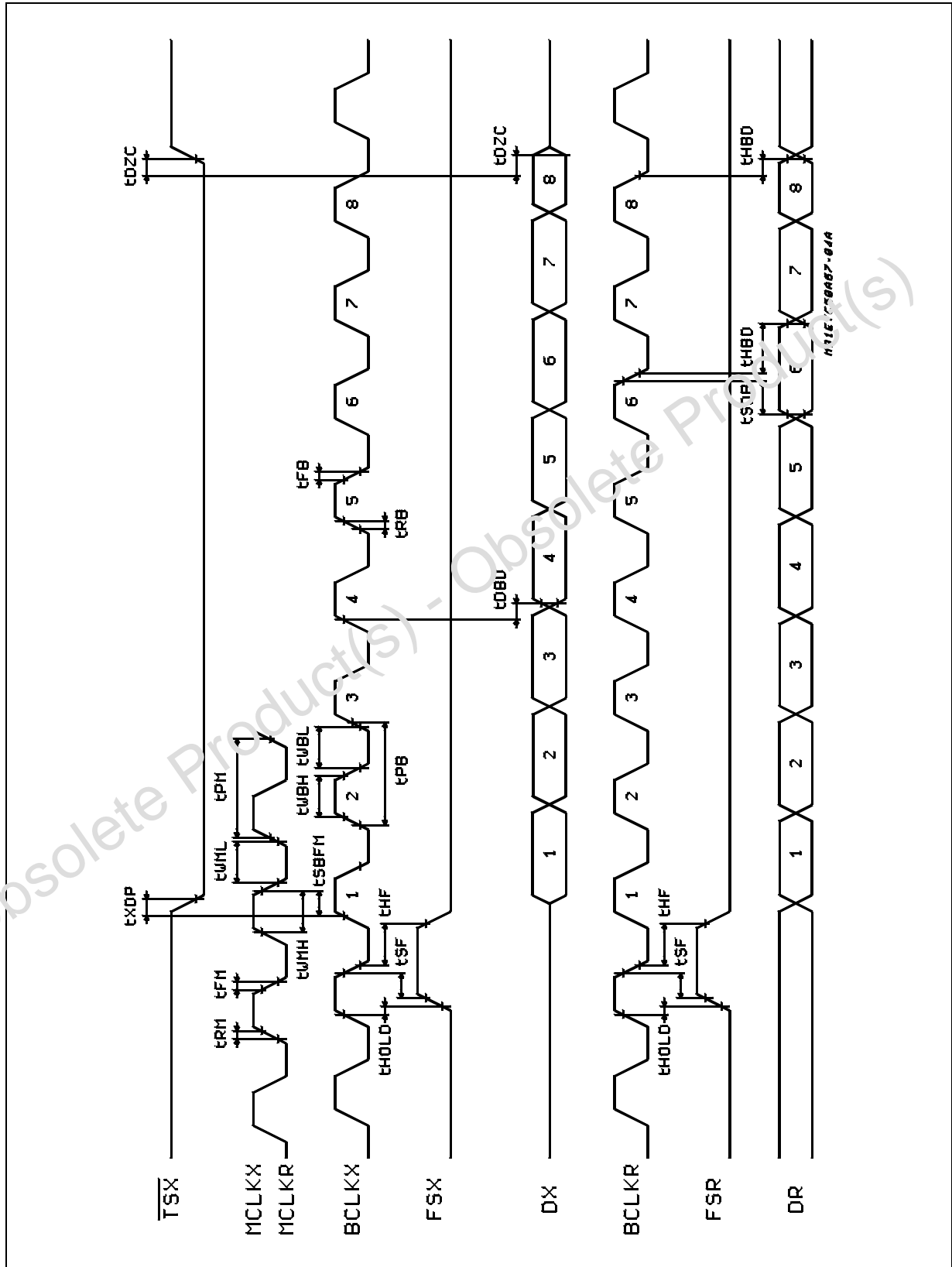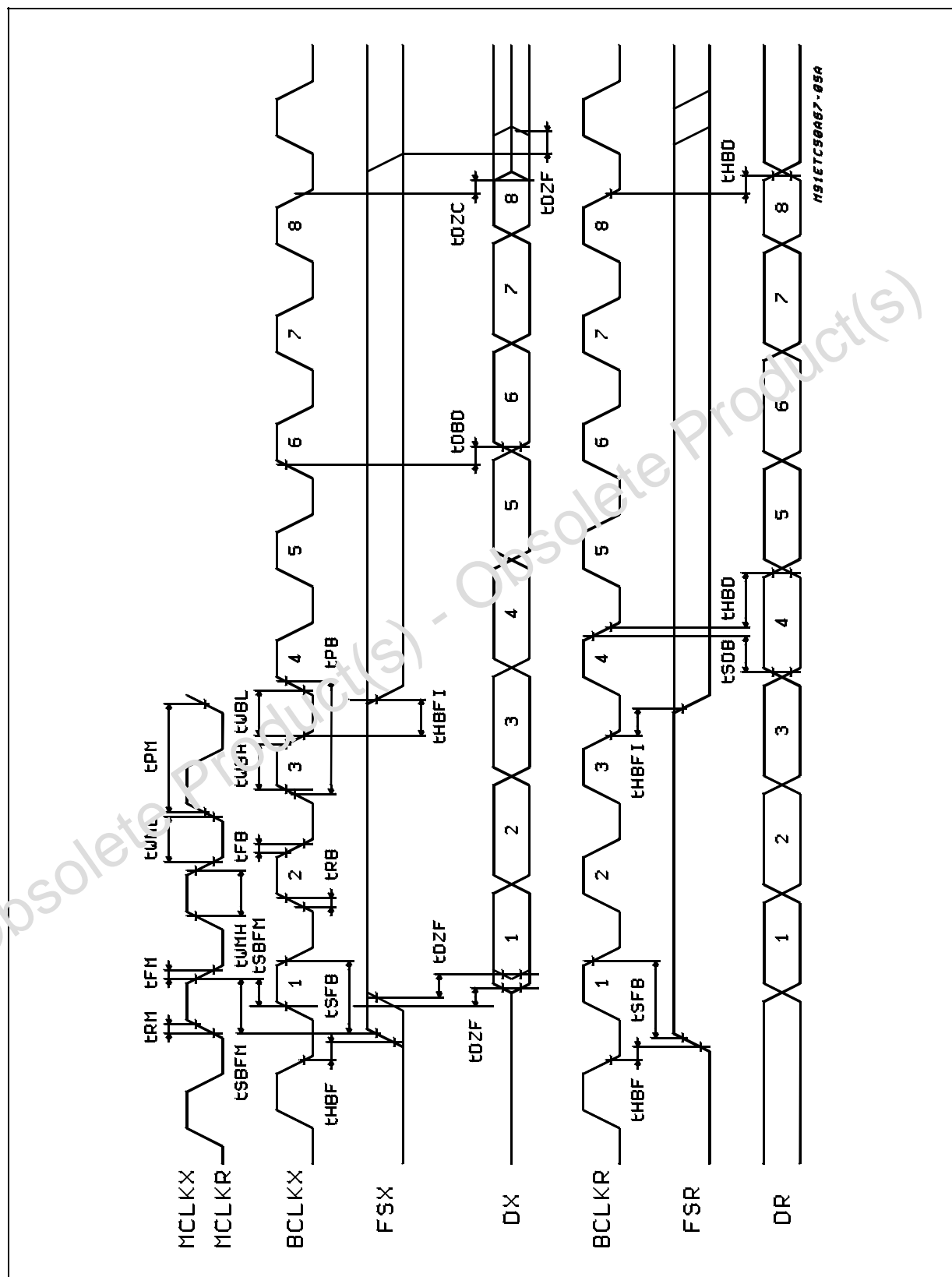
Figure 2 : Short Frame Sync Timing.

Figure 3 : Long Frame Sync Timing.

TRANSMISSION CHARACTERISTICS

(all devices) T_A = 0°C to 70°C (ETC5064-X/67-X: T_A = –40°C to 85°), V_{CC} = 5V ± 5%, V_{BB} = – 5V ± 5%, GNDA = 0V, f = 1.02kHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity–gain non–inverting. (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels - Nominal 0 dBm0 is 4 dBm (600Ω). 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 **ETC5067** 3.17 dBm0 **ETC5064**		2.492 2.501		VPK
G_{XA}	Transmit Gain, Absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = -5V) Input at GS_X = 0dBm0 at 1020Hz	-0.15		0.15	dB
GXR	Transmit Gain, Relative to GXA f = 16Hz f = 50Hz f = 60Hz f = 180Hz f = 200Hz f = 300Hz -3000Hz f = 3200Hz (ETC5064-X/67-X) f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	- - - -2.0 -1.8 -0.15 -0.35 -0.35 -0.7 		-40 -30 -26 -0.2 -0.1 0.15 0.20 0.05 0 -14 -32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature T_A = 0°C to +70°C T_A = –40°C to +85°C (ETC5064-X/67-X)	-0.1 -0.15		0.1 0.15	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5V ±5%, V_{BB} = 5V ±5%)	-0.05		0.05	dB
G_{XRL}	Transmit Gain Variation with Level Sinusolidal Test Method Reference Level = -10dBm0 VF_XI^+ = -40dBm0 to +3dBm0 VF_XI^+ = -50dBm0 to -40dBm0 VF_XI^+ = -55dBm0 to -50dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = -5V) Input = Digital Code Sequence for 0dBm0 Signal at 1020Hz	-0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f = 0Hz to 3000Hz f = 3200Hz (ETC5064-X/67-X) f = 3300Hz f = 3400Hz f = 4000Hz	-0.15 -0.35 -0.35 -0.7 		0.15 0.20 0.05 0 -14	dB
G_{RAT}	Absolute Receive Gain Variation with Temeperature T_A = 0°C to +70°C T_A = –40°C to +85°C (ETC5064-X/67-X)	-0.1 -0.15		0.1 0.15	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5V ±5%, V_{BB} = -5V ±5%)	-0.05		0.05	dB
G_{RRL}	Receive Gain Variation with Level Sinusoidal Test Method; Reference Input PCM code corresponds to an ideally encoded -10dBm0 signal PCM level = -40dBm0 to +3dBm0 PCM level = -50dBm0 to -40dBm0 PCM level = -55dBm0 to -50dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
V_{RO}	Receive Filter Output at VF_RO R_L = 10KΩ	-2.5		2.5	V

TRANSMISSION CHARACTERISTICS (continued)**.**
ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA} f = 500 Hz-600 Hz f = 600 Hz-800 Hz f = 800 Hz-1000 Hz f = 1000 Hz-1600 Hz f = 1600 Hz-2600Hz f = 2600 Hz-2800 Hz f = 2800 Hz-3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	µs
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA} f = 500 Hz-1000 Hz f = 1000 Hz-1600 Hz f = 1600 Hz-2600 Hz f = 2600 Hz-2800 Hz f = 2800 Hz-3000 Hz	− 40 − 30	− 25 − 20 70 100 145	90 125 175	µs

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message (A-LAW, VF_XI^+ = 0 V, Weighted 1) **ETC5064** **ETC5064-X**		 − 74 − 74	 − 69 − 67	 dBm0p dBm0p
N_{RP}	Receive Noise, P Message Weighted (A-LAW, PCM Code Equals Positive Zero)		− 82	− 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted (µ-LAW, VF_xI^+ = 0 V) **ETC5064** **ETC5064-X**		12 12	15 16	dBrnC0 dBrnC0
N_{RC}	Receive Noise, C Message Weighted (µ-LAW. PCM Code Equals Alternating Positive and Negative Zero)		8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, VF_XI^+ = 0 V			− 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms) f = 0 Hz-4000Hz A LAW µ LAW f = 4 kHz-25 kHz f = 25 kHz-50 kHz	 40 40 40 36			 dBp dBc dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = − 5.0 V_{DC} + 100 mVrms) f = 0 Hz-4000Hz A LAW µ LAW f = 4 kHz-25 kHz f = 25 kHz-50 kHz	 40 40 40 36			 dBp dBc dB dB
SOS	Spurious out-of-band Signals at the Channel Output 0 dBm0, 300 Hz-3400 Hz input PCM applied at D_R 4600 Hz-7600 Hz 7600 Hz-8400 Hz 8400 Hz-100,000 Hz			 −32 −40 −32	 dB dB dB

TRANSMISSION CHARACTERISTICS (continued).

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit

STD$_X$ or STD$_R$	Signal to Total Distortion (sinusoidal test method)
	
	Transmit or Receive Half-channel
	Level = 3.0 dBm0
	= 0 dBm0 to − 30 dBm0
	= − 40 dBm0 XMT
	                  RCV
	= − 55 dBm0 XMT
	                  RCV
		
		33
		36
		29
		30
		14
		15
					dBp (ALAW)
					
					dBc (µLAW)

SFD$_X$	Single Frequency Distortion, Transmit (T$_A$ = 25°C)			− 46	dB
SFD$_R$	Single Frequency Distortion, Receive (T$_A$ = 25°C)			− 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF$_X$I$^+$ = − 4 dBm0 to − 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz			− 41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT$_{X-R}$	Transmit to Receive Crosstalk, 0dBm0 Transmit f = 300 Hz-3400 Hz, D$_R$ = Steady PCM Code **ETC5064/67** **ETC5064-X/67-X**		− 90	− 75 − 65	dB dB
CT$_{R-X}$	Receive to Transmit Crosstalk, 0dBm0 Receive Level (note 2) f = 300 Hz-3400 Hz, VF$_X$I = 0 V **ETC5064/67** **ETC5064-X/67-X**		− 90	− 70 − 65	dB dB

POWER AMPLIFIERS

| Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{OL}$	Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range 10 dBm0 to + 3 dBm0 (balanced load, R$_L$ connected between VPO$^+$ and VPO$^-$) R$_L$ = 600 Ω R$_L$ = 1200 Ω R$_L$ = 30 kΩ	 33 3.5 4.0			Vrms
S/D$_P$	Signal/Distortion R$_L$ = 600 Ω, 0 dBm0	50			dB

Notes : 1. Measured by extrapolation from the distortion test results.
2. PPSRX, NPSRX, CTR−X measured with a −50dBm0 activating signal applied at VF$_X$I$^+$

ENCODING FORMAT AT D$_X$ OUTPUT

	A-Law (Including even bit inversion)	µLaw
V$_{IN}$ (at GS$_X$) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V$_{IN}$ (at GS$_X$) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V$_{IN}$ (at GS$_X$) = − Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

While the pins at the ETC506X family are well protected against electrical misure, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1μF supply decoupling capacitors should be connected from this common ground point to VCC and VBB as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to VCC and VBB with 10μF capacitors.

Figure 4 : Typical Asynchronous Application.

Note 1 : Transmit gain $= 20 \times \log \left(\dfrac{R1 + R2}{R2} \right)$, $(R1 + R2) \geqslant 10 \text{ k}\Omega$

Note 2 : Receive gain $= 20 \times \log \left(\dfrac{2 \times R3}{R4} \right)$, $R4 \geqslant 10 \text{ k}\Omega$

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

OUTLINE AND MECHANICAL DATA

SO20

SO20MEC
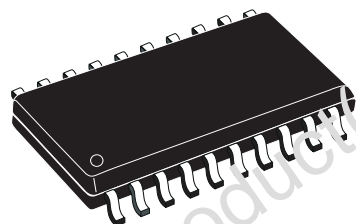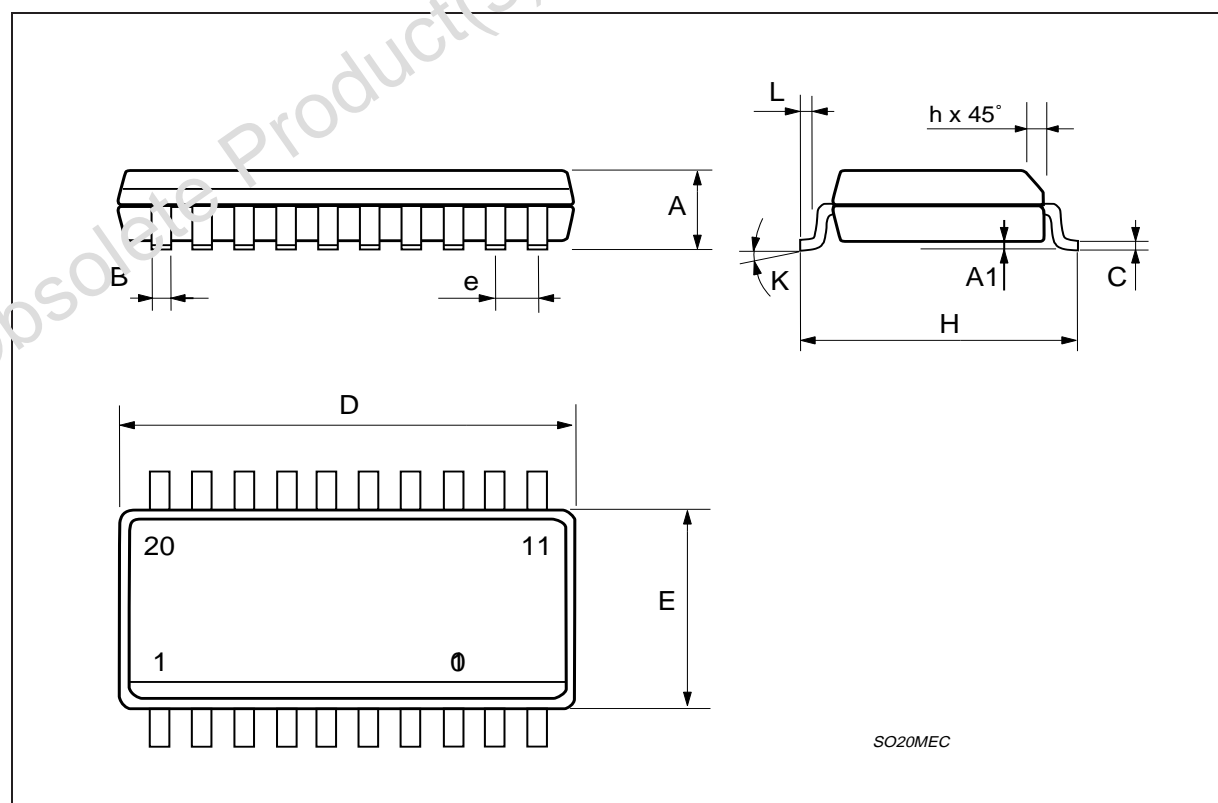
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

OUTLINE AND MECHANICAL DATA

PLCC20

PLCC20ME

G (Seating Plane Coplanarity)
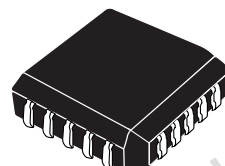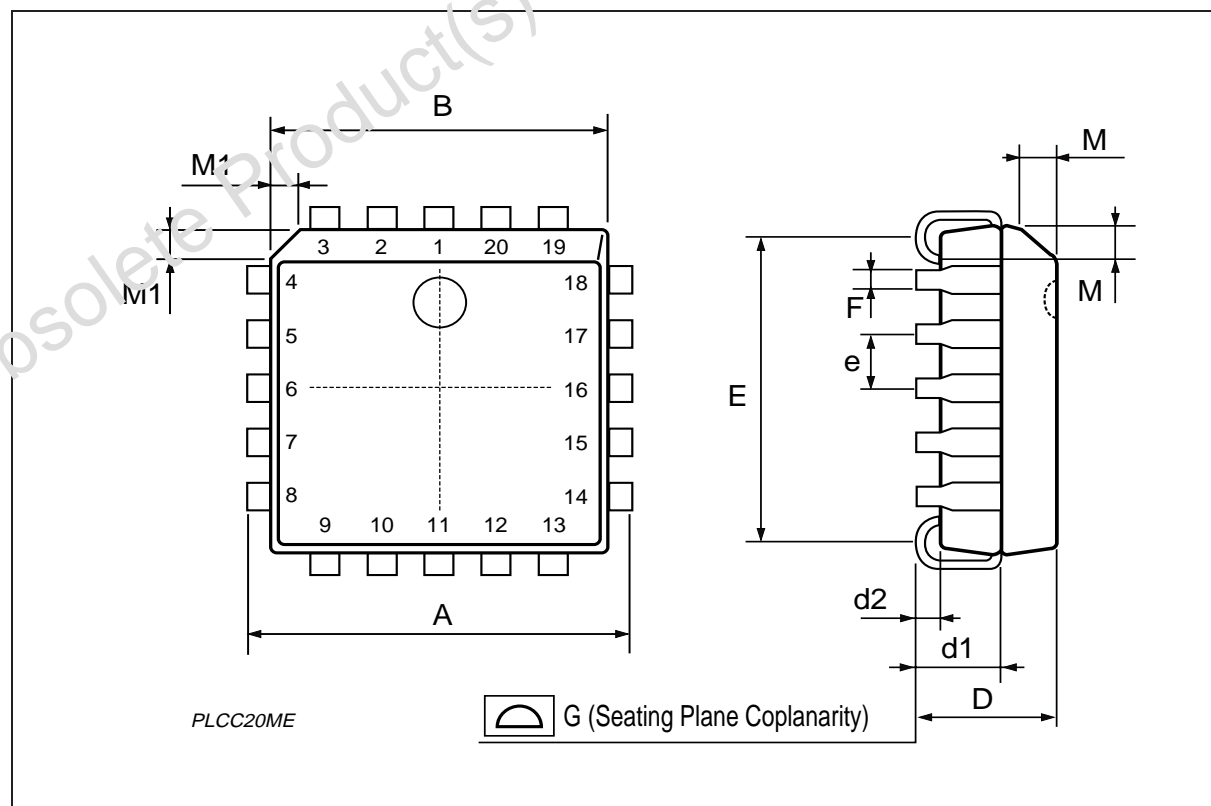
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

OUTLINE AND MECHANICAL DATA

DIP20

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