ROHM
SEMICONDUCTOR

STRUCTURE Silicon Monolithic Integrated Circuit
TYPE 1ch DC/DC converter IC
PRODUCT SERIES **BD95503MUV**
FEATURES ・Built in 1ch H³Reg DC/DC converter controller
・Adjustable output voltage setting (0.75V～5.5V)

○Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage	VIN, VINS	24 *1*2	V
BOOT Voltage	BOOT	30 *1*2	V
BOOT-SW Voltage	BOOT-SW	7 *1*2	V
Output Voltage	VOUT	7 *1*2	V
Output Feedback Voltage	FB	VREG	V
VREG Voltage	VREG	7 *1*2	V
Current Limit Setting Voltage	ILIM	VREG	V
Logic Input Voltage	EN	24 *1*2	V
Output Current（Average）	Isw	3*1	A
Power Dissipation 1	Pd1	0.34 *3	W
Power Dissipation 2	Pd2	0.70 *4	W
Power Dissipation 3	Pd3	1.21 *5	W
Power Dissipation 4	Pd4	3.56 *6	W
Operating Temperature Range	Topr	-20～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 2.7mW/℃ for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*4 Reduced by 5.6mW/℃ for increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB, copper foil area : 10.29mm²)
*5 Reduced by 9.7mW/℃ for increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB, copper foil area: 10.29mm², 2-3layer: 5505mm²)
*6 Reduced by 28.5mW/℃ for increase in Ta of 1℃ over 25℃. (when mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB, copper foil area: 5505mm²)

○Operating Conditions （Ta=25℃）

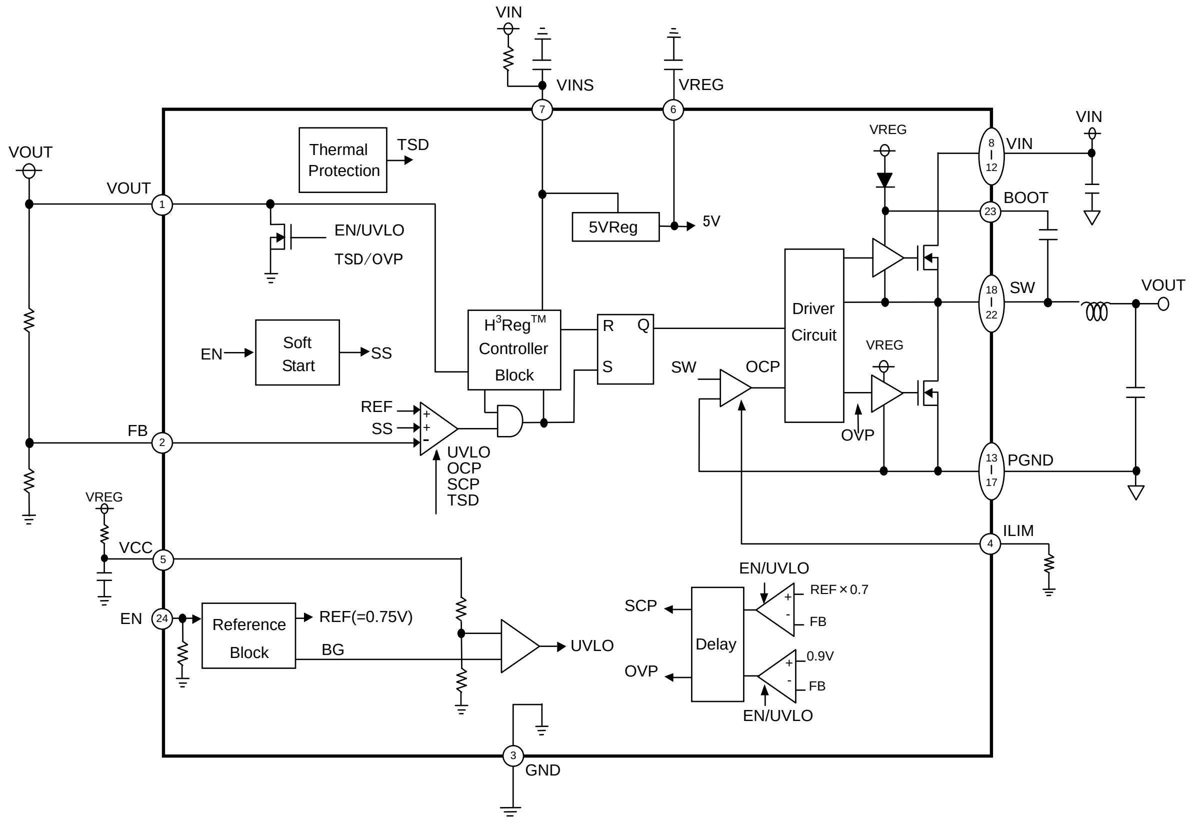
Parameter	Symbol	MIN.	MAX.	Unit
Input Voltage	VIN, VINS	7.5	20	V
BOOT Voltage	BOOT	4.5	25	V
SW Voltage	SW	-0.7	20	V
BOOT-SW Voltage	BOOT-SW	4.5	5.5	V
Logic Input Voltage	EN	0	20	V
Output Voltage	VOUT	0.75	5.5	V
MIN ON TIME	tonmin	-	100	ns

● This product is not designed to be used in a radioactive environment.

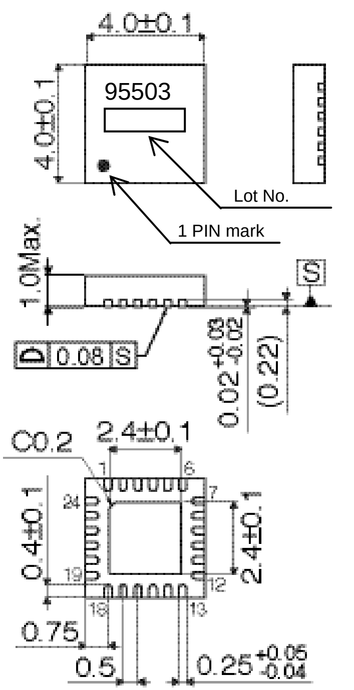
○Electrical Characteristics (Unless otherwise noted, Ta=25℃ VCC=5V, VIN=VINS=12V, V_{EN}=3V, VOUT=1.8V)

Parameter	Symbol	Standard Value			Unit	Conditions
		MIN.	TYP.	MAX.		
[Whole Device]						
VIN Bias current	I_{IN}	-	1.0	2.0	mA	VCC=VREG
VIN Standby current	I_{IN}_stb	-	0	10	μA	V_{EN}=0V
EN Low Voltage	V_{EN}_low	GND	-	0.3	V	
EN High Voltage	V_{EN}_high	2.2	-	20	V	
EN Pull-down resistance	R_{EN}	30	50	70	kΩ	
[5VLinear Regulator]						
VREG Standby Voltage	VREG_stb	-	-	0.1	V	V_{EN}=0V
VREG Output Voltage	VREG	4.9	5.1	5.3	V	VIN=VINS=7.5V to 20V Ireg=10mA
[Under Voltage Lock Out]						
VREG threshold Voltage	$VREG_{UVLO}$	3.75	4.20	4.65	V	VREG:Sweep up
VREG hysteresis Voltage	$dVREG_{UVLO}$	100	160	220	mV	VREG:Sweep down
[Over Voltage Protection]						
FB threshold Voltage	FB_{OVP}	0.8	0.9	1.0	V	
[H^{3}Reg^{TM} Control]						
ON Time	ton	200	300	400	ns	
MIN OFF Time	Toffmin	300	500	-	ns	
[FET Driver]						
High side ON resistance	R_{HGhon}	-	0.270	0.540	Ω	
Low side ON resistance	R_{LGlon}	-	0.135	0.270	Ω	
[Current Control]						
Current Limit threshold Voltage	Vilim	440	470	500	mV	R_{ILIM}=47kΩ
[Output Voltage Sense]						
FB threshold Voltage	FB	0.738	0.750	0.762	V	
FB Input current	I_{FB}	-1	-	1	μA	
VOUT discharge current	I_{VOUT}	5	10	-	mA	VOUT=1V, V_{EN}=0V
[SCP]						
Threshold Voltage	Vthscp	REF×0.6	REF×0.7	REF×0.8	V	

○Block Diagram



○Physical Dimension



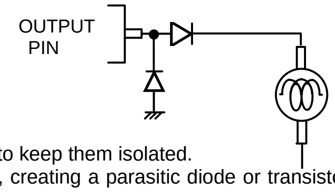
(Unit : mm)

○Pin number・Pin name

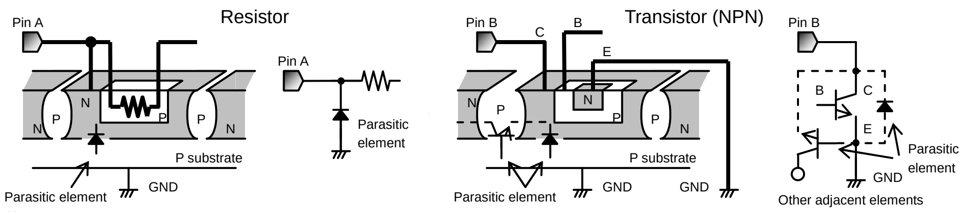
PIN No.	PIN name
1	VOUT
2	FB
3	GND
4	ILIM
5	VCC
6	VREG
7	VINS
8-12	VIN
13-17	PGND
18-22	SW
23	BOOT
24	EN
Reverse	FIN

○ NOTE FOR USE

1. Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. Supply line
Since the motor’s reverse electromotive force gives rise to the return of regenerative current, measures should be taken to establish a channel for the current, such as adding a capacitor between the power supply and GND. In determining the approach to take, make sure that no problems will be posed by the various characteristics involved, such as capacitance loss at low temperatures with an electrolytic capacitor.
3. GND voltage
The potential of GND, PGND pin must be minimum potential in all operating conditions.
4. Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
5. Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
6. Actions in strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
7. ASO
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.
8. Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.
9. Electrical characteristics
The electrical characteristics in the Specifications may vary depending on ambient temperature, power supply voltage, circuit(s) externally applied, and/or other conditions. It is therefore requested to carefully check them including transient characteristics.
10. Not of a radiation-resistant design.
11. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.



12. Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated.
P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



13. Ground Wiring Pattern
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
14. Operating ranges
If it is within the operating ranges, certain circuit functions and operations are warranted in the working ambient temperature range. With respect to characteristic values, it is unable to warrant standard values of electric characteristics but there are no sudden variations in characteristic values within these ranges.
15. Thermal shutdown circuit
This IC is provided with a built-in thermal shutdown (TSD) circuit, which is activated when the chip temperature reaches the threshold value listed below. When TSD is on, the device goes to high impedance mode. Note that the TSD circuit is provided for the exclusive purpose shutting down the IC in the presence of extreme heat, and is not designed to protect the IC per se or guarantee performance when or after extreme heat conditions occur. Therefore, do not operate the IC with the expectation of continued use or subsequent operation once the TSD is activated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature[℃] (typ.)
175	15

16.Output Voltage Resistor Setting
Output volage is adjusted with resistor. Total 10kohm resistor is recommended so that the output voltage is not affected by the FB input current (Typ. 1uA).
17. Heat sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND.

Notes

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