March 2015

FQT13N06L

N-Channel QFET® MOSFET

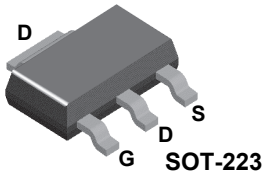
60 V, 2.8 A, 110 mΩ

General Description

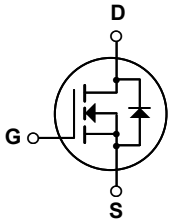
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 2.8 A, 60 V, $R_{DS(on)}$ = 110 mΩ (Max.) @V_{GS} = 10 V, I_D = 1.4 A
- Low Gate Charge (Typ. 4.8 nC)
- Low Crss (Typ. 17 pF)
- 100% Avalanche Tested



SOT-223
FQT Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQT13N06L	Unit
V_{DSS}	Drain-Source Voltage		60	V
I_D	Drain Current - Continuous (T_C = 25°C)		2.8	A
	- Continuous (T_C = 70°C)		2.24	A
I_{DM}	Drain Current - Pulsed	(Note 1)	11.2	A
V_{GSS}	Gate-Source Voltage		± 20	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	85	mJ
I_{AR}	Avalanche Current	(Note 1)	2.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	0.21	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		2.1	W
	- Derate above 25°C		0.017	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	60	°C/W

* When mounted on the minimum pad size recommended(PCB mount).

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.05	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 48 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.4 A	--	0.088	0.11	Ω
		V_{GS} = 5 V, I_D = 1.4 A	--	0.110	0.14	
g_{FS}	Forward Transconductance	V_{DS} = 25 V, I_D = 1.4 A (Note 4)	--	4.1	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	270	350	pF
C_{oss}	Output Capacitance		--	95	125	pF
C_{rss}	Reverse Transfer Capacitance		--	17	23	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 6.8 A, R_G = 25 Ω (Note 4, 5)	--	8	25	ns
t_r	Turn-On Rise Time		--	90	190	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 13.6 A, V_{GS} = 5 V (Note 4, 5)	--	4.8	6.4	nC
Q_{gs}	Gate-Source Charge		--	1.6	--	nC
Q_{gd}	Gate-Drain Charge		--	2.7	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	11.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.8 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 13.6 A, dI_F / dt = 100 A/μs (Note 4)	--	45	--	ns
Q_{rr}	Reverse Recovery Charge		--	45	--	nC

Notes:
1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 12.6 mH, I_{AS} = 2.8 A, V_{DD} = 25 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 13.6 A, di/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Pulse test : pulse width ≤ 300 μs, Duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

Typical Characteristics

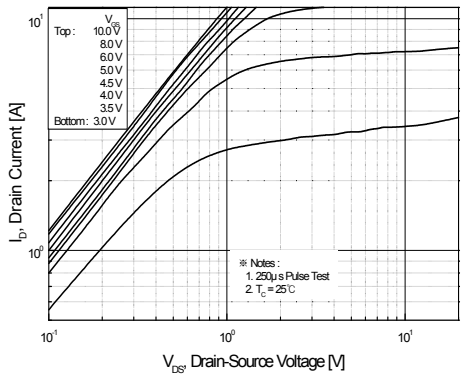


Figure 1. On-Region Characteristics

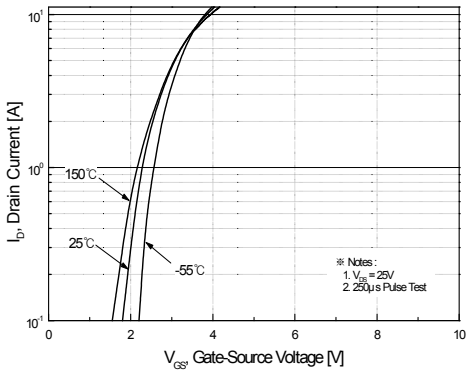


Figure 2. Transfer Characteristics

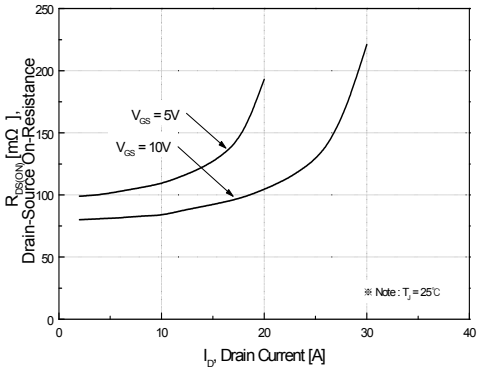


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

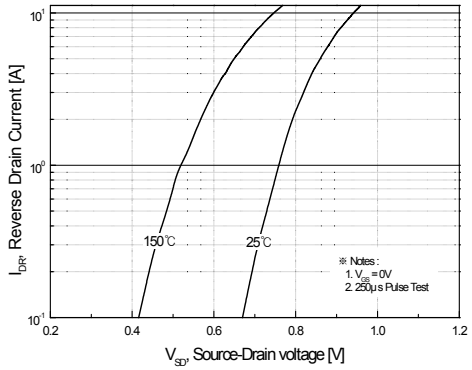


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

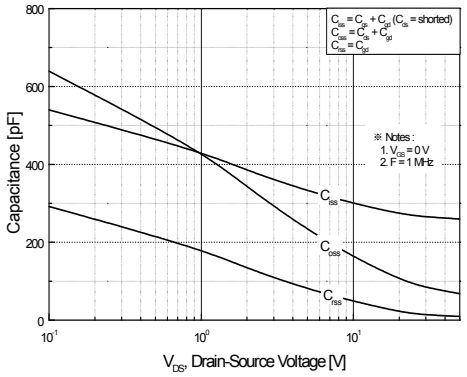


Figure 5. Capacitance Characteristics

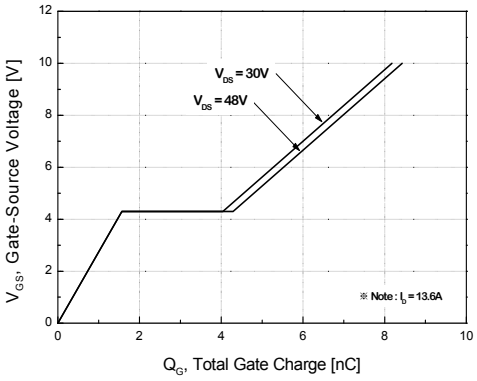


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

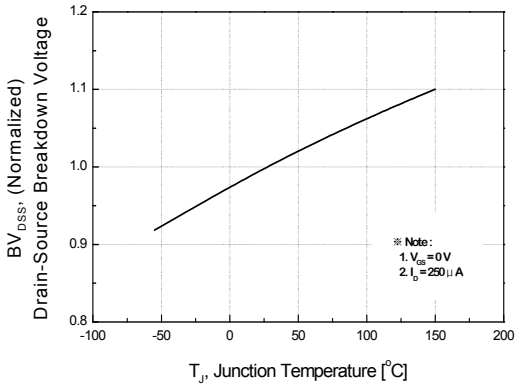


Figure 7. Breakdown Voltage Variation vs Temperature

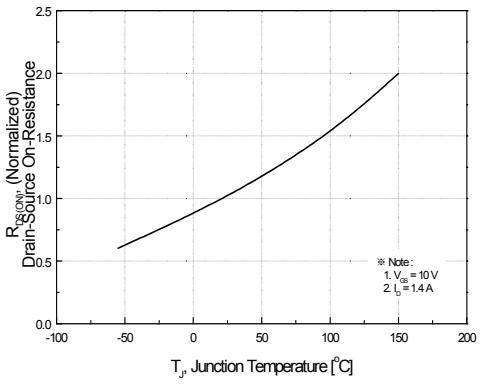


Figure 8. On-Resistance Variation vs Temperature

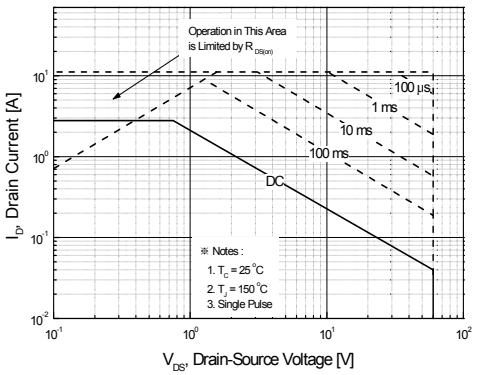


Figure 9. Maximum Safe Operating Area

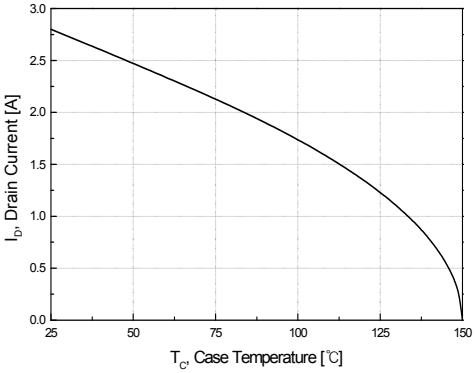


Figure 10. Maximum Drain Current vs Case Temperature

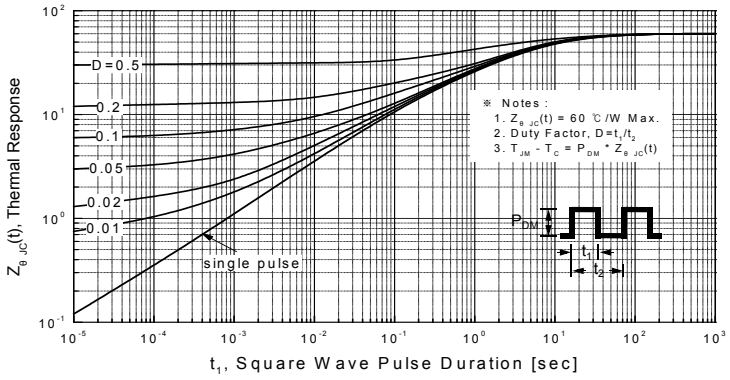


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

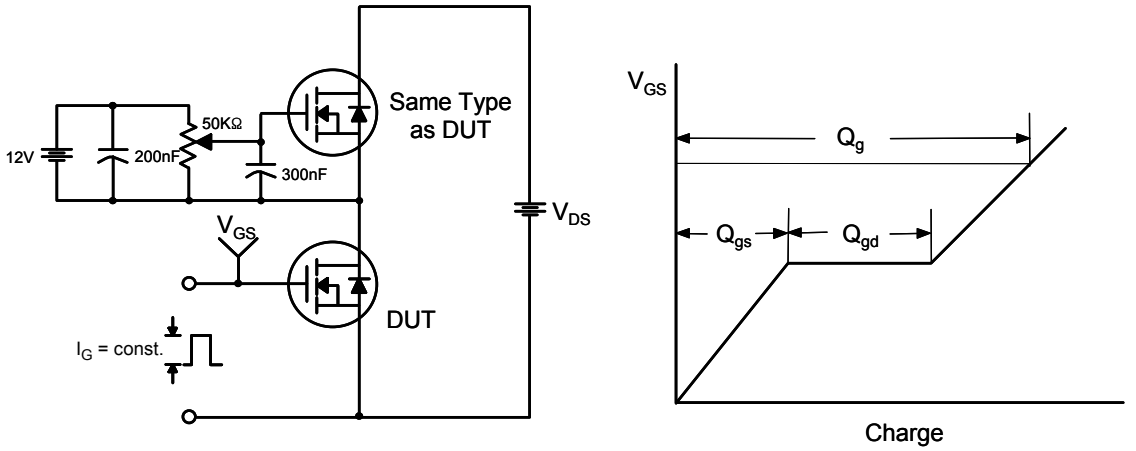


Figure 13. Resistive Switching Test Circuit & Waveforms

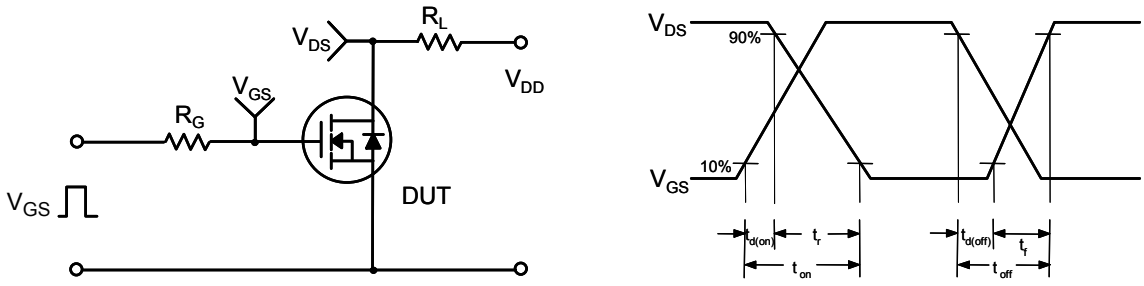


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

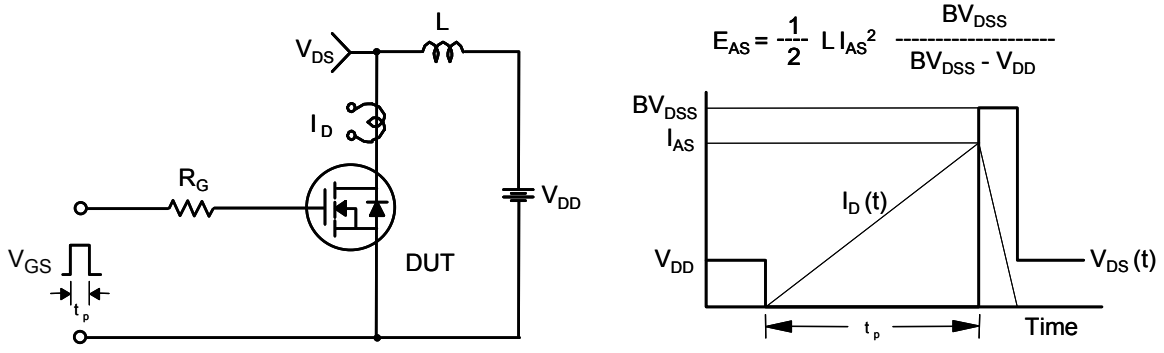
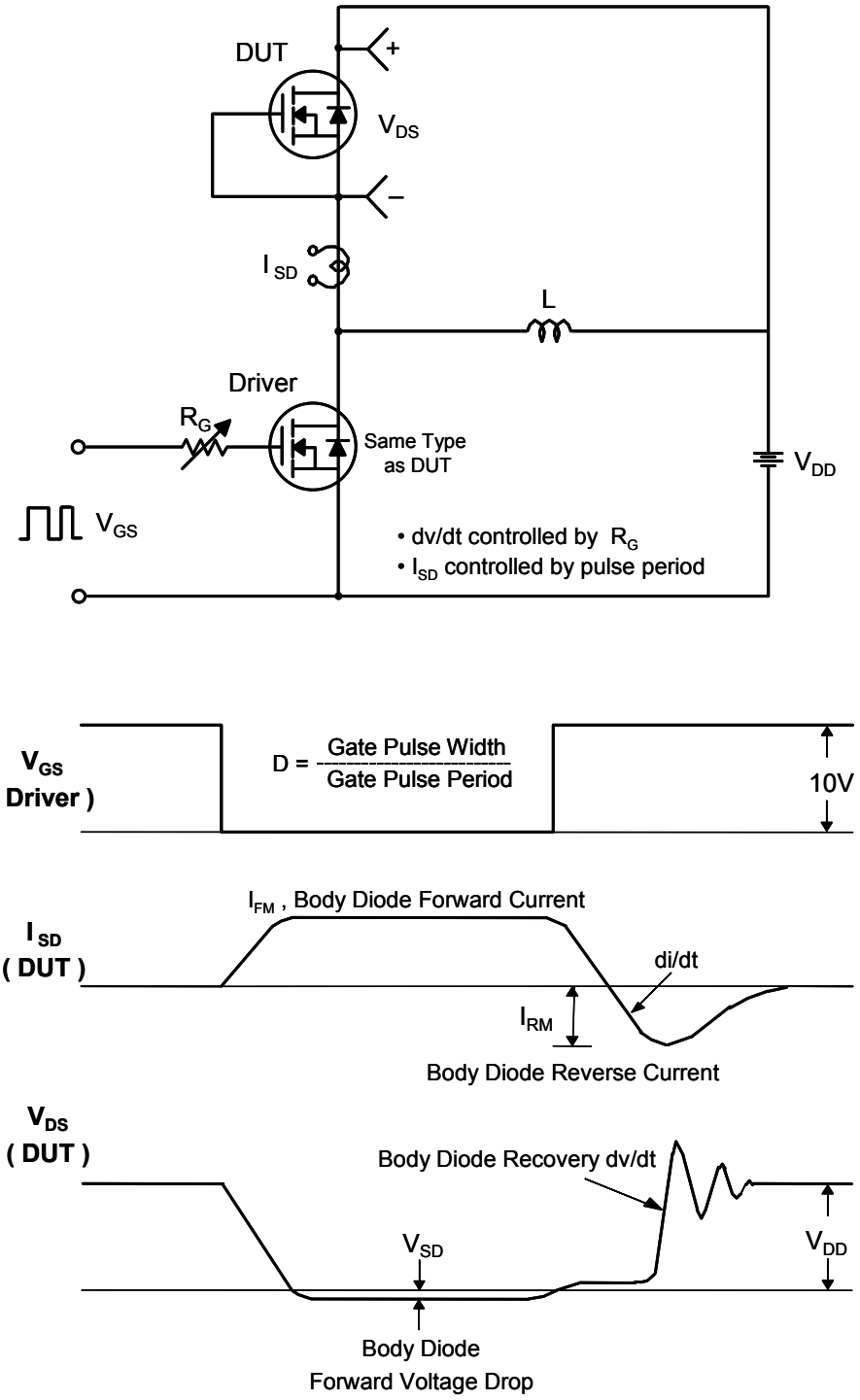


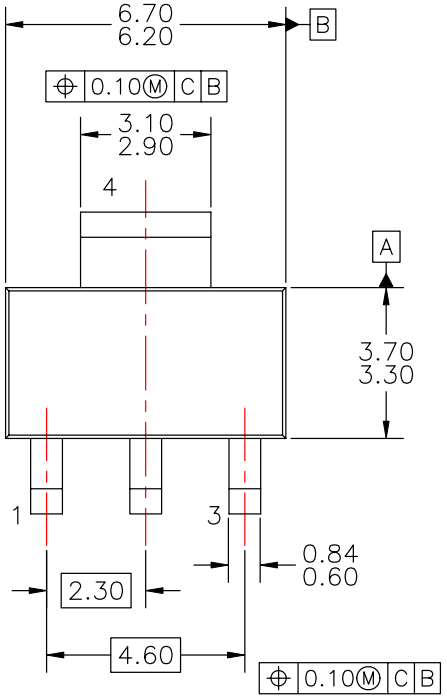
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

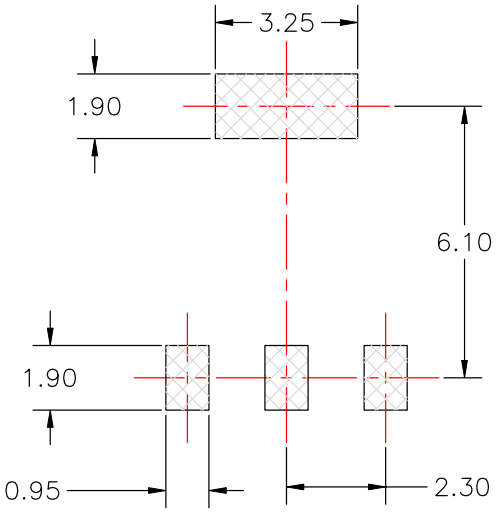


APPROVED
July-14-2008

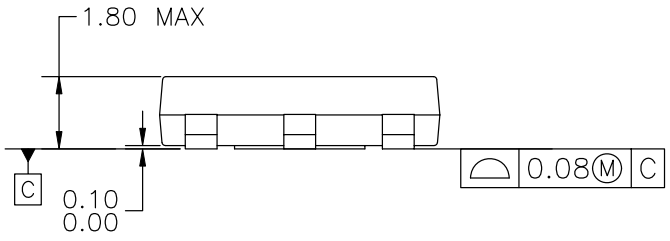
REVISIONS

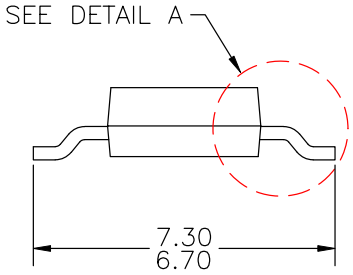
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR $0.74^{+0.05}_{-0.07}$ TO 0.60–0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR $1.80^{}_{1.20}$ TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR $0.3^{+0.09}_{-0.07}$ TO 0.20–0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR $3.56^{+0.18}_{-0.38}$ TO $3.70^{}_{3.30}$; CHG BODY LN FR $6.5^{+0.3}_{-0.4}$ TO $6.70^{}_{6.30}$; CHG TOTAL PKG WID FR $6.96^{+0.33}_{-0.38}$ TO $7.30^{}_{6.70}$; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP

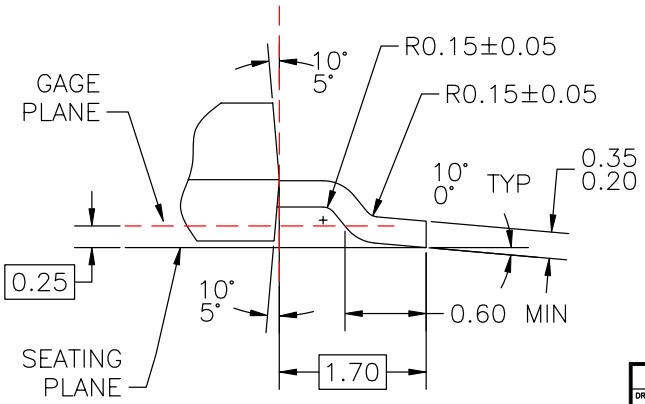




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING BASED ON JEDEC REGISTRATION TO–261, VARIATION AA.
B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
C) ALL DIMENSIONS ARE IN MILLIMETERS.
D) DRAWING CONFORMS TO ASME Y14.5M–1994.
E) LANDPATTERN NAME: SOT230P700X180–4BN
F) DRAWING FILENAME: MKT–MA04AREV2

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	26FEB2008
CHECKED: L.Z. STA CRUZ	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

FAIRCHILD SEMICONDUCTOR TM

MOLDED PACKAGE
SOT–223, 4 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
1:1	A3	MKT–MA04A	2

FORMERLY: N/A

SHEET : 1 OF 1

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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