SN65C1167E, SN65C1168E
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS WITH ±15-kV ESD PROTECTION

SLLS740A – MARCH 2007 – REVISED APRIL 2007

FEATURES

- **Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11**
- **Operate From Single 5-V Power Supply**
- **ESD Protection for RS-422 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2, Contact Discharge**
  - **±8-kV IEC 61000-4-2, Air-Gap Discharge**
- **Low Supply-Current Requirements: 9 mA Max**
- **Low Pulse Skew**
- **Receiver Input Impedance . . . 17 kΩ (Typ)**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Common-Mode Input Voltage Range of –7 V to 7 V**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Receiver 3-State Outputs Active-Low Enable (SN65C1167E Only)**

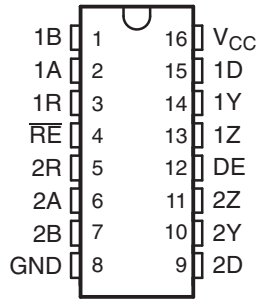
DESCRIPTION/ORDERING INFORMATION

The SN65C1167E and SN65C1168E consist of dual drivers and dual receivers with ±15-kV ESD (Human Body Model [HBM]) and ±8-kV ESD (IEC61000-4-2 Air-Gap Discharge and Contact Discharge) for RS-422 bus pins. The devices meet the requirements of TIA/EIA-422-B and ITU recommendation V.11.

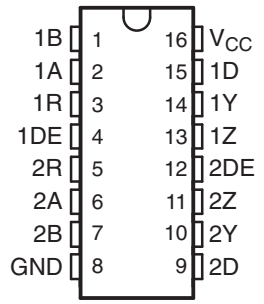
The SN65C1167E combines dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be connected together externally to function as direction control.

SN65C1168E drivers have individual active-high enables.

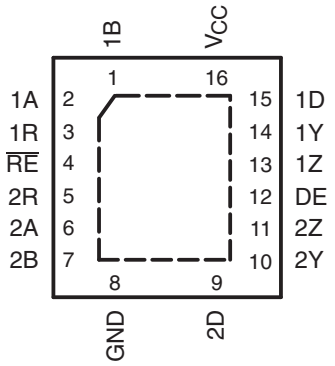
SN65C1167E . . . NS OR PW PACKAGE
(TOP VIEW)



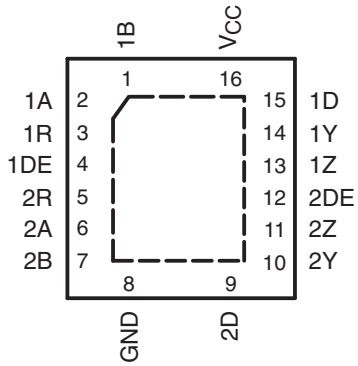
SN65C1168E . . . NS OR PW PACKAGE
(TOP VIEW)



SN65C1167E . . . RGY PACKAGE
(TOP VIEW)



SN65C1168E . . . RGY PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOP – NS	Tube of 50	SN65C1167ENS	65C1167E
			SN65C1168ENS	65C1168E
		Reel of 2000	SN65C1167ENSR	65C1167E
			SN65C1168ENSR	65C1168E
	TSSOP – PW	Tube of 90	SN65C1167EPW	CB1167E
			SN65C1168EPW	CB1168E
		Reel of 2000	SN65C1167EPWR	CB1167E
			SN65C1168EPWR	CB1168E
	QFN – RGY	Reel of 1000	SN65C1167ERGYR	CB1167
			SN65C1168ERGYR	CB1168

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES
Each Driver

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN65C1167E, Each Receiver(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq$ –0.2 V	L	L
X	H	Z
Open	L	H

(1) H = High level, L = Low level, ? = Indeterminate, X = Irrelevant, Z = High impedance (off)

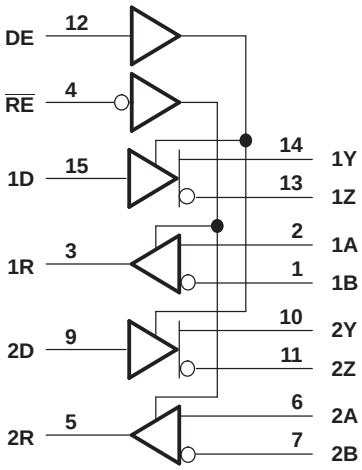
SN65C1168E, Each Receiver(1)

DIFFERENTIAL INPUTS A–B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
–0.2 V < V_{ID} < 0.2 V	?
$V_{ID} \leq$ –0.2 V	L
Open	H

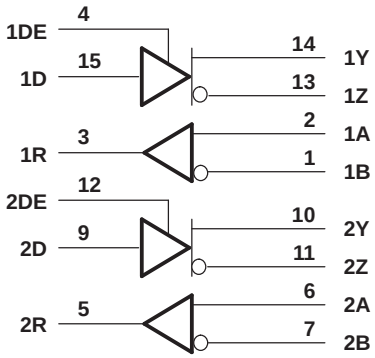
(1) H = High level, L = Low level, ? = Indeterminate

LOGIC DIAGRAMS (POSITIVE LOGIC)

SN65C1167E

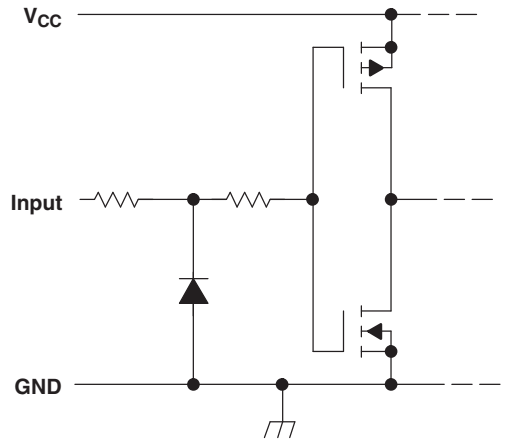


SN65C1168E

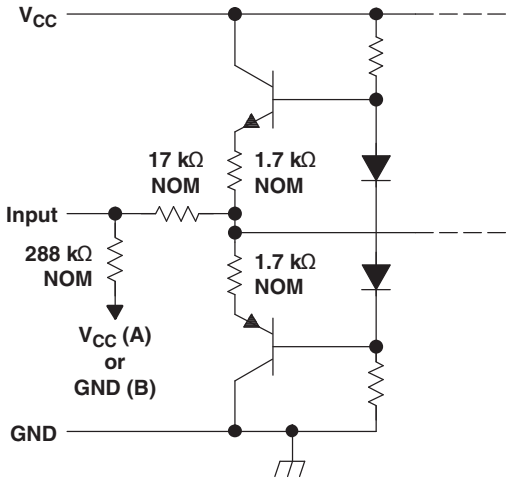


SCHEMATIC OF INPUTS

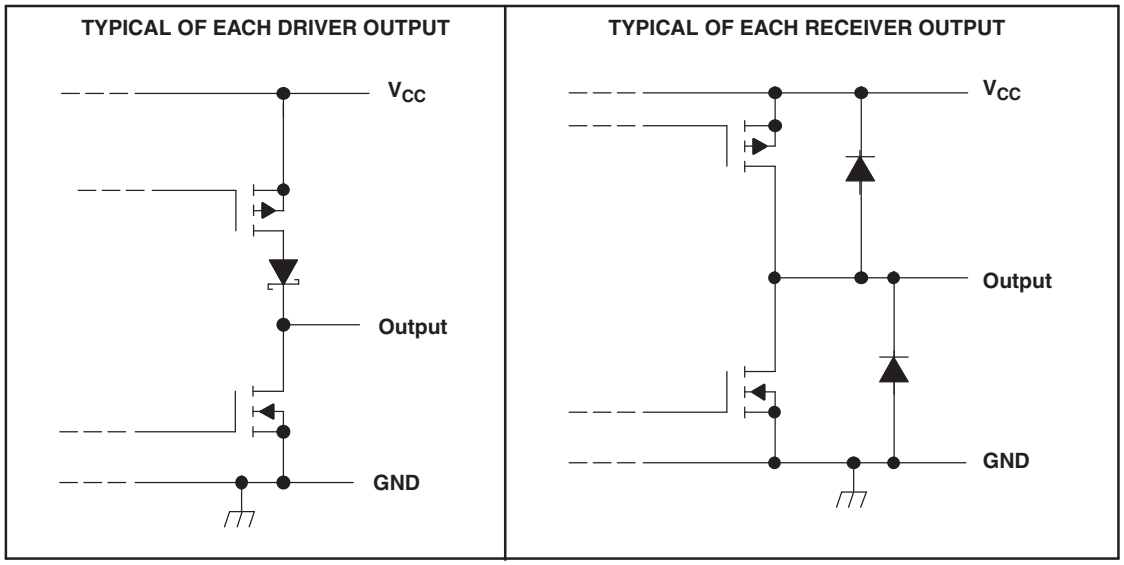
EQUIVALENT OF DRIVER ENABLE INPUT



EQUIVALENT OF A OR B INPUT



SCHEMATIC OF OUTPUTS



Absolute Maximum Ratings(1)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	7	V
V_I	Input voltage range	Driver, DE, RE	–0.5	7	V
		A or B, Receiver	–14	14	
V_{ID}	Differential input voltage range(3)	Receiver	–14	14	V
V_O	Output voltage range	Driver	–0.5	7	V
		Receiver	–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current range	Driver, V_I < 0		–20	mA
I_{OK}	Output clamp current range	Driver, V_O < 0		–20	mA
		Receiver		±20	
I_O	Output current range	Driver		±150	mA
		Receiver		±25	
I_{CC}	Supply current range			200	mA
	GND current			–200	mA
T_J	Operating virtual junction temperature			150	°C
θ_{JA}	Package thermal impedance(4)(5)	NS package		64	°C/W
		PW package		108	
		RGY package		39	
T_A	Operating free-air temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential input voltage are with respect to the network GND.
(3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.
(4) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IC}	Common-mode input voltage(1)	Receiver			±7	V
V_{ID}	Differential input voltage	Receiver			±7	V
V_I	Input voltage	Except A, B	0		5.5	V
V_O	Output voltage	Receiver	0		V_{CC}	V
V_{IH}	High-level input voltage	Except A, B	2			V
V_{IL}	Low-level input voltage	Except A, B			0.8	V
I_{OH}	High-level output current	Receiver			–6	mA
		Driver			–20	
I_{OL}	Low-level output current	Receiver			6	mA
		Driver			20	
T_A	Operating free-air temperature		–40		85	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –20 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage 1	I_O = 0 mA		2		6	V
$\|V_{OD2}\|$	Differential output voltage 2	R_L = 100 Ω, See Figure 1(2)		2	3.7		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 100 Ω, See Figure 1(2)				±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω, See Figure 1(2)				±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage	R_L = 100 Ω, See Figure 1(2)				±0.4	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0 V	V_O = 6 V			100	µA
			V_O = –0.25 V			100	
I_{OZ}	High-impedance-state output current	V_O = 2.5 V				20	µA
		V_O = 5 V				–20	
I_{IH}	High-level input current	V_I = V_{CC} or V_{IH}				1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}				–1	µA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND(3)		–30		–150	mA
I_{CC}	Supply current (total package)	No load, Enabled	V_I = V_{CC} or GND		4	6	mA
			V_I = 2.4 or 0.5 V(4)		5	9	
C_i	Input capacitance				6		pF

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Refer to TIA/EIA-422-B for exact conditions.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(4) This parameter is measured per input, while the other inputs are at V_{CC} or GND.

Switching Characteristics

over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 2	R3 = 500 Ω, S1 is open,		8	16	ns
t_{PLH}	Propagation delay time, low- to high-level output				8	16	ns
$t_{sk(p)}$	Pulse skew				1.5	4	ns
t_r	Rise time	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 3	R3 = 500 Ω, S1 is open,		5	10	ns
t_f	Fall time				5	10	ns
t_{PZH}	Output-enable time to high level	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 4	R3 = 500 Ω, S1 is closed,		10	19	ns
t_{PZL}	Output-enable time to low level				10	19	ns
t_{PHZ}	Output-disable time from high level	R1 = R2 = 50 Ω, C1 = C2 = C3 = 40 pF, See Figure 4	R3 = 500 Ω, S1 is closed,		7	16	ns
t_{PLZ}	Output-disable time from low level				7	16	ns

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver output	HBM	±15	kV
	IEC 61000-4-2, Air-Gap Discharge	±8	
	IEC 61000-4-2, Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input				–0.2(2)			V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	SN65C1167E	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = –6 mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV,	I_{OL} = 6 mA		0.1	0.3	V
I_{OZ}	High-impedance state output current	SN65C1167E	V_O = V_{CC} or GND			±0.5	±5	µA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = –10 V			–2.5	
I_I	Enable input current, $\overline{RE}$	SN65C1167E	V_I = V_{CC} or GND				±1	µA
r_I	Input resistance		V_{IC} = –7 V to 7 V,	Other input at 0 V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4 V or 0.5 V(3)		5	9	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) Refer to TIA/EIA-422-B for exact conditions.

Switching Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5		9	15	27	ns
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 5		9	15	27	ns
t_{TLH}	Transition time, low- to high-level output	V_{IC} = 0 V,	See Figure 5		4	9	ns
t_{THL}	Transition time, high- to low-level output				4	9	ns
t_{PZH}	Output-enable time to high level	SN65C1167E	R_L = 1 kΩ, C_L= 50 pF See Figure 6		7	22	ns
t_{PZL}	Output-enable time to low level				7	22	ns
t_{PHZ}	Output-disable time from high level				12	22	ns
t_{PLZ}	Output-disable time from low level				12	22	ns

(1) Measured per input while the other inputs are at V_{CC} or GND
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Receiver input	HBM	±15	kV
	IEC 61000-4-2, Air-Gap Discharge	±8	
	IEC 61000-4-2, Contact Discharge	±8	

PARAMETER MEASUREMENT INFORMATION

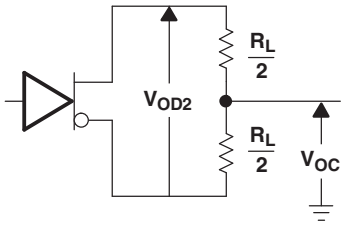
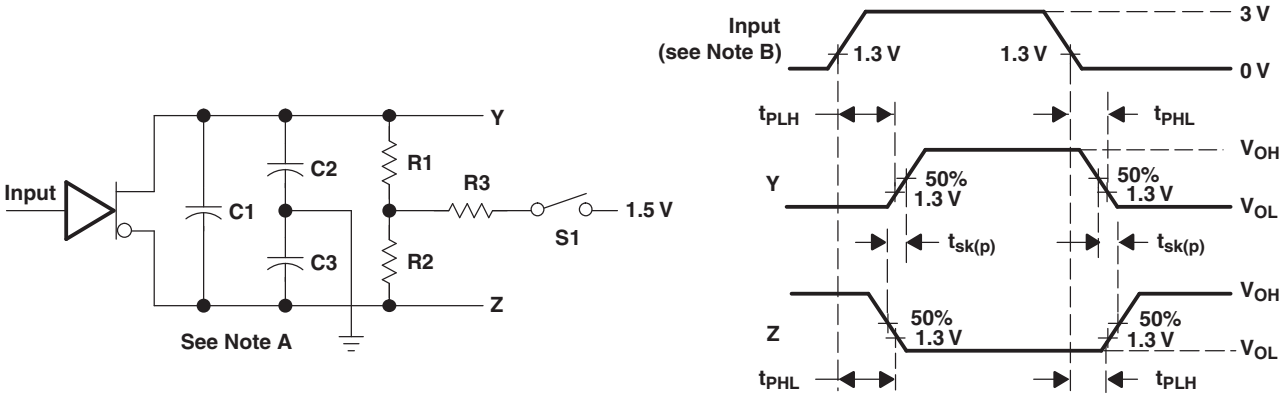


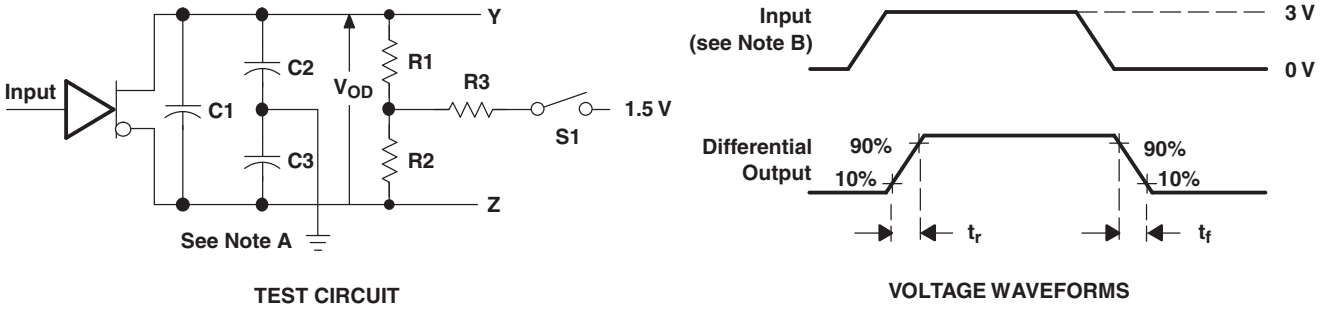
Figure 1. Driver Test Circuit, V_{OD} and V_{OC}



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \le 6$ ns.

Figure 2. Driver Test Circuit and Voltage Waveforms

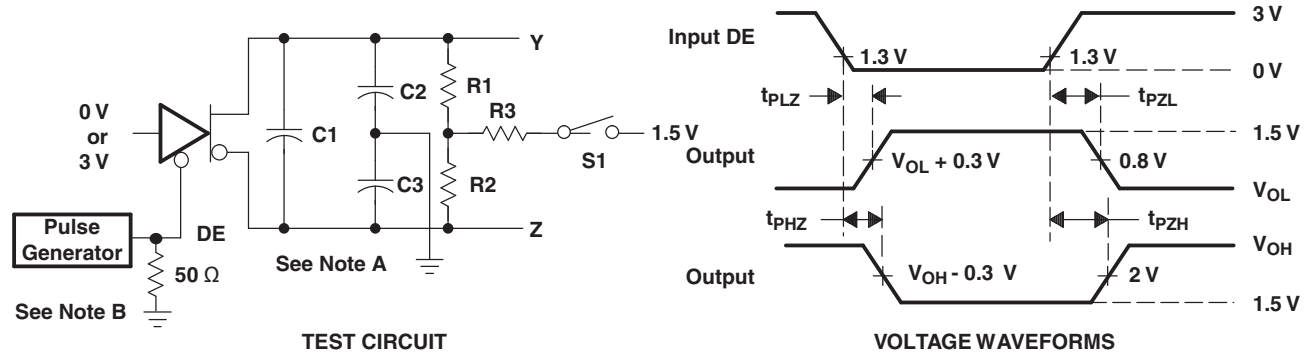


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \le 6$ ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

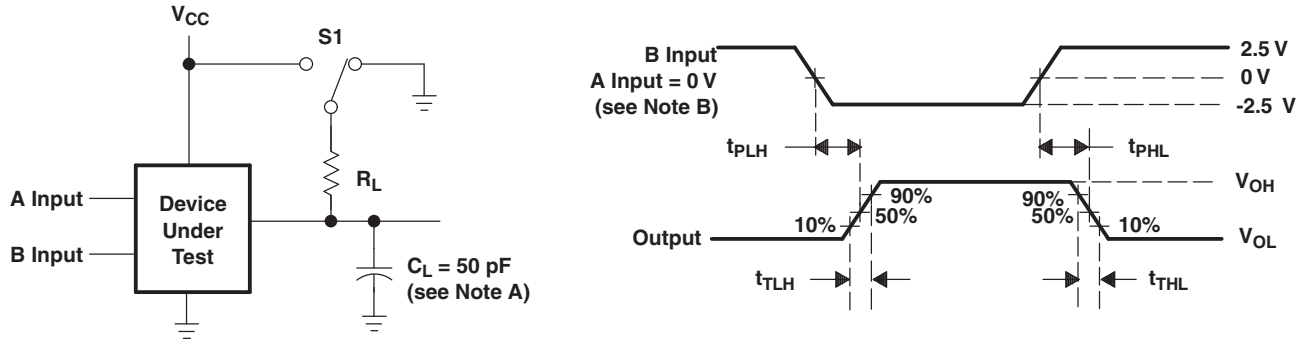
PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \le 6$ ns.

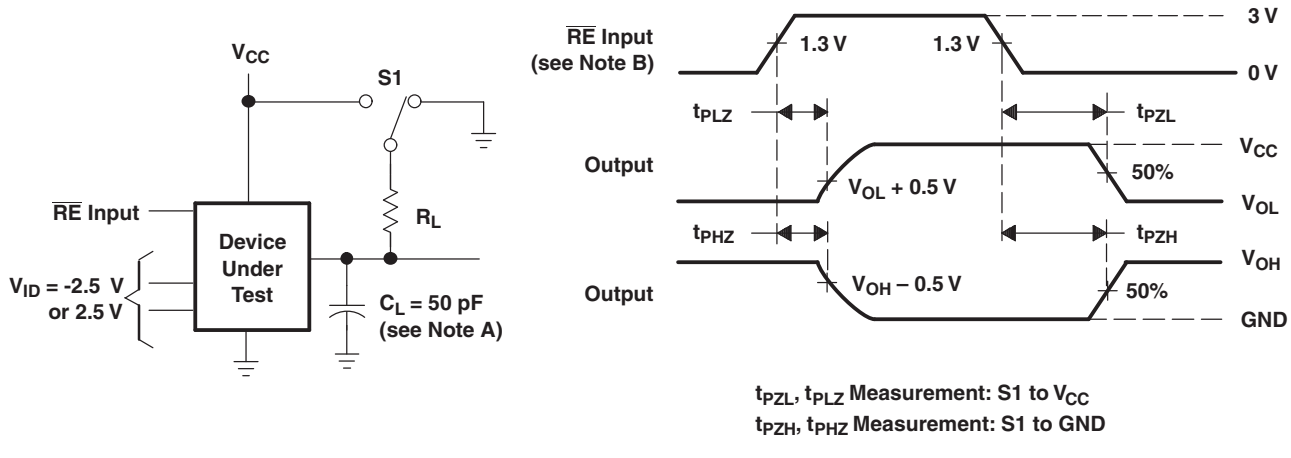
Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR≤ 1 MHz, duty cycle = 50%, $t_r = t_f \le 6$ ns.

Figure 5. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR≤ 1 MHz, duty cycle = 50%, $t_r = t_f \le 6$ ns.

Figure 6. Receiver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C1167ENS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E	Samples
SN65C1167ENSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1167E	Samples
SN65C1167EPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E	Samples
SN65C1167EPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1167E	Samples
SN65C1167ERGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB1167	Samples
SN65C1168ENS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E	Samples
SN65C1168ENSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E	Samples
SN65C1168ENSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C1168E	Samples
SN65C1168EPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E	Samples
SN65C1168EPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E	Samples
SN65C1168EPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E	Samples
SN65C1168EPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB1168E	Samples
SN65C1168ERGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB1168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

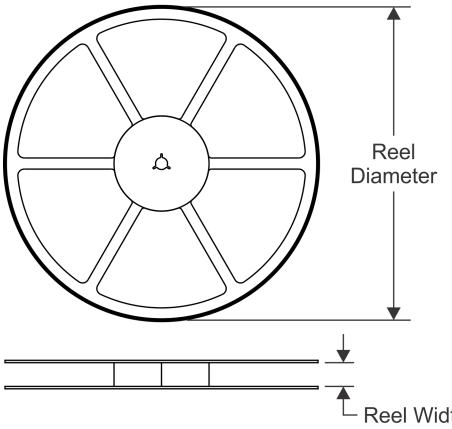
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

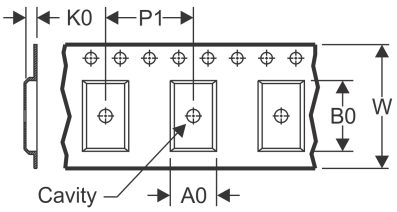
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

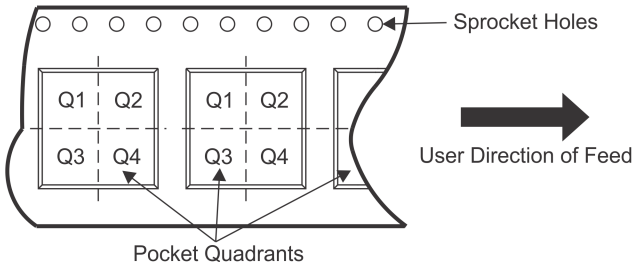


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

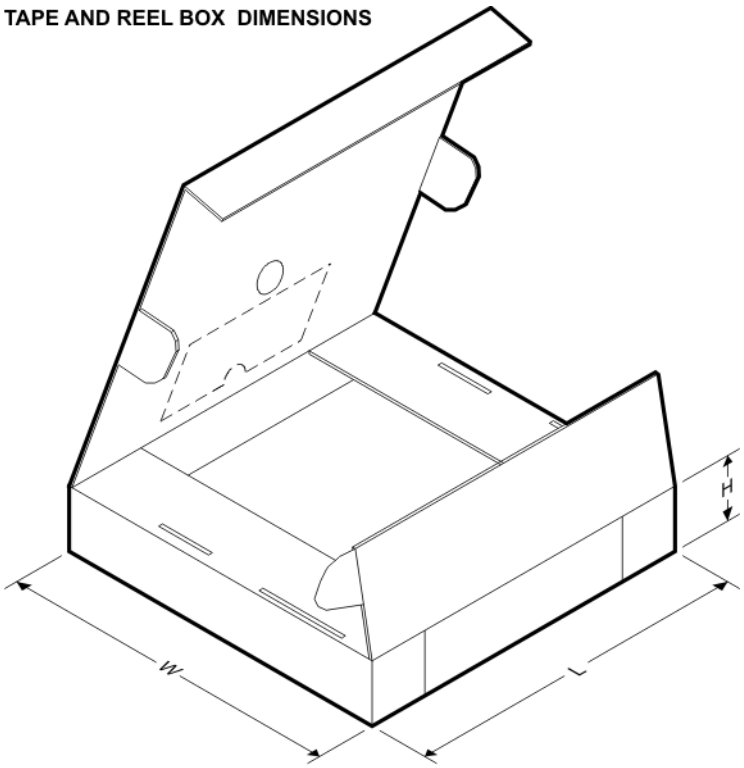
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C1167ENSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C1167EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1167ERGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65C1168EPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65C1168ERGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

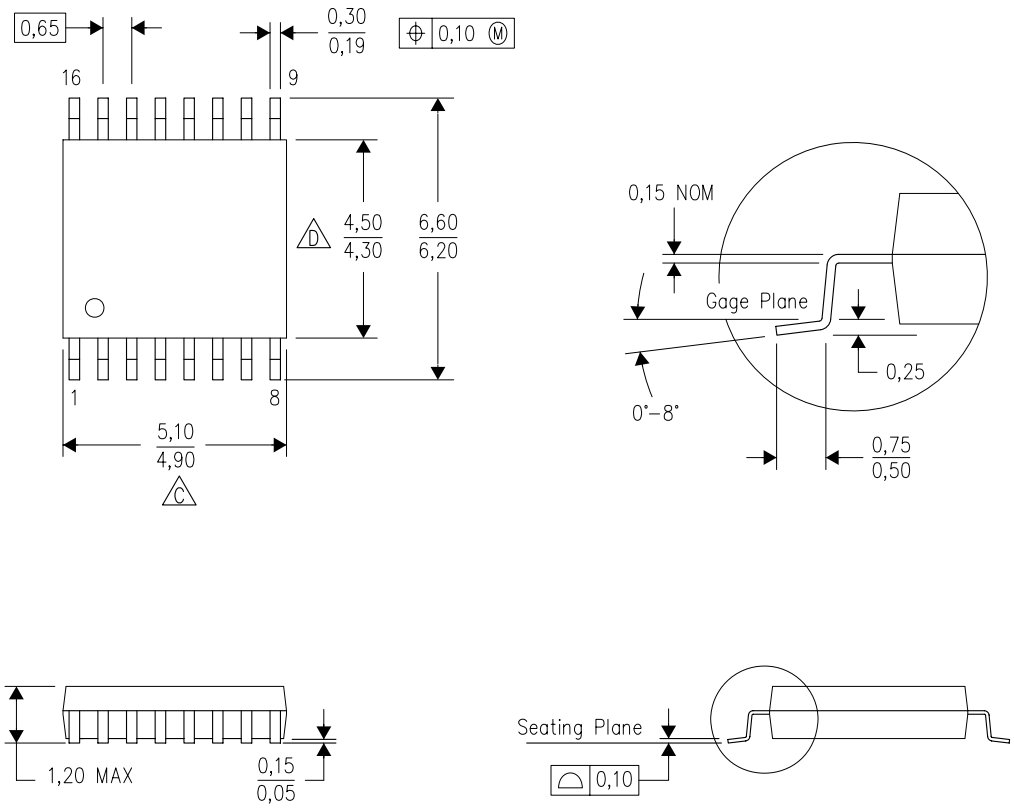
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C1167ENSR	SO	NS	16	2000	367.0	367.0	38.0
SN65C1167EPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65C1167ERGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
SN65C1168EPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65C1168ERGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

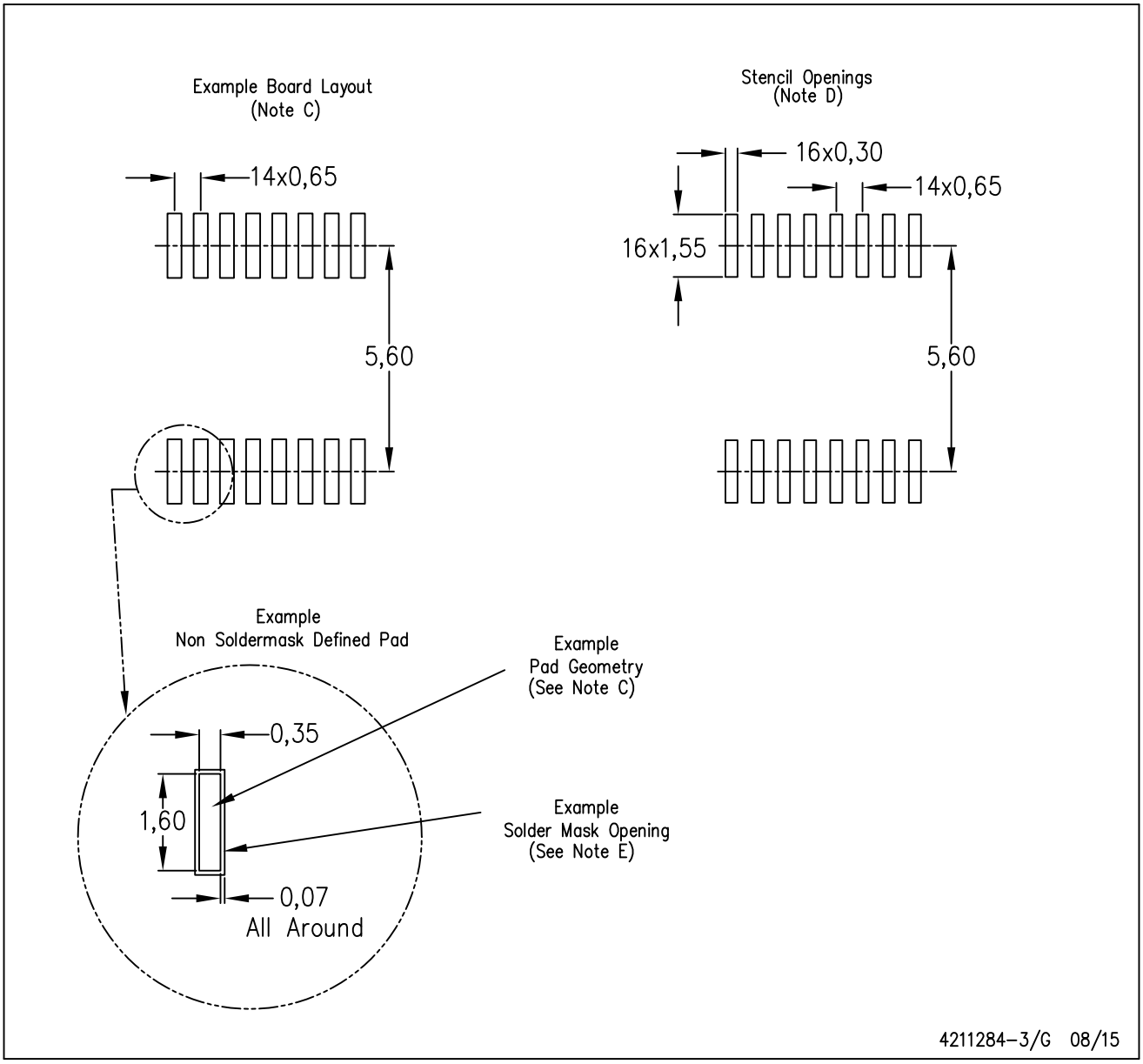
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

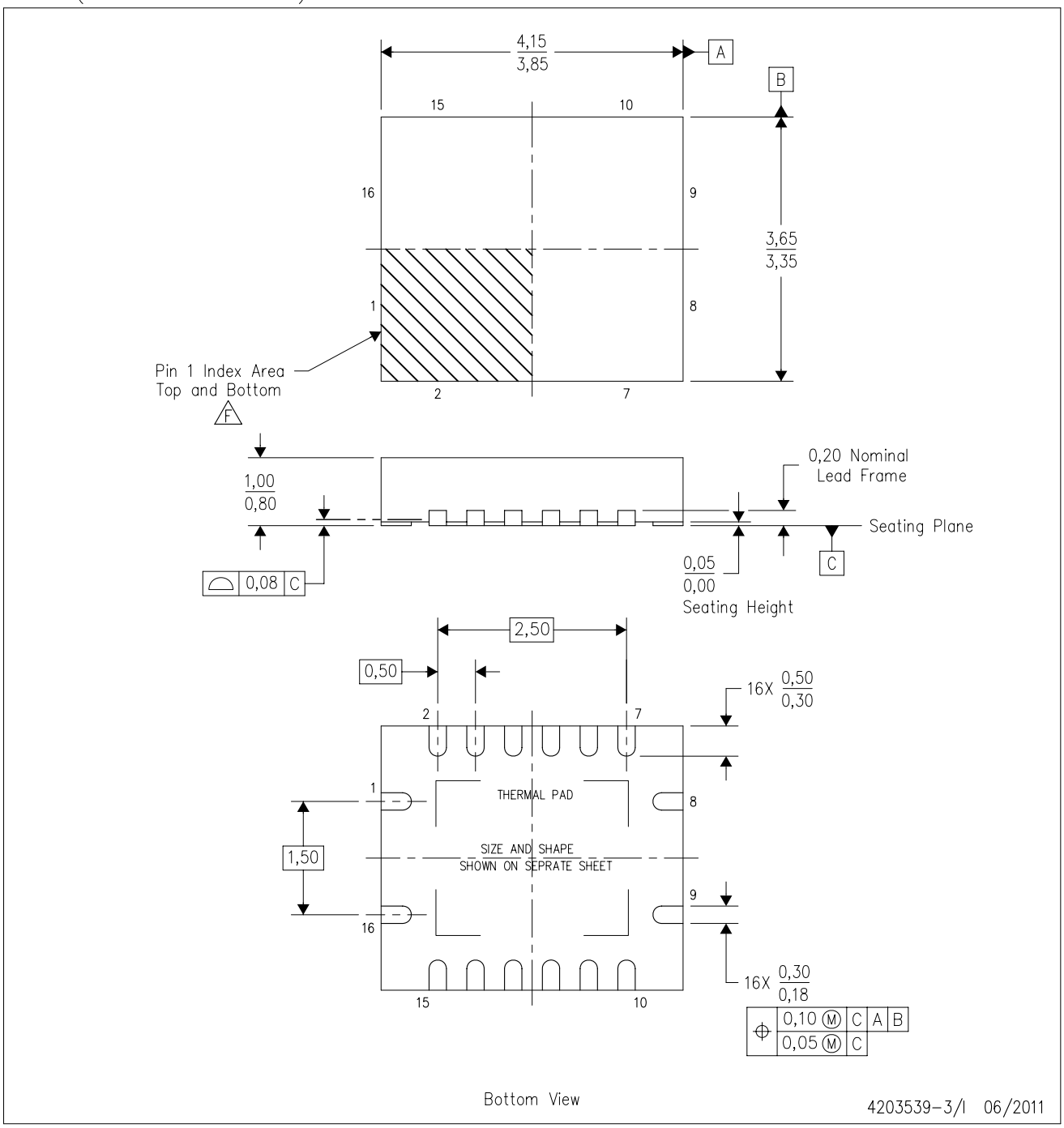
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

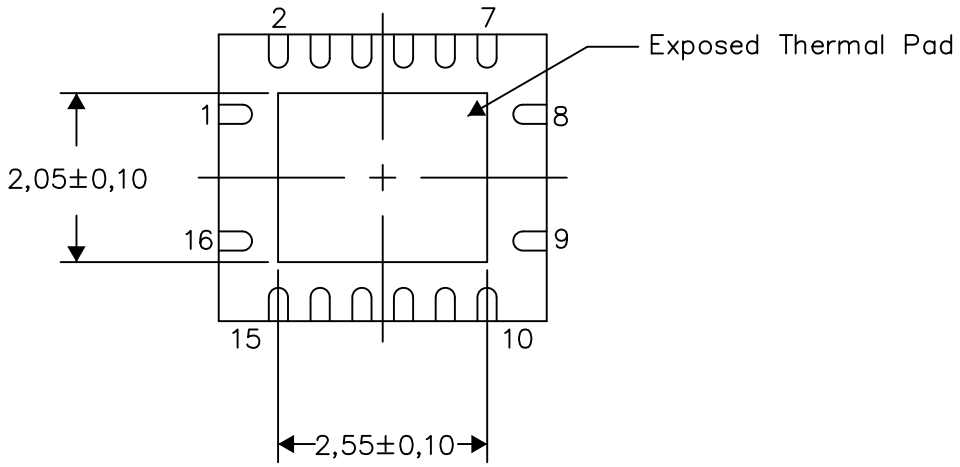
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



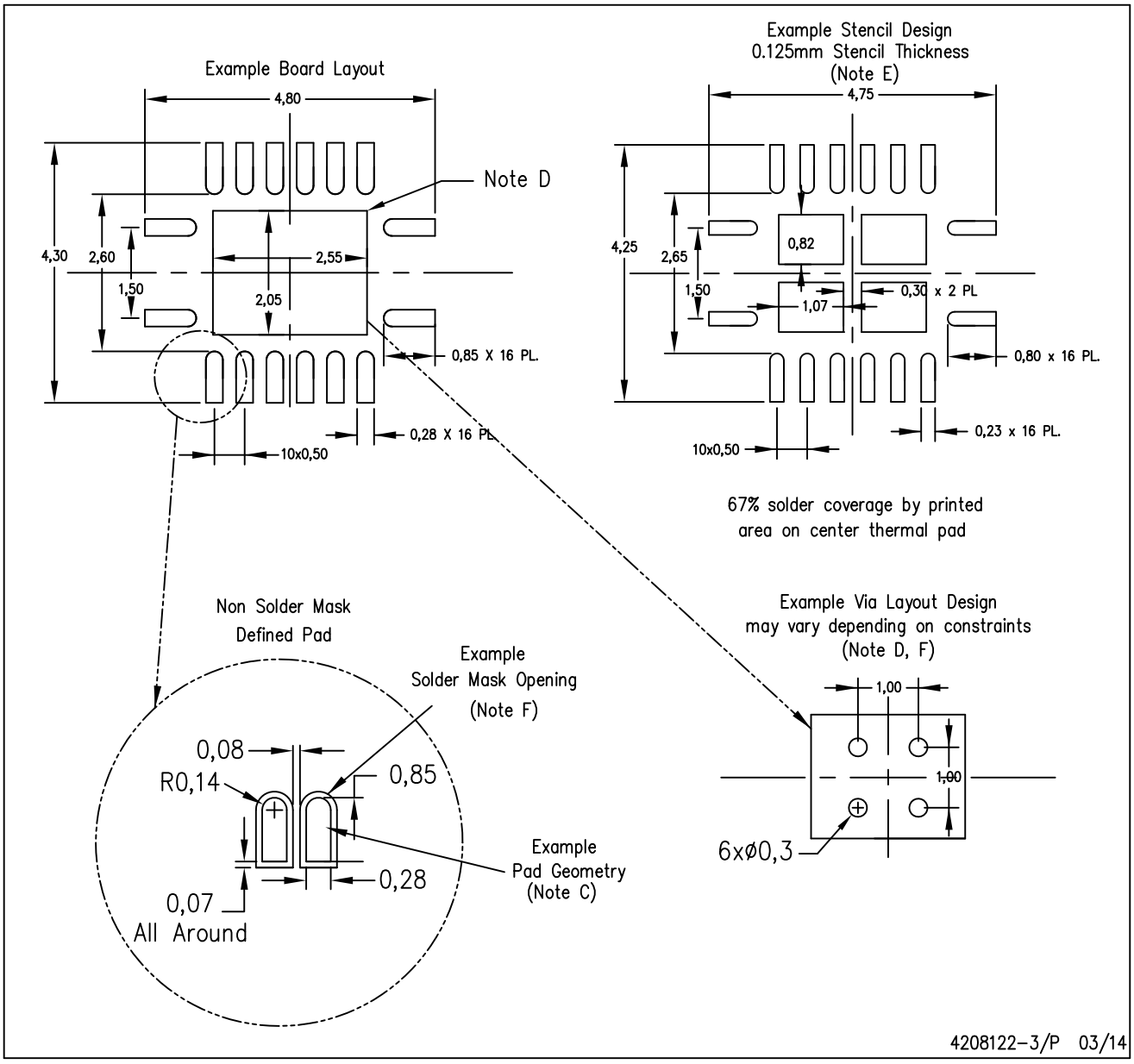
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

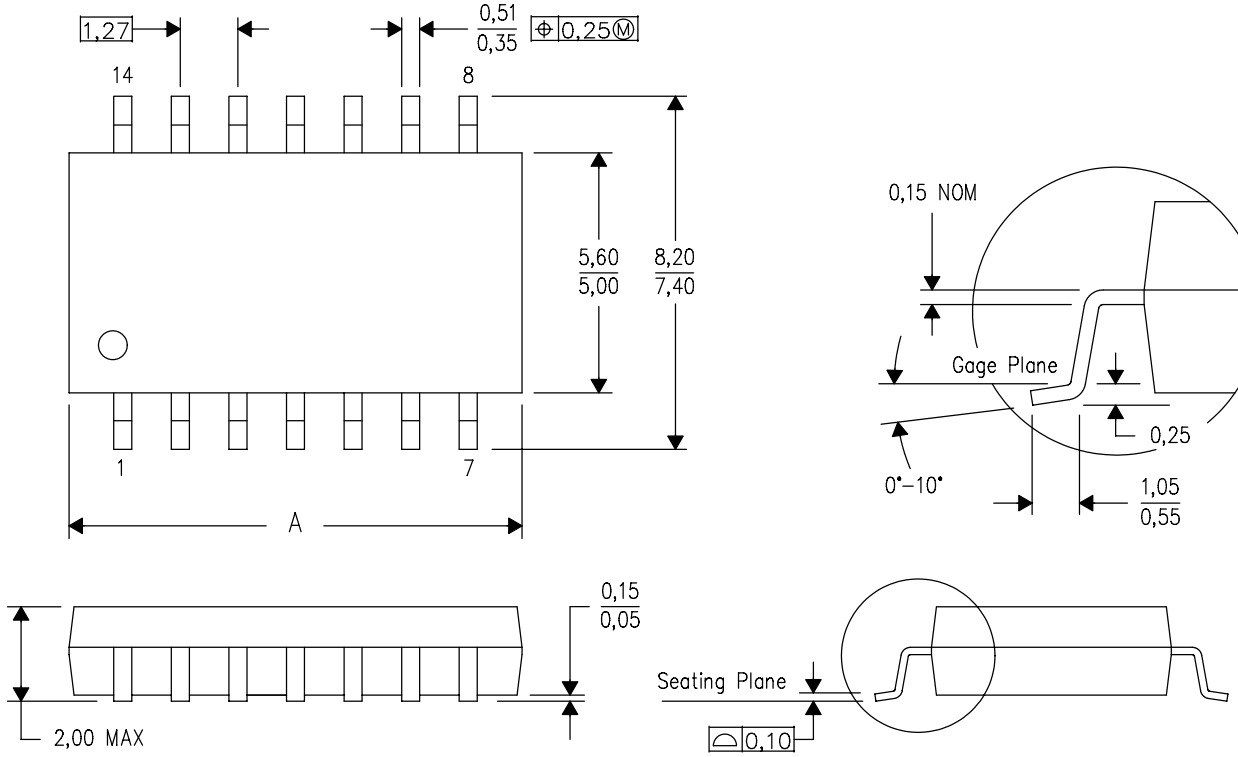


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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