VIPER16

Fixed frequency VIPer™ plus family

Datasheet - production data

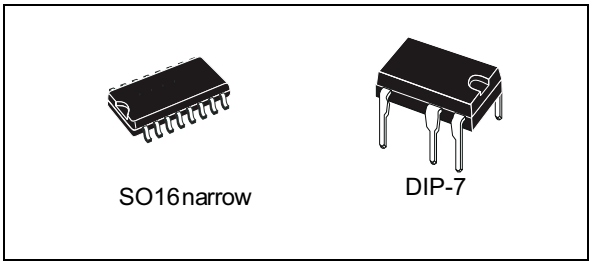
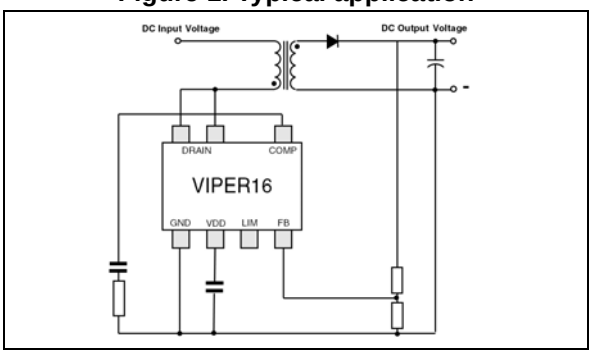


Figure 1. Typical application



Features

- 800 V avalanche rugged power section
- PWM operation with frequency jittering for low EMI
- Operating frequency:
  - 60 kHz for L type
  - 115 kHz for H type
- No need of auxiliary winding for low power application
- Standby power < 30 mW at 230 V_{AC}
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

Application

- Replacement of capacitive power supply
- Auxiliary power supply for appliances,
- Power metering
- LED drivers

Description

The device is an off-line converter with an 800 V avalanche ruggedness power section, a PWM controller, user defined overcurrent limit, protection against feedback network disconnection, hysteretic thermal protection, soft start up and safe auto restart after any fault condition. It is able to power itself directly from the rectified mains, eliminating the need for an auxiliary bias winding. Advance frequency jittering reduces EMI filter cost. Burst mode operation and the devices very low consumption both help to meet the standard set by energy saving regulations.

Table 1. Device summary

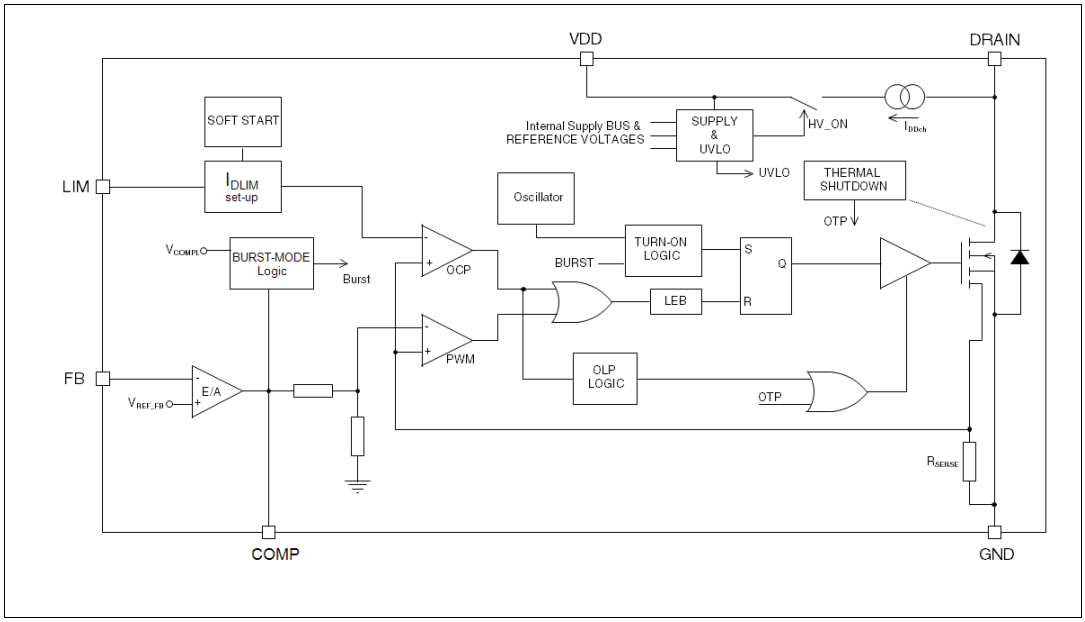
Order codes	Package	Packaging
VIPER16LN	DIP-7	Tube
VIPER16HN		
VIPER16HD	SO16 narrow	Tube
VIPER16HDTR		Tape and reel
VIPER16LD		Tube
VIPER16LDTR		Tape and reel

This is information on a product in full production. www.st.com

Contents

1 Block diagram

Figure 2. Block diagram



2 Typical power

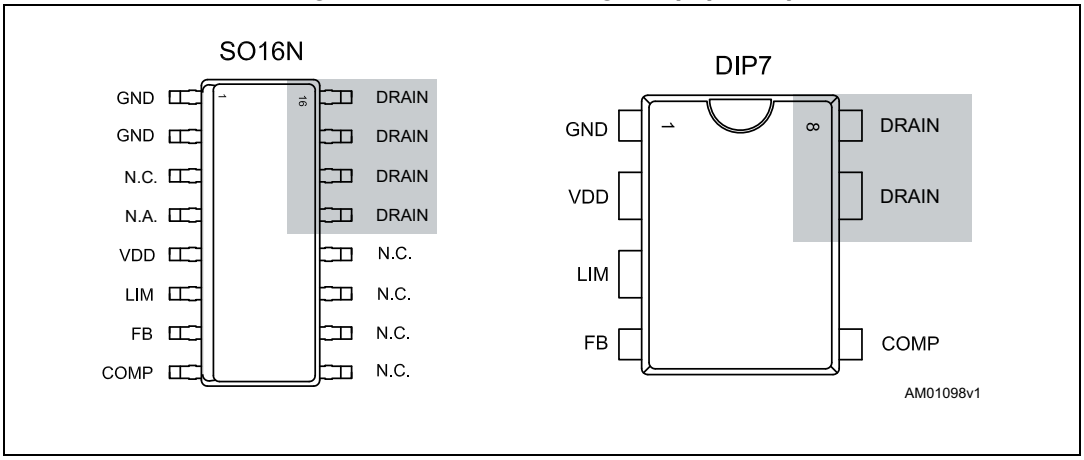
Table 2. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
VIPER16	9 W	10 W	5 W	6 W

1. Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3. Pin description

Pin N.		Name	Function
DIP-7	SO16		
1	1-2	GND	Connected to the source of the internal power MOSFET and controller ground reference.
-	4	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity, is highly recommended connect it to GND (pin 1-2).
2	5	VDD	Supply voltage of the control section. This pin provides the charging current of the external capacitor.
3	6	LIM	This pin allows setting the drain current limitation to a lower value respect to I_{Dlim}, which is the default one. The limit can be reduced by connecting an external resistor between this pin and GND. In case of high electrical noise, a capacitor could be connected between this pin and GND, the capacitor value must be lower than 470 nF in order to not impact the functionality of the pin. The pin can be left open if default drain current limitation, I_{Dlim}, is used.
4	7	FB	Inverting input of the internal trans conductance error amplifier. Connecting the converter output to this pin through a single resistor results in an output voltage equal to the error amplifier reference voltage (see V_{FB_REF} on *Table 8*). An external resistors divider is required for higher output voltages.

Table 3. Pin description (continued)

Pin N.		Name	Function
DIP-7	SO16		
5	8	COMP	Output of the internal trans conductance error amplifier. The compensation network have to be placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop. The pin is used also to directly control the PWM with an optocoupler. The linear voltage range extends from V_{COMPL} to V_{COMPH} (*Table 8*).
7,8	13-16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Pin (DIP-7)	Parameter	Value		Unit
			Min	Max	
V_{DRAIN}	7, 8	Drain-to-source (ground) voltage		800	V
E_{AV}	7, 8	Repetitive avalanche energy (limited by T_J = 150 °C)		2	mJ
I_{AR}	7, 8	Repetitive avalanche current (limited by T_J = 150 °C)		1	A
I_{DRAIN}	7, 8	Pulse drain current (limited by T_J = 150 °C)		2.5	A
V_{COMP}	5	Input pin voltage	-0.3	3.5	V
V_{FB}	4	Input pin voltage	-0.3	4.8	V
V_{LIM}	3	Input pin voltage	-0.3	2.4	V
V_{DD}	2	Supply voltage	-0.3	Self limited	V
I_{DD}	2	Input current		20	mA
P_{TOT}		Power dissipation at T_A < 40 °C (DIP-7)		1	W
		Power dissipation at T_A < 60 °C (SO16N)		1	W
T_J		Operating junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C
$ESD_{(HBM)}$	1 to 8	Human body model		4	kV
$ESD_{(CDM)}$	1 to 8	Charge device model		1.5	kV

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value SO16N	Max value DIP-7	Unit
R_{thJP}	Thermal resistance junction pin (Dissipated power = 1 W)	35	40	°C/W
R_{thJA}	Thermal resistance junction ambient (Dissipated power = 1 W)	90	110	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (Dissipated power = 1 W)	80	90	°C/W

1. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq in) of Cu (35 µm thick)

4.3 Electrical characteristics

(T_J = -25 to 125 °C, V_{DD} = 14 V [(a)]; unless otherwise specified)

Table 6. Power section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{BVDSS}	Break-down voltage	I_{DRAIN} = 1 mA, V_{COMP} = GND, T_J = 25 °C	800			V
$R_{DS(on)}$	Drain-source on state resistance	I_{DRAIN} = 0.2 A, T_J = 25 °C		20	24	Ω
		I_{DRAIN} = 0.2 A, T_J = 125 °C		40	48	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		10		pF
I_{OFF}	OFF state drain current	V_{DRAIN} = 640 V V_{FB} = GND			60	µA
		V_{DRAIN} = 800 V V_{FB} = GND			75	µA

Table 7. Supply section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		40	50	60	V
I_{DDch1}	Start up charging current	V_{DRAIN} = 100 V to 640 V, V_{DD} = 4 V	-0.6		-1.8	mA
I_{DDch2}	Charging current during operation	V_{DRAIN} = 100 V to 640 V, V_{DD} = 9 V falling edge	-7		-14	mA
V_{DD}	Operating voltage range		11.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 15 mA	23.5			V
V_{DDon}	V_{DD} start up threshold		12	13	14	V
V_{DDCSon}	VDD on internal high voltage current generator threshold		9.5	10.5	11.5	V
V_{DDoff}	V_{DD} under voltage shutdown threshold		7	8	9	V

a. Adjust V_{DD} above V_{DDon} start-up threshold before setting to 14 V

Table 7. Supply section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Current						
I_{DD0}	Operating supply current, not switching	F_{OSC} = 0 kHz, V_{COMP} = GND			0.6	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V, F_{SW} = 60 kHz			1.3	mA
		V_{DRAIN} = 120 V, F_{SW} = 115 kHz			1.5	mA
I_{DDoff}	Operating supply current with $V_{DD} < V_{DDoff}$	$V_{DD} < V_{DDoff}$			0.35	mA
I_{DDol}	Open loop failure current threshold	$V_{DD} = V_{DDclamp}$ V_{COMP} = 3.3 V,	4			mA

Table 8. Controller section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Error amplifier						
V_{REF_FB}	FB reference voltage		3.2	3.3	3.4	V
$I_{FB\_PULL\ UP}$	Current pull up			-1		µA
G_M	Trans conductance			2		mA/V
Current setting (LIM) pin						
V_{LIM_LOW}	Low level clamp voltage	I_{LIM} = -100 µA		0.5		V
Compensation (COMP) pin						
V_{COMPH}	Upper saturation limit	T_J = 25 °C		3		V
V_{COMPL}	Burst mode threshold	T_J = 25 °C	1	1.1	1.2	V
V_{COMPL_HYS}	Burst mode hysteresis	T_J = 25 °C		40		mV
H_{COMP}	ΔV_{COMP} / ΔI_{DRAIN}		4		9	V/A
$R_{COMP(DYN)}$	Dynamic resistance	V_{FB} = GND		15		kΩ
I_{COMP}	Source / sink current	V_{FB} > 100 mV		150		µA
	Max source current	V_{COMP} = GND, V_{FB} = GND		220		µA
Current limitation						
I_{Dlim}	Drain current limitation	I_{LIM} = -10 µA, V_{COMP} = 3.3 V, T_J = 25 °C	0.38	0.4	0.42	A
t_{SS}	Soft-start time			8.5		ms
T_{ON_MIN}	Minimum turn ON time		220		450	ns
I_{Dlim_bm}	Burst mode current limitation	$V_{COMP} = V_{COMPL}$		85		mA
Overload						
t_{OVL}	Overload time			50		ms
$t_{RESTART}$	Restart time after fault			1		s

Table 8. Controller section (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Oscillator section						
F_{OSC}	Switching frequency	VIPer16L	54	60	66	kHz
		VIPer16H	103	115	127	kHz
F_D	Modulation depth	F_{OSC} = 60 kHz		±4		kHz
		F_{OSC} = 115 kHz		±8		kHz
F_M	Modulation frequency			230		Hz
D_{MAX}	Maximum duty cycle		70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature(1)		150	160		°C
T_{HYST}	Thermal shutdown hysteresis(1)			30		°C

1. Specification assured by design, characterization and statistical correlation.

5 Typical electrical characteristics

Figure 4. IDlim vs T_J

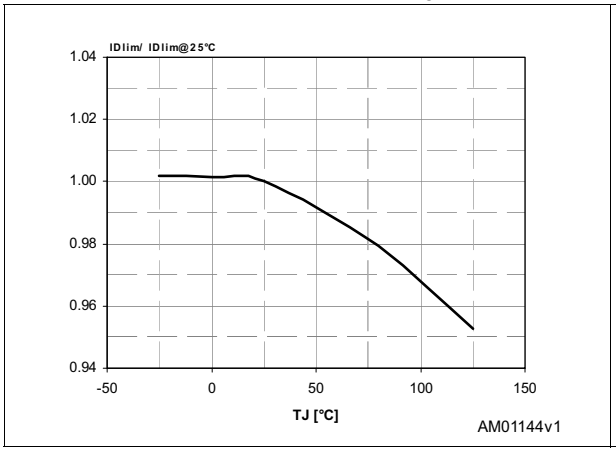


Figure 5. F_{OSC} vs T_J

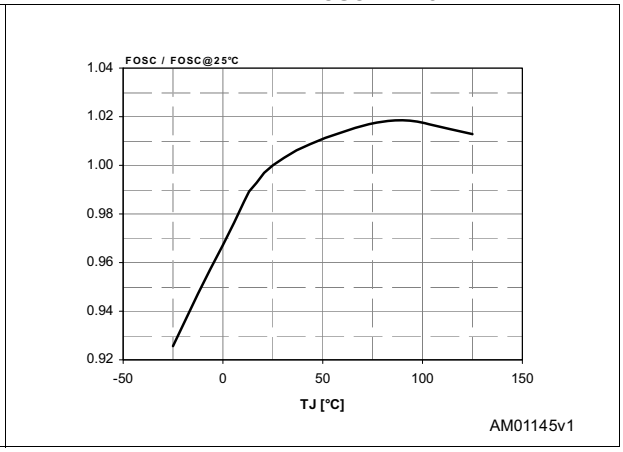


Figure 6. V_{DRAIN_START} vs T_J

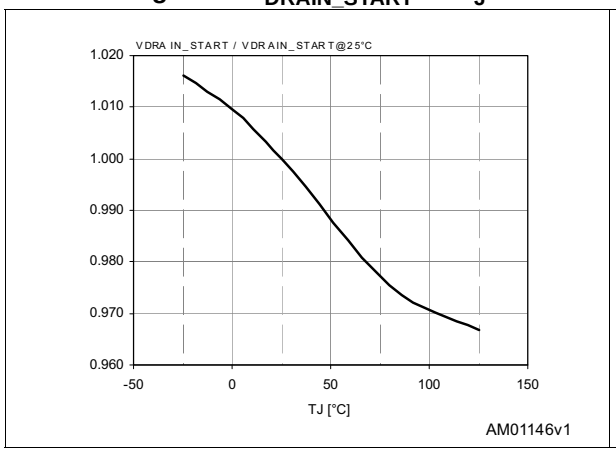


Figure 7. H_{COMP} vs T_J

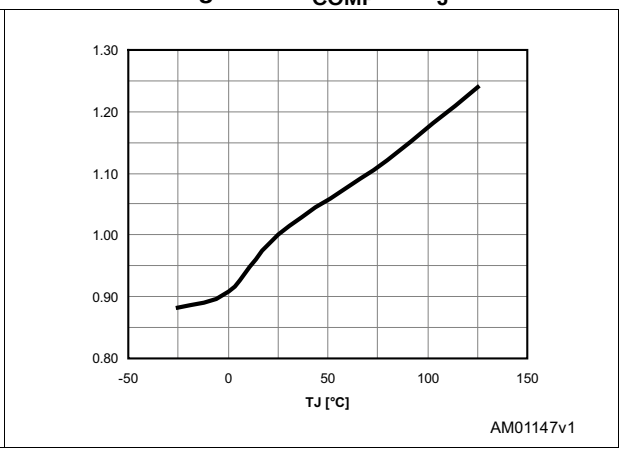


Figure 8. G_M vs T_J

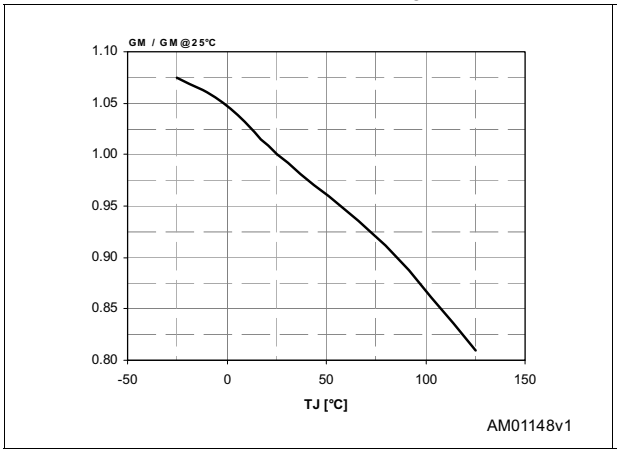


Figure 9. V_{REF_FB} vs T_J

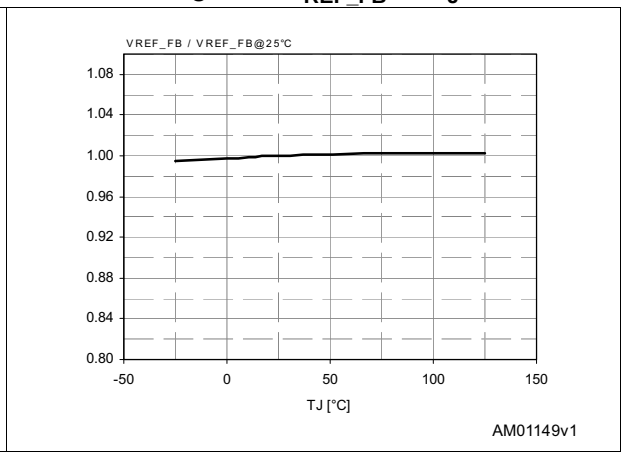


Figure 10. I_{COMP} vs T_J

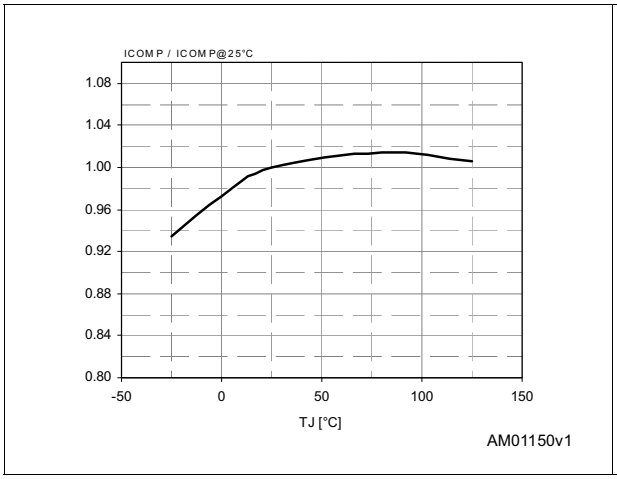


Figure 11. Operating supply current (no switching) vs T_J

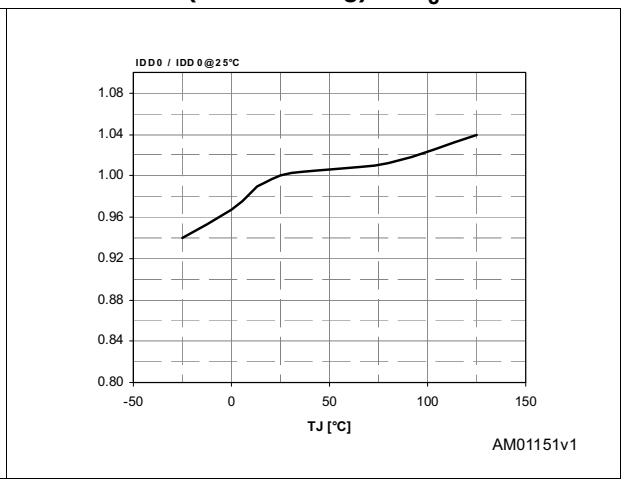


Figure 12. Operating supply current (switching) vs T_J

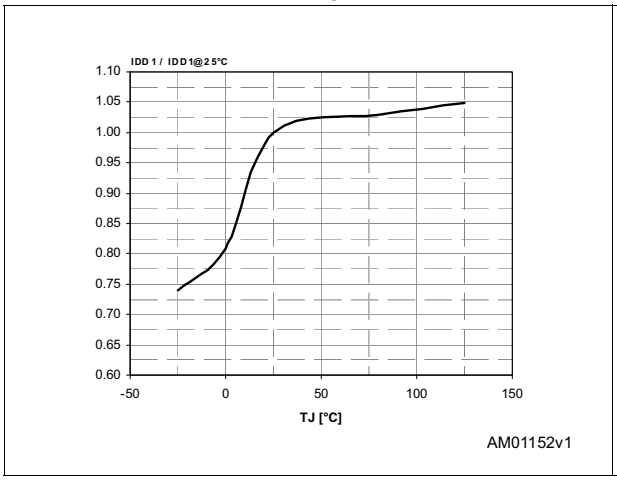


Figure 13. IDlim vs R_{LIM}

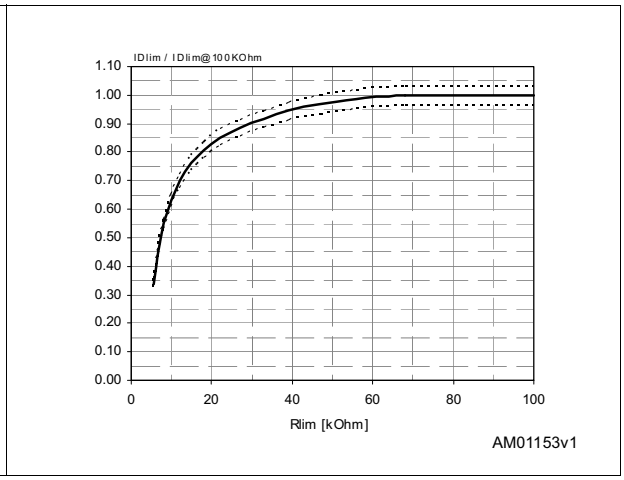


Figure 14. Power MOSFET on-resistance vs T_J

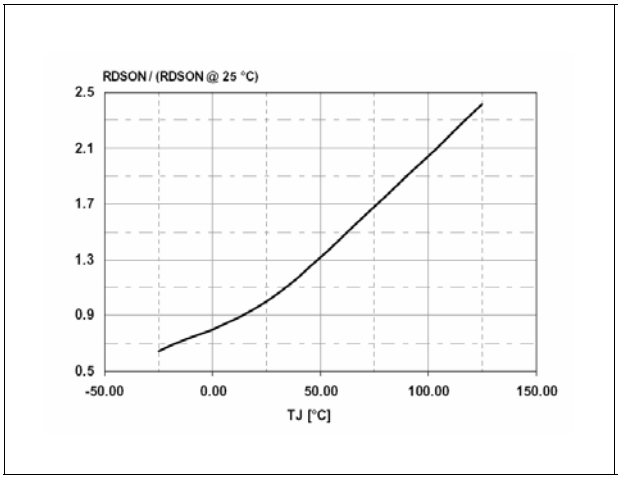


Figure 15. Power MOSFET break down voltage vs T_J

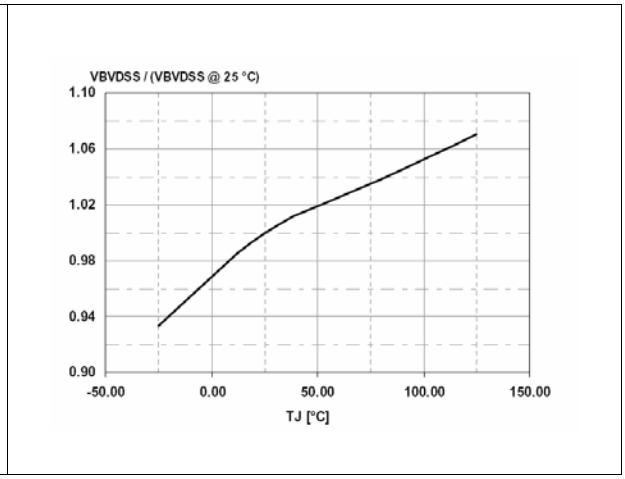
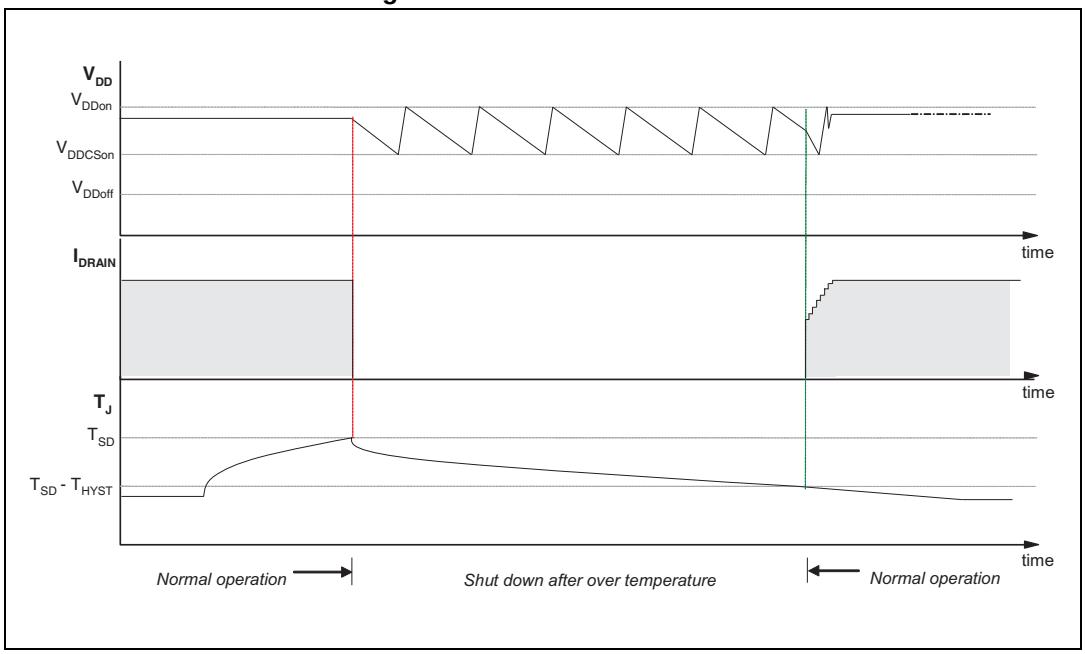


Figure 16. Thermal shutdown



6 Typical circuit

Figure 17. Buck converter

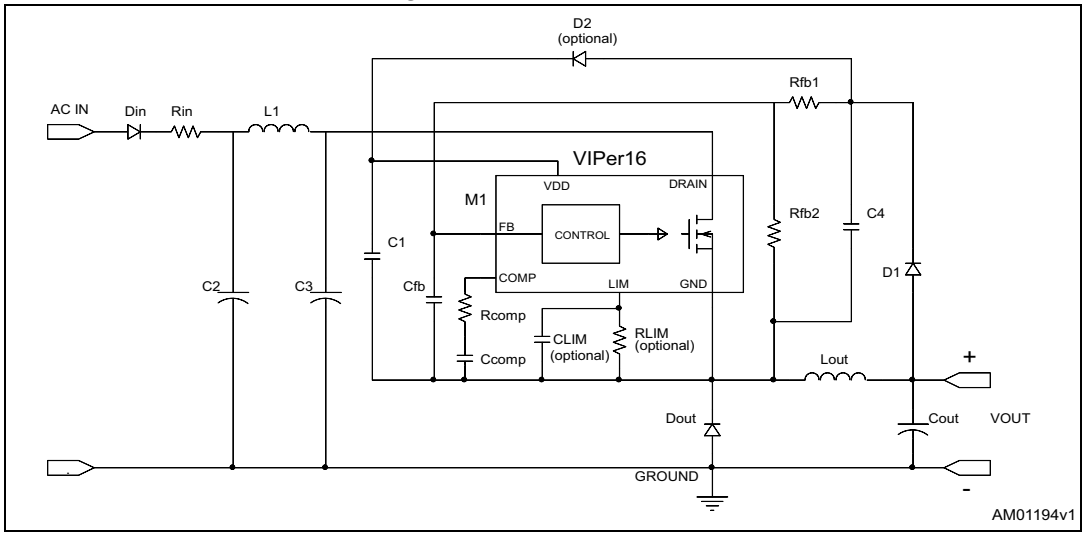


Figure 18. Buck boost converter

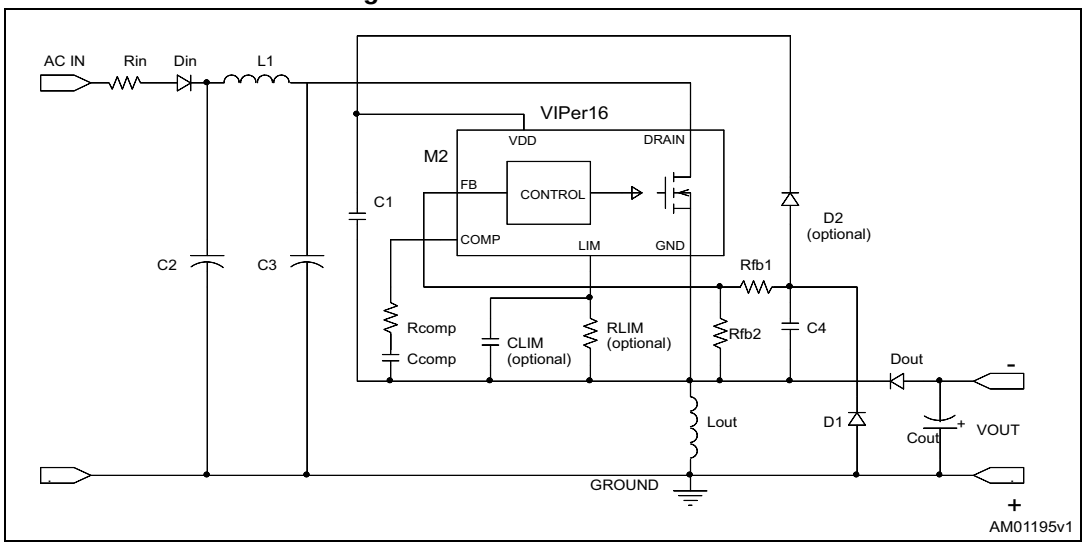


Figure 19. Flyback converter (primary regulation)

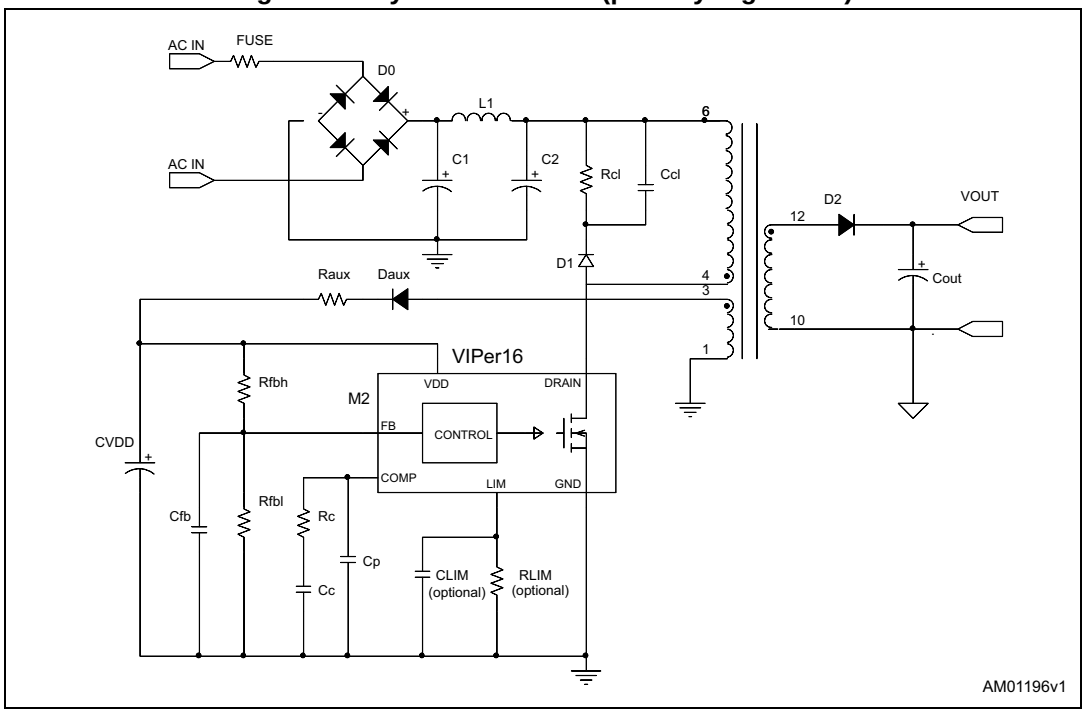
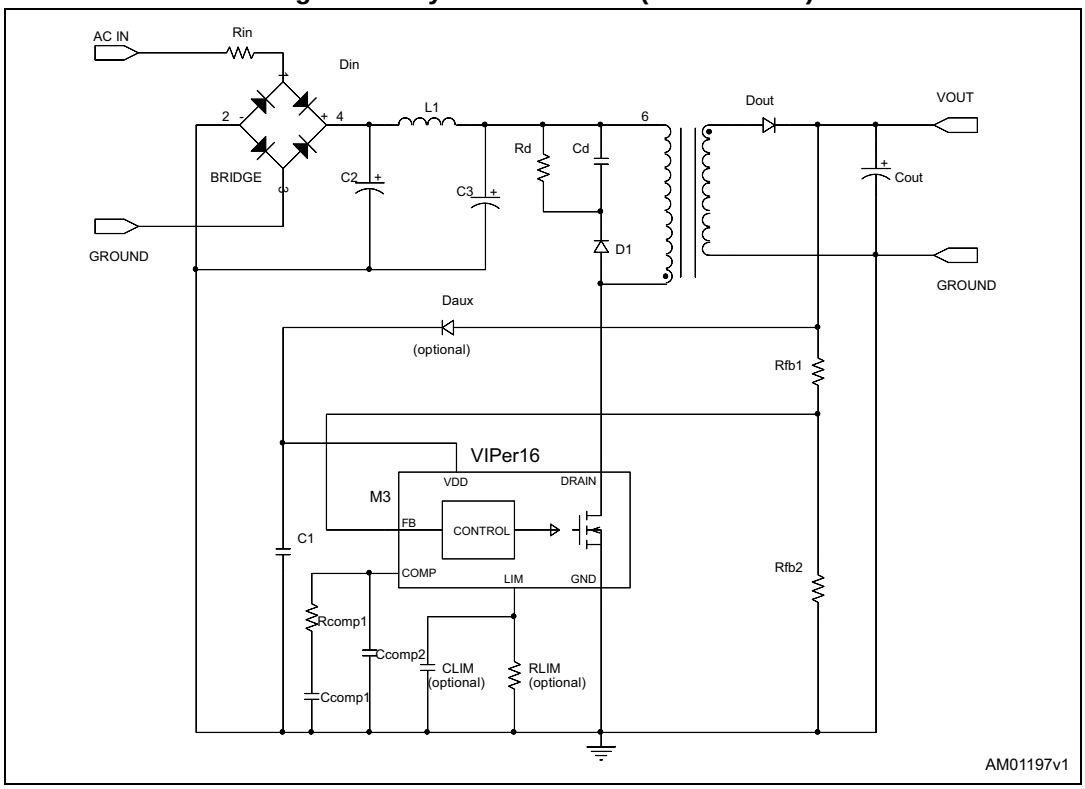


Figure 20. Flyback converter (non isolated)



7 Power section

The power section is implemented with an n-channel power MOSFET with a breakdown voltage of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω. It includes a SenseFET structure to allow a virtually lossless current sensing and the thermal sensor.

The gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-ON and turn-OFF in order to minimize common mode EMI. During UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned ON accidentally.

8 High voltage current generator

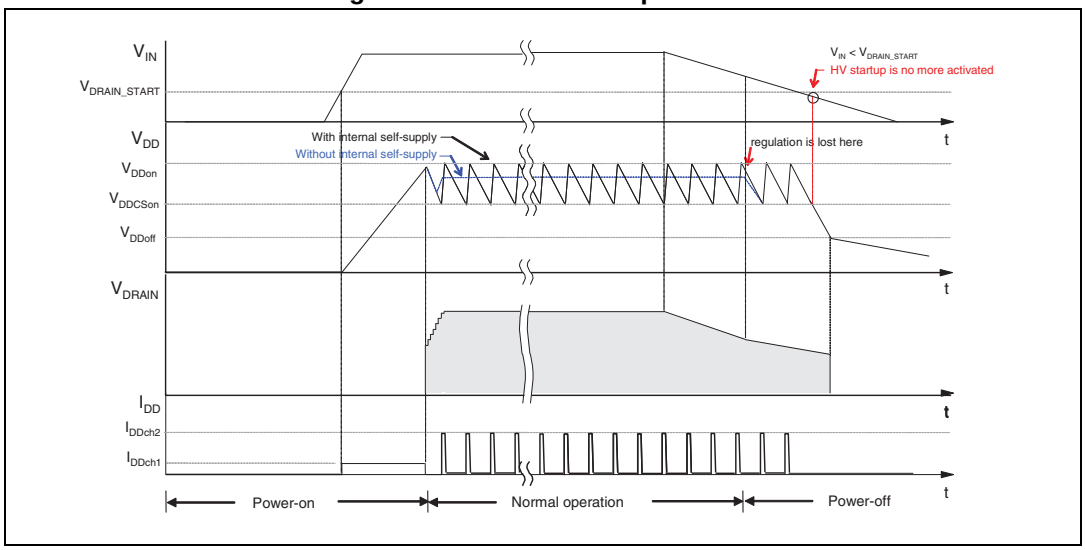
The high voltage current generator is supplied by the DRAIN pin. At the first start up of the converter it is enabled when the voltage across the input bulk capacitor reaches the V_{DRAIN_START} threshold, sourcing a I_{DDch1} current (see *Table 7 on page 8*); as the V_{DD} voltage reaches the V_{DDon} threshold, the power section starts switching and the high voltage current generator is turned OFF. The VIPer16 is powered by the energy stored in the V_{DD} capacitor.

In steady state condition, if the self biasing function is used, the high voltage current generator is activated between V_{DDCSon} and V_{DDon} (see *Table 7 on page 8*), delivering I_{DDch2}, see *Table 7 on page 8* to the V_{DD} capacitor during the MOSFET off time (see *Figure 21 on page 16*).

The device can also be supplied through the auxiliary winding; in this case the high voltage current source is disabled during steady-state operation, provided that VDD is above V_{DDCSon}.

At converter power-down, the V_{DD} voltage drops and the converter activity stops as it falls below V_{DDoff} threshold (see *Table 7 on page 8*).

Figure 21. Power on and power off



9 Oscillator

The switching frequency is internally fixed at 60 kHz (part number VIPER16LN or LD) or 115 kHz (part number VIPER16HN or HD).

In both cases the switching frequency is modulated by approximately ±4 kHz (60 kHz version) or ±8 kHz (115 kHz version) at 230 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of sideband harmonics having the same energy on the whole but smaller amplitudes.

10 Soft start-up

During the converters' start-up phase, the soft-start function progressively increases the cycle-by-cycle drain current limit, up to the default value I_{Dlim}. By this way the drain current is further limited and the output voltage is progressively increased reducing the stress on the secondary diode. The soft-start time is internally fixed to t_{SS}, see typical value on *Table 8 on page 9*, and the function is activated for any attempt of converter start-up and after a fault event.

This function helps prevent transformers' saturation during start-up and short-circuit.

11 Adjustable current limit set point

The VIPer16 includes a current mode PWM controller: cycle by cycle the drain current is sensed through the integrated resistor R_{SENSE} and the voltage is applied to the non inverting input of the PWM comparator, see *Figure 2 on page 4*. As soon as the sensed voltage is equal to the voltage derived from the COMP pin, the power MOSFET is switched OFF.

In parallel with the PWM operations, the comparator OCP, see *Figure 2 on page 4*, checks the level of the drain current and switch OFF the power MOSFET in case the current is higher than the threshold I_{Dlim}, see *Table 8 on page 9*.

The level of the drain current limit, I_{Dlim}, can be reduced depending from the sunk current from the pin LIM. The resistor R_{LIM}, between LIM and GND pins, fixes the current sunk and than the level of the current limit, I_{Dlim}, see *Figure 13 on page 12*.

When the LIM pin is left open or if the R_{LIM} has an high value (i.e. > 80 kΩ) the current limit is fixed to its default value, I_{Dlim}, as reported on *Table 8 on page 9*.

12 FB pin and COMP pin

The device can be used both in non-isolated and in isolated topology. In case of non-isolated topology, the feedback signal from the output voltage is applied directly to the FB pin as inverting input of the internal error amplifier having the reference voltage, V_{REF_FB}, see the *Table 8 on page 9*.

The output of the error amplifier sources and sinks the current, I_{COMP}, respectively to and from the compensation network connected on the COMP pin. This signal is then compared, in the PWM comparator, with the signal coming from the SenseFET; the power MOSFET is switched off when the two values are the same on cycle by cycle basis. See the *Figure 2 on page 4* and the *Figure 22 on page 18*.

When the power supply output voltage is equal to the error amplifier reference voltage, V_{REF_FB}, a single resistor has to be connected from the output to the FB pin. For higher output voltages the external resistor divider is needed. If the voltage on FB pin is accidentally left floating, an internal pull-up protects the controller.

The output of the error amplifier is externally accessible through the COMP pin and it's used for the loop compensation: usually an RC network.

As reported on *Figure 22 on page 18*, in case of isolated power supply, the internal error amplifier has to be disabled (FB pin shorted to GND). In this case an internal resistor is connected between an internal reference voltage and the COMP pin, see the *Figure 22 on page 18*. The current loop has to be closed on the COMP pin through the opto-transistor in parallel with the compensation network. The V_{COMP} dynamics ranges is between V_{COMPL} and V_{COMPH} as reported on *Figure 23 on page 19*.

When the voltage V_{COMP} drops below the voltage threshold V_{COMPL}, the converter enters burst mode, see *Section 13 on page 19*.

When the voltage V_{COMP} rises above the V_{COMPH} threshold, the peak drain current will reach its limit, as well as the deliverable output power.

Figure 22. Feedback circuit

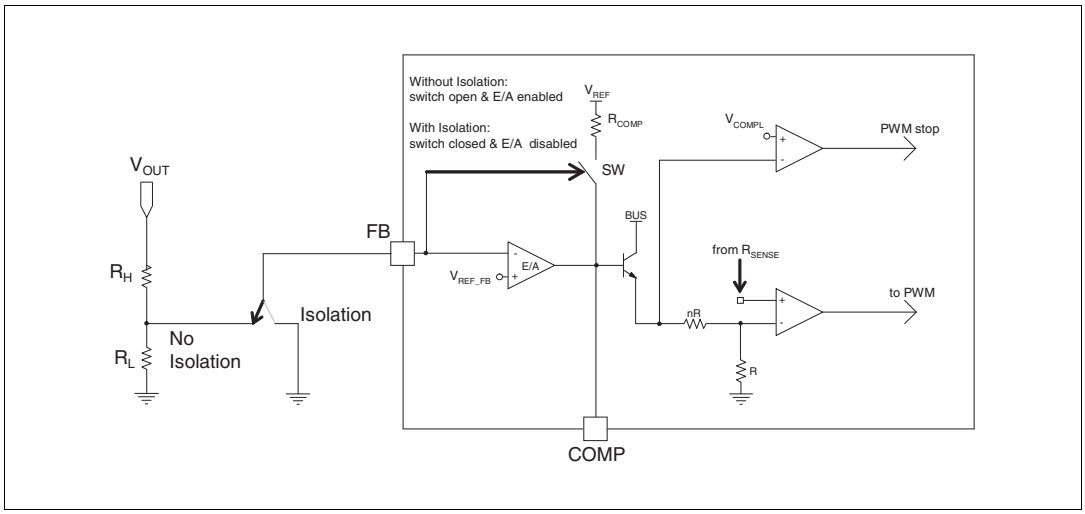
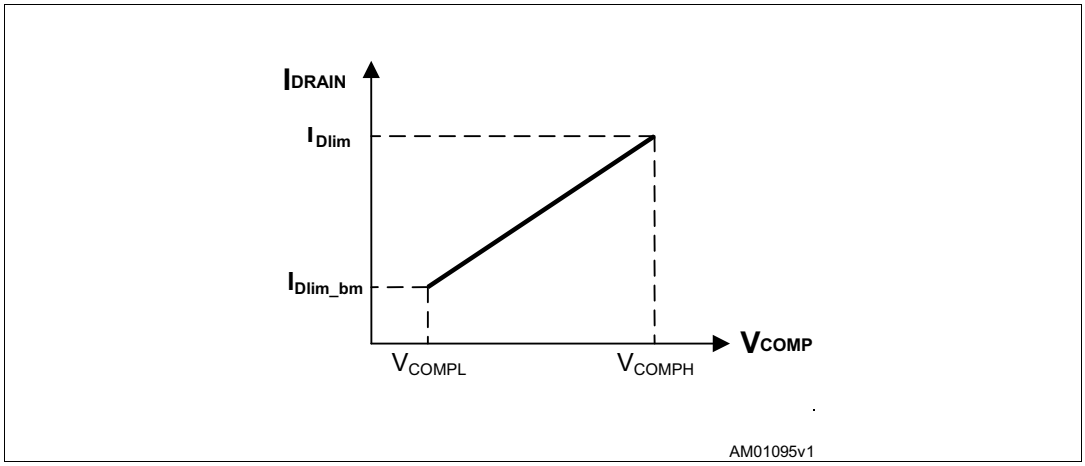


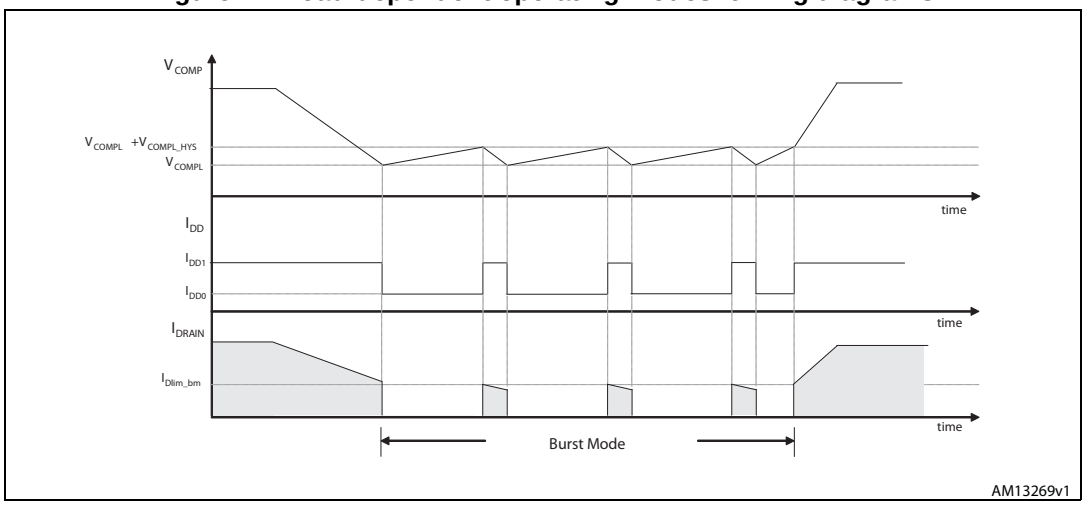
Figure 23. COMP pin voltage versus I_{DRAIN}



13 Burst mode

When the voltage V_{COMP} drops below the threshold, V_{COMPL}, the power MOSFET is kept in OFF state and the consumption is reduced to I_{DD0} current, as reported on *Table 7 on page 8*. As reaction at the energy delivery stop, the V_{COMP} voltage increases and as soon as it exceeds the threshold V_{COMPL} + V_{COMPL_HYS}, the converter starts switching again with consumption level equal to I_{DD1} current. This ON-OFF operation mode, referred to as “burst mode” and reported on *Figure 24 on page 19*, reduces the average frequency, which can go down even to a few hundreds hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. During the burst mode, the drain current limit is reduced to the value I_{Dlim_bm} (reported on *Table 8 on page 9*) in order to avoid the audible noise issue.

Figure 24. Load-dependent operating modes: timing diagrams



14 Automatic auto restart after overload or short-circuit

The overload protection is implemented in automatic way using the integrated up-down counter. Every cycle, it is incremented or decremented depending if the current logic detects the limit condition or not. The limit condition is the peak drain current, I_{Dlim} , reported on *Table 8 on page 9* or the one set by the user through the R_{LIM} resistor, as reported in *Figure 13 on page 12*. After the reset of the counter, if the peak drain current is continuously equal to the level I_{Dlim}, the counter will be incremented till the fixed time, t_{OVL}, after that will be disabled the power MOSFET switch ON. It will be activated again, through the soft start, after the $t_{RESTART}$ time, see the *Figure 25* and *Figure 26 on page 20* and the mentioned time values on *Table 8 on page 9*.

In case of overload or short-circuit event, the power MOSFET switching will be stopped after a time that depends from the counter and that can be as maximum equal to t_{OVL}. The protection will occur in the same way until the overload condition is removed, see *Figure 25* and *Figure 26 on page 20*. This protection ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoiding the IC overheating in case of repeated overload events. If the overload is removed before the protection tripping, the counter will be decremented cycle by cycle down to zero and the IC will not be stopped.

Figure 25. Timing diagram: OLP sequence (IC externally biased)

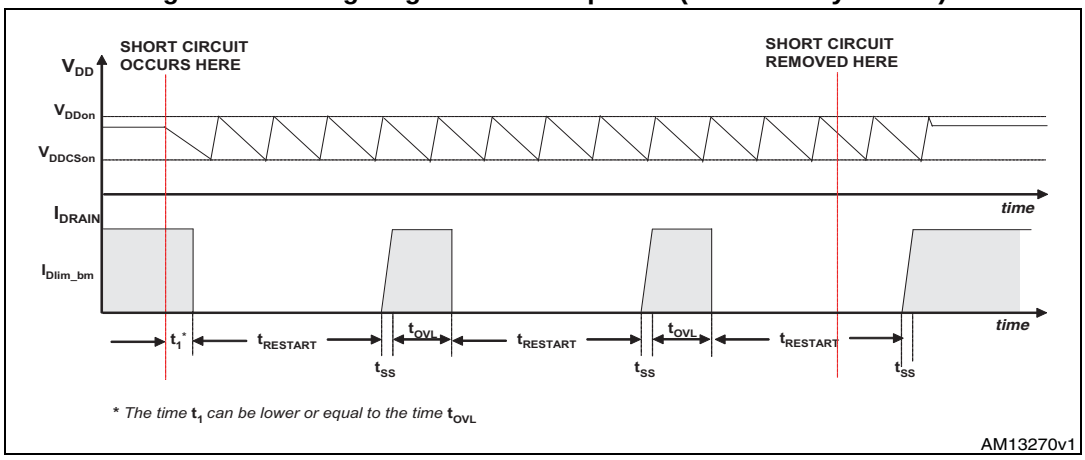
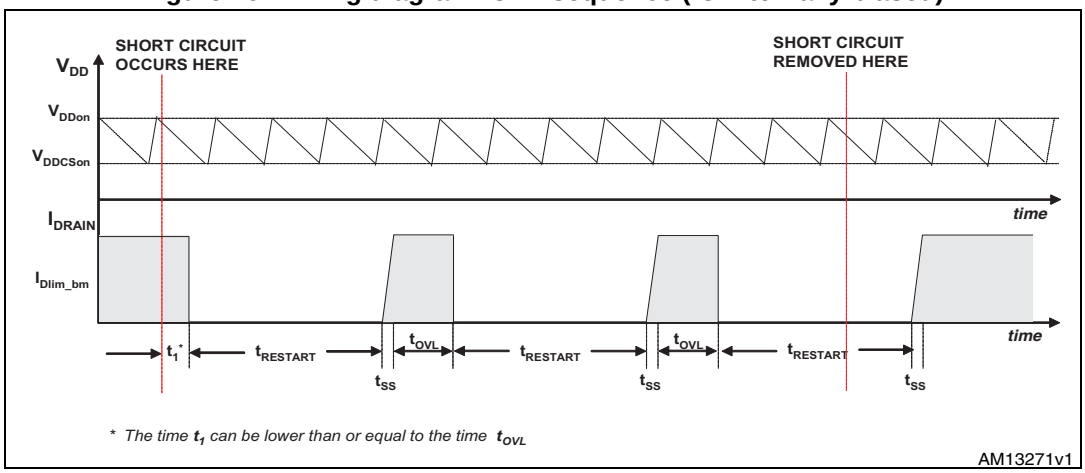


Figure 26. Timing diagram: OLP sequence (IC internally biased)



15 Open loop failure protection

In case the power supply is built in fly-back topology and the VIPer16 is supplied by an auxiliary winding, as shown in *Figure 27 on page 21* and *Figure 28 on page 22*, the converter is protected against feedback loop failure or accidental disconnections of the winding.

The following description is applicable for the schematics of *Figure 27 on page 21* and *Figure 28 on page 22*, respectively the non-isolated fly-back and the isolated fly-back.

If R_H is opened or R_L is shorted, the VIPer16 works at its drain current limitation. The output voltage, V_{OUT}, will increase and so the auxiliary voltage, V_{AUX}, which is coupled with the output through the secondary-to-auxiliary turns ratio.

As the auxiliary voltage increases up to the internal V_{DD} active clamp, $V_{DDclamp}$ (the value is reported on *Table 8 on page 9*) and the clamp current injected on VDD pin exceeds the latch threshold, I_{DDol} (the value is reported on *Table 8 on page 9*), a fault signal is internally generated.

In order to distinguish an actual malfunction from a bad auxiliary winding design, both the above conditions (drain current equal to the drain current limitation and current higher than I_{DDol} through VDD clamp) have to be verified to reveal the fault.

If R_L is opened or R_H is shorted, the output voltage, V_{OUT}, will be clamped to the reference voltage V_{REF_FB} (in case of non isolated fly-back) or to the external TL voltage reference (in case of isolated fly-back).

Figure 27. FB pin connection for non-isolated fly-back

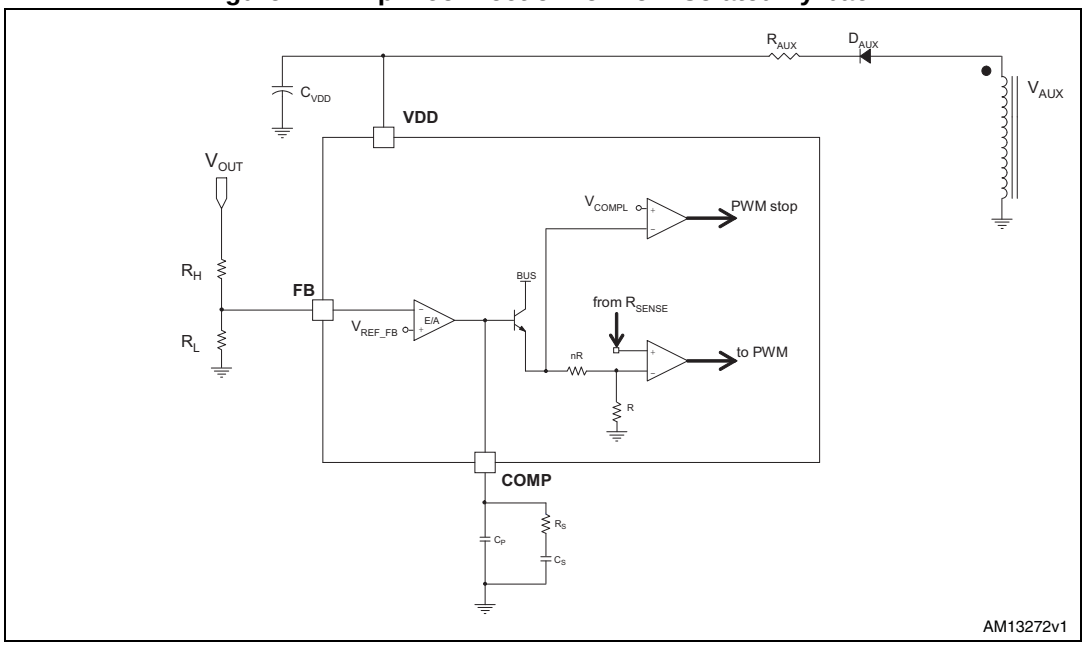
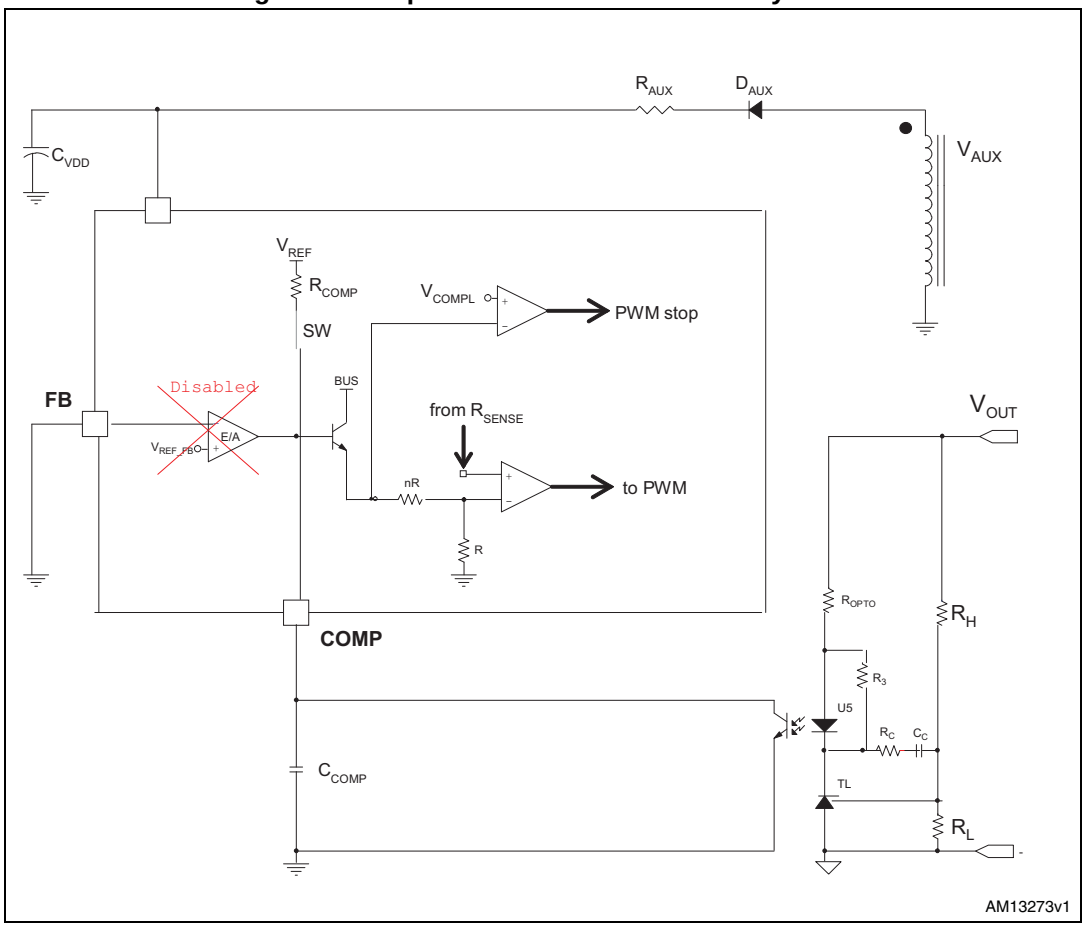


Figure 28. FB pin connection for isolated fly-back



16 Layout guidelines and design recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the VIPer16 as well. Also some trick can be used to make the design rugged versus external influences.

Careful component placing, correct traces routing, appropriate traces widths and compliance with isolation distances are the major issues.

The main reasons to have a proper PCB routing are:

- Provide a noise free path for the signal ground and for the internal references, ensuring good immunity against external noises and switching noises
- Minimize the pulsed loops (both primary and secondary) to reduce the electromagnetic interferences, both radiated and conducted and passing more easily the EMC regulations.

The below list can be used as guideline when designing a SMPS using VIPer16.

- Signal ground routing should be routed separately from power ground and, in general, from any pulsed high current loop;
- Connect all the signal ground traces to the power ground, using a single "star point", placed close to the IC GND pin;
- With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VDD capacitor on the auxiliary return and then to the main GND using a single track;
- The compensation network should be connected as close as possible to the COMP pin, maintaining the trace for the GND as short as possible;
- A small bypass capacitor (a few hundreds pF up to 0.1 µF) to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor should be used, placed as close as possible to the VDD pin;
- When using SO16 package it is recommended to connect the pin 4 to GND pin, using a signal track, in order to improve the noise immunity. This is highly recommended in case of high nosily environment;
- An optional capacitor can be connected on the LIM pin in order to improve the IC noise immunity. It is strongly recommended to don't exceed 470nF.
- The IC thermal dissipation takes place through the drain pins. An adequate heat sink copper area has to be designed under the drain pins to improve the thermal dissipation;
- It is not recommended to place large copper areas on the GND pins.
- Minimize the area of the pulsed loops (primary, RCD and secondary loops), in order to reduce its parasitic self- inductance and the radiated electromagnetic field: this will greatly reduce the electromagnetic interferences produced by the power supply during the switching.

Figure 29. Suggested routing for converter: flyback case

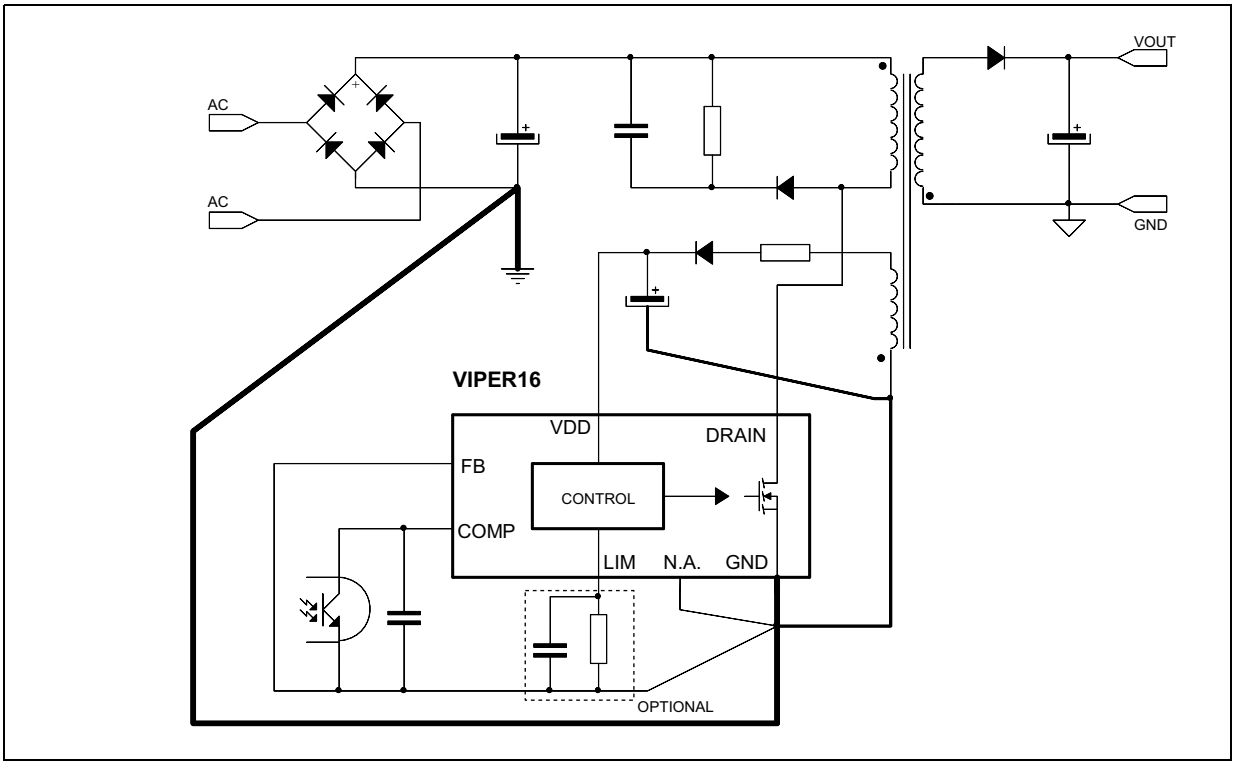
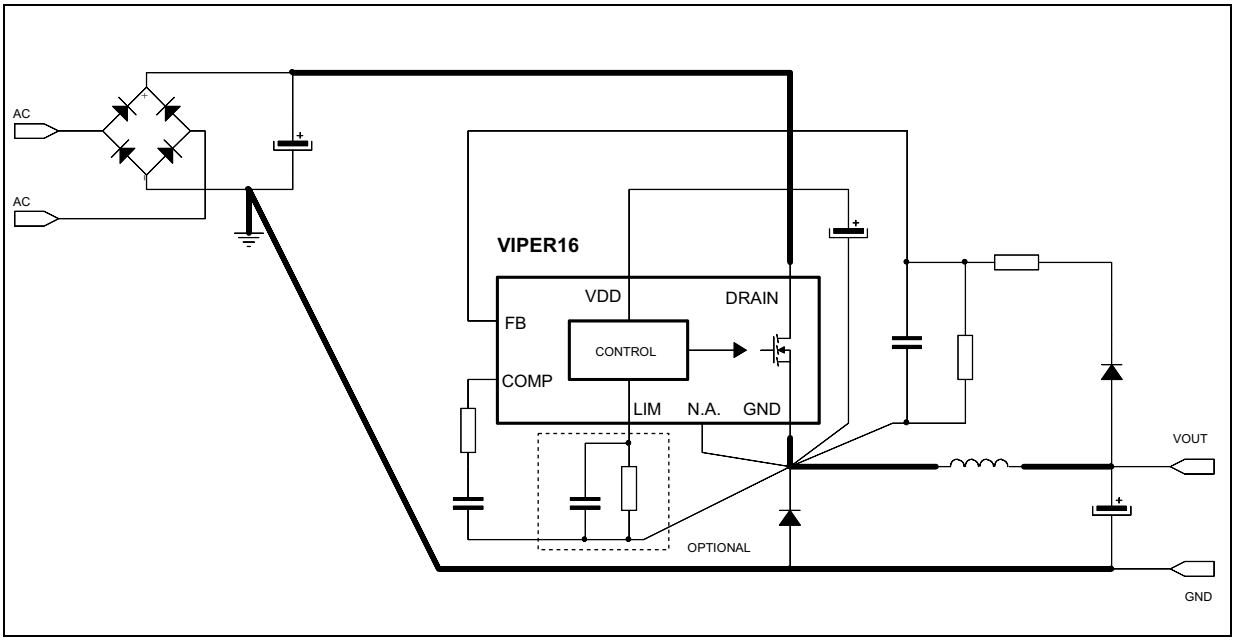


Figure 30. Suggested routing for converter: buck case



17 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 31. DIP-7 package dimensions

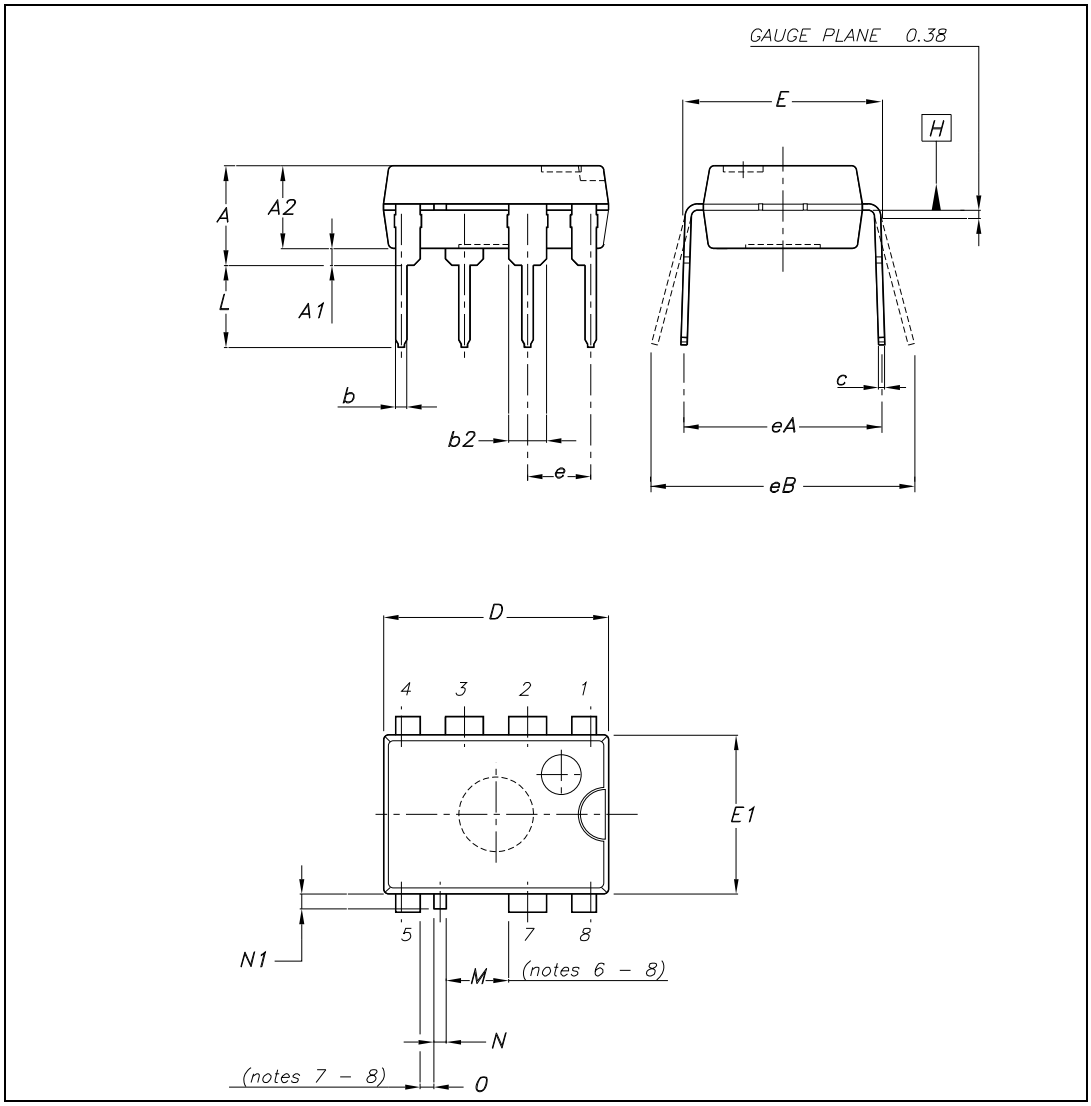


Table 9. DIP-7 mechanical data

Dim.	mm		
	Typ	Min	Max
A			5,33
A1		0,38	
A2	3,30	2,92	4,95
b	0,46	0,36	0,56
b2	1,52	1,14	1,78
c	0,25	0,20	0,36
D	9,27	9,02	10,16
E	7,87	7,62	8,26
E1	6,35	6,10	7,11
e	2,54		
eA	7,62		
eB			10,92
L	3,30	2,92	3,81
M (6)(8)	2,508		
N	0,50	0,40	0,60
N1			0,60
O (7)(8)	0,548		

1- The leads size is comprehensive of the thickness of the leads finishing material.

2- Dimensions do not include mold protrusion, not to exceed 0,25 mm in total (both side).

3- Package outline exclusive of metal burrs dimensions.

4- Datum plane “H” coincident with the bottom of lead, where lead exits body.

5- Ref. POA MOTHER doc. 0037880

6- Creepage distance > 800 V

7- Creepage distance 250 V

8- Creepage distance as shown in the 664-1 CEI / IEC standard.

Figure 32. SO16N package dimensions

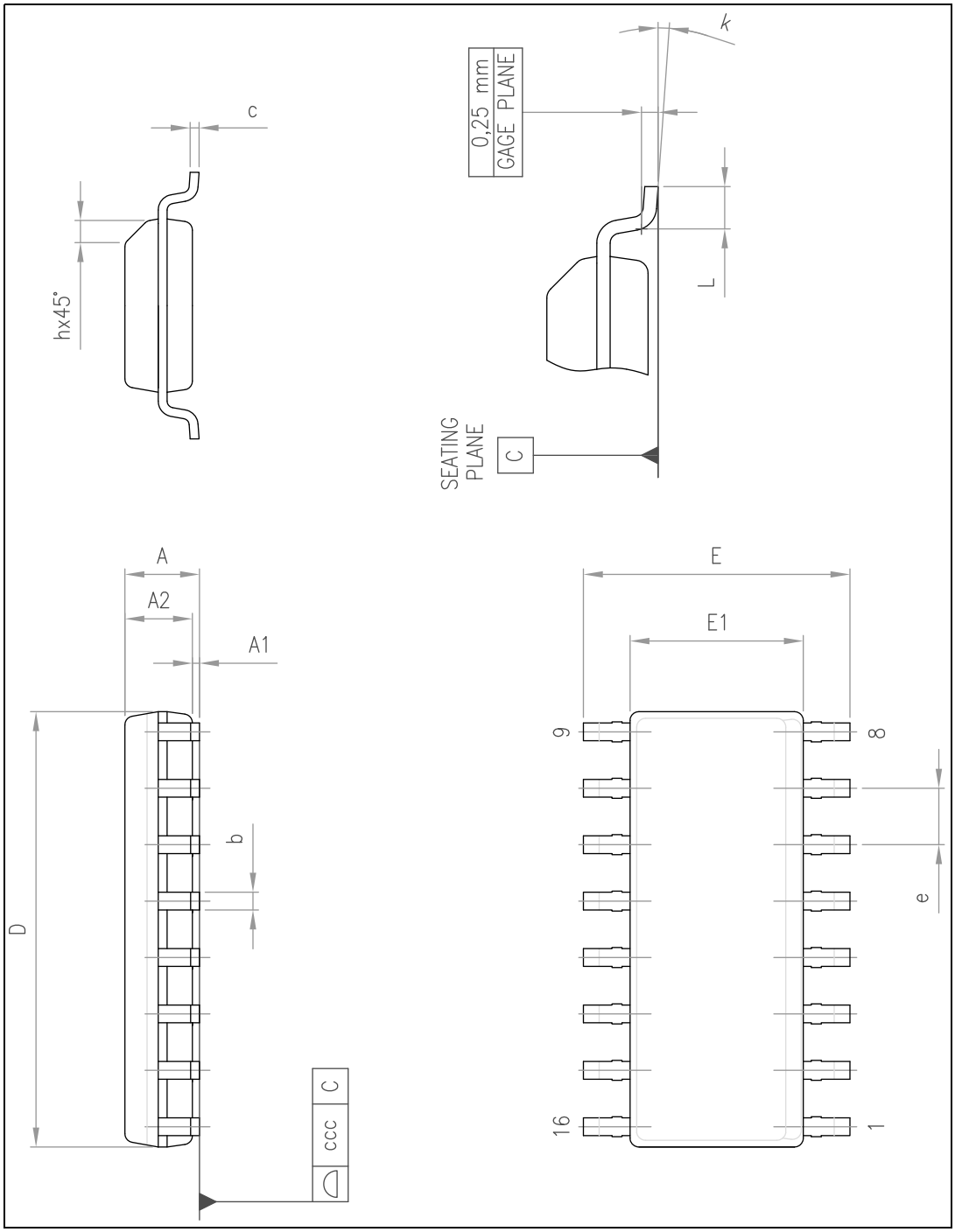


Table 10. SO16N mechanical data

Dim.	mm		
	Min	Typ	Max
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

18 Revision history

Table 11. Document revision history

Date	Revision	Changes
21-Jan-2009	1	Initial release
07-Dec-2009	2	Updated *Figure 7 on page 11*
14-May-2010	3	Updated *Figure 3 on page 5* and *Table 3 on page 5*
26-Aug-2010	4	Updated *Table 3 on page 5*, *Figure 16 on page 13* and *Figure 21 on page 16*
10-Oct-2011	5	Updated *Figure 32 on page 27* and *Table 7 on page 8*
26-May-2014	6	Updated the features in cover page, *Table 3: Pin description*, *Table 4: Absolute maximum ratings*, *Table 6: Power section*, *Table 7: Supply section*. Modified *Figure 17*, *18*, *19* and *20*. Added *Section 16: Layout guidelines and design recommendations*. Minor text changes.
13-Jun-2014	7	Updated *Table 3: Pin description* and *Table 6: Power section*. Minor text changes.

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