



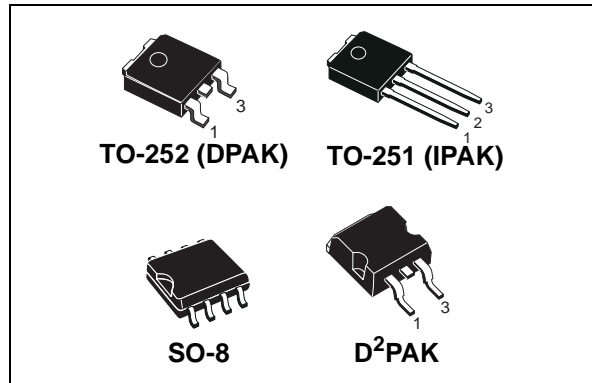
VNB14NV04, VND14NV04 VND14NV04-1, VNS14NV04

"OMNIFET II"
fully autoprotected Power MOSFET

Features

TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNB14NV04 VND14NV04 VND14NV04-1 VNS14NV04	35 m Ω	12 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



Description

The VNB14NV04, VND14NV04, VND14NV04-1 and VNS14NV04 are monolithic devices made using STMicroelectronics VIPower™ M0 technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Tube	Tube (lead free)	Tape and reel	Tape and reel (lead free)
D²PAK	VNB14NV04	VNB14NV04-E	VNB14NV0413TR	VNB14NV04TR-E
TO-252 (DPAK)	VND14NV04	VND14NV04-E	VND14NV0413TR	VND14NV04TR-E
TO-251 (IPAK)	VND14NV04-1	VND14NV04-1-E	-	-
SO-8	VNS14NV04	-	-	-

Contents

1	Block diagram	5
2	Electrical specification	6
2.1	Absolute maximum rating	6
2.2	Thermal data	7
2.3	Electrical characteristics	7
3	Protection features	9
4	Package thermal data	18
4.1	DPAK thermal data	18
4.2	SO-8 thermal data	20
4.3	D ² PAK thermal data	21
5	Package information	24
5.1	ECOPACK®	24
5.2	TO-251 (IPAK) mechanical data	24
5.3	D ² PAK mechanical data	25
5.4	TO-252 (DPAK) mechanical data	27
5.5	SO-8 mechanical data	28
6	Revision history	30

List of tables

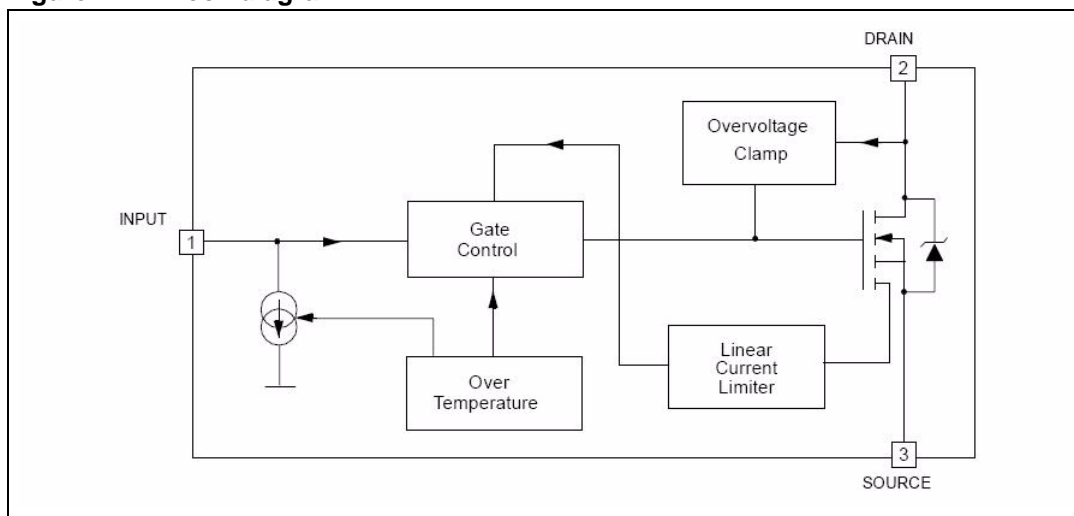
Table 1.	Device summary	1
Table 2.	Absolute maximum rating	6
Table 3.	Thermal data	7
Table 4.	Electrical characteristics	7
Table 5.	DPAK thermal parameter	19
Table 6.	D ² PAK thermal parameter	22
Table 7.	TO-251 (IPAK) mechanical data	24
Table 8.	D ² PAK mechanical data	26
Table 9.	TO-252 (DPAK) mechanical data	27
Table 10.	SO-8 mechanical data	28
Table 11.	Document revision history	30

List of figures

Figure 1.	Block diagram	5
Figure 2.	Current and voltage conventions	6
Figure 3.	Switching time test circuit for resistive load	10
Figure 4.	Test circuit for diode recovery times	10
Figure 5.	Unclamped inductive load test circuits	11
Figure 6.	Unclamped inductive waveforms	11
Figure 7.	Input charge test circuit.	11
Figure 8.	Source-drain diode forward characteristics	12
Figure 9.	Static drain source on resistance	12
Figure 10.	Derating curve	12
Figure 11.	Static drain-source on resistance vs. input voltage (part 1/2)	12
Figure 12.	Static drain-source on resistance vs. input voltage (part 2/2)	12
Figure 13.	Transconductance	12
Figure 14.	Static drain-source on resistance vs. i_d	13
Figure 15.	Transfer characteristics	13
Figure 16.	Turn-on current slope (part 1/2)	13
Figure 17.	Turn-on current slope (part 2/2)	13
Figure 18.	Input voltage vs. input charge.	13
Figure 19.	Turn-off drain source voltage slope (part 1/2).	13
Figure 20.	Turn-off drain source voltage slope (part 2/2).	14
Figure 21.	Capacitance variations	14
Figure 22.	Switching time resistive load (part 1/2)	14
Figure 23.	Switching time resistive load (part 2/2)	14
Figure 24.	Output characteristics	14
Figure 25.	Normalized on resistance vs. temperature	14
Figure 26.	Normalized input threshold voltage vs. temperature	15
Figure 27.	Current limit vs. junction temperatures	15
Figure 28.	Step response current limit.	15
Figure 29.	DPAK maximum turn-off current versus load inductance	16
Figure 30.	DPAK demagnetization.	16
Figure 31.	D ² PAK maximum turn-off current versus load inductance	17
Figure 32.	D ² PAK demagnetization.	17
Figure 33.	DPAK PC board ⁽¹⁾	18
Figure 34.	DPAK $R_{thj-amb}$ vs PCB copper area in open box free air condition.	18
Figure 35.	DPAK thermal impedance junction ambient single pulse	19
Figure 36.	Thermal fitting model of an OMNIFET II in DPAK.	19
Figure 37.	SO-8 PC board ⁽¹⁾	20
Figure 38.	SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition	20
Figure 39.	D ² PAK PC board ⁽¹⁾	21
Figure 40.	D ² PAK $R_{thj-amb}$ vs PCB copper area in open box free air condition.	21
Figure 41.	D ² PAK thermal impedance junction ambient single pulse	22
Figure 42.	Thermal fitting model of an OMNIFET II in D ² PAK.	22
Figure 43.	TO-251 (IPAK) package dimension	24
Figure 44.	D ² PAK package dimension	25
Figure 45.	TO-252 (DPAK) package dimension	27
Figure 46.	SO-8 package dimension	28

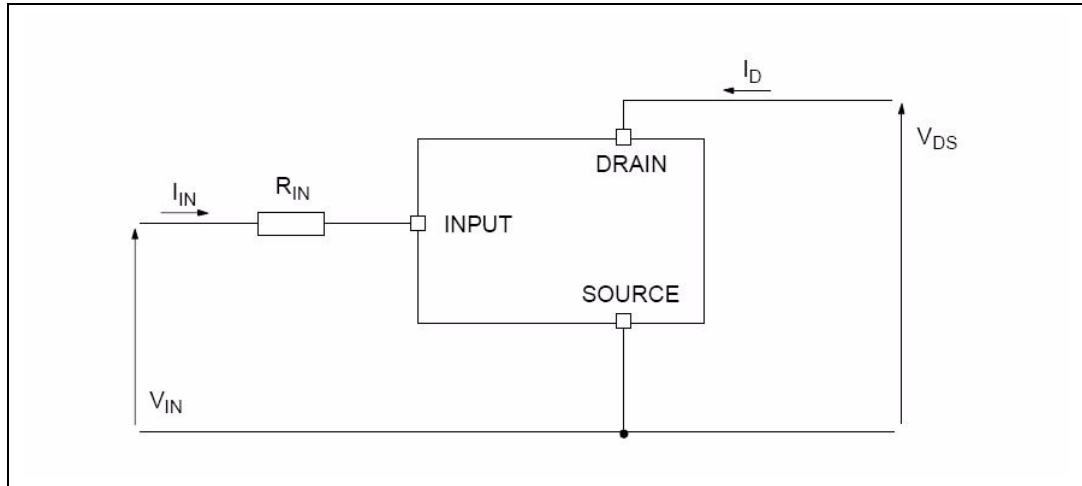
1 Block diagram

Figure 1. Block diagram



2 Electrical specification

Figure 2. Current and voltage conventions



2.1 Absolute maximum rating

Table 2. Absolute maximum rating

Symbol	Parameter	Value				Unit
		SO-8	DPAK	IPAK	D ² PAK	
V_{DS}	Drain-source voltage ($V_{IN}=0$ V)	Internally clamped				V
V_{IN}	Input voltage	Internally clamped				V
I_{IN}	Input current	+/-20				mA
$R_{IN\ MIN}$	Minimum input series impedance	10				Ω
I_D	Drain current	Internally limited				A
I_R	Reverse DC output current	-15				A
V_{ESD1}	Electrostatic discharge ($R=1.5$ K Ω , $C=100$ pF)	4000				V
V_{ESD2}	Electrostatic discharge on output pin only ($R=330$ Ω , $C=150$ pF)	16500				V
P_{tot}	Total dissipation at $T_c=25$ °C	4.6	74	74	74	W
E_{MAX}	Maximum switching energy ($L=0.4$ mH; $R_L=0$ Ω ; $V_{bat}=13.5$ V; $T_{jstart}=150$ °C; $I_L=18$ A)		93		93	mJ
T_j	Operating junction temperature	Internally limited				°C
T_c	Case operating temperature	Internally limited				°C
T_{stg}	Storage temperature	-55 to 150				°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		SO-8	DPAK	IPAK	D ² PAK	
R _{thj-case}	Thermal resistance junction-case max		1.7	1.7	1.7	°C/W
R _{thj-lead}	Thermal resistance junction-lead max	27				°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	90 ⁽¹⁾	65 ⁽¹⁾	102	52 ⁽¹⁾	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm² of Cu (at least 35 μm thick) connected to all DRAIN pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

-40 < T_j < 150 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off						
V _{CLAMP}	Drain-source clamp voltage	V _{IN} =0 V; I _D =7 A	40	45	55	V
V _{CLTH}	Drain-source clamp threshold voltage	V _{IN} =0 V; I _D =2 mA	36			V
V _{INTH}	Input threshold voltage	V _{DS} =V _{IN} ; I _D =1 mA	0.5		2.5	V
I _{ISS}	Supply current from input pin	V _{DS} =0 V; V _{IN} =5 V		100	150	μA
V _{INCL}	Input-source clamp voltage	I _{IN} =1 mA I _{IN} =-1 mA	6 -1.0	6.8	8 -0.3	V
I _{DSS}	Zero input voltage drain current (V _{IN} =0 V)	V _{DS} =13 V; V _{IN} =0 V; T _j =25 °C V _{DS} =25 V; V _{IN} =0 V			30 75	μA
On						
R _{DS(on)}	Static drain-source on resistance	V _{in} = 5 V I _D = 7 A T _j = 25 °C V _{in} = 5 V I _D = 7 A			35 70	mΩ
Dynamic (T_j=25°C, unless otherwise specified)						
g _{fs} ⁽¹⁾	Forward transconductance	V _{DD} = 13 V I _D = 7 A		18		S
C _{oss}	Output capacitance	V _{DS} = 13 V f = 1 MHz V _{IN} = 0 V		400		pF
Switching						
t _{d(on)}	Turn-on delay time	V _{DD} = 15 V I _D = 7 A V _{gen} = 5 V R _{gen} = R _{IN MIN} = 10 Ω (see Figure 3)		80	250	ns
t _r	Rise time			350	1000	ns
t _{d(off)}	Turn-off delay time			450	1350	ns
t _f	Fall time			150	500	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ $I_D = 7\text{ A}$ $V_{gen} = 5\text{ V}$ $R_{gen} = 2.2\text{ K}\Omega$ (see Figure 3)		1.5	4.5	μs
t_r	Rise time			9.7	30.0	μs
$t_{d(off)}$	Turn-off delay time				25.0	μs
t_f	Fall time			10.2	30.0	μs
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{ V}$ $I_D = 7\text{ A}$ $V_{gen} = 5\text{ V}$ $R_{gen} = R_{IN\text{ MIN}} = 10\ \Omega$		16		A/ μs
Q_i	Total input charge	$V_{DD} = 12\text{ V}$ $I_D = 7\text{ A}$ $V_{in} = 5\text{ V}$; $I_{gen} = 2.13\text{ mA}$ (see Figure 7)		36.8		nC
Source drain diode						
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7\text{ A}$ $V_{in} = 0\text{ V}$		0.8		V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$; $di/dt = 40\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $L = 200\ \mu\text{H}$ (see test circuit, Figure 4)		300		ns
Q_{rr}	Reverse recovery charge			0.8		μC
I_{RRM}	Reverse recovery current			5		A
Protection						
I_{lim}	Drain current limit	$V_{IN} = 5\text{ V}$; $V_{DS} = 13\text{ V}$	12	18	24	A
t_{dlim}	Step response current limit	$V_{IN} = 5\text{ V}$; $V_{DS} = 13\text{ V}$		45		μs
T_{jsh}	Over temperature shutdown		150	175	200	$^{\circ}\text{C}$
T_{jrs}	Over temperature reset		135			$^{\circ}\text{C}$
I_{gf}	Fault sink current	$V_{IN} = 5\text{ V}$; $V_{DS} = 13\text{ V}$; $T_j = T_{jsh}$	10	15	20	mA
E_{as}	Single pulse avalanche energy	starting $T_j = 25\text{ }^{\circ}\text{C}$; $V_{DD} = 24\text{ V}$ $V_{IN} = 5\text{ V}$; $R_{gen} = R_{IN\text{ MIN}} = 10\ \Omega$; $L = 24\text{ mH}$ (see Figure 5 and Figure 6)	400			mJ

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50 KHz. The only difference from the user's standpoint is that a small DC current I_{SS} (typ. 100 μ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{jsh} .
- Over temperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Over temperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback: in the case of an over temperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf} , the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{SS} .

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 3. Switching time test circuit for resistive load

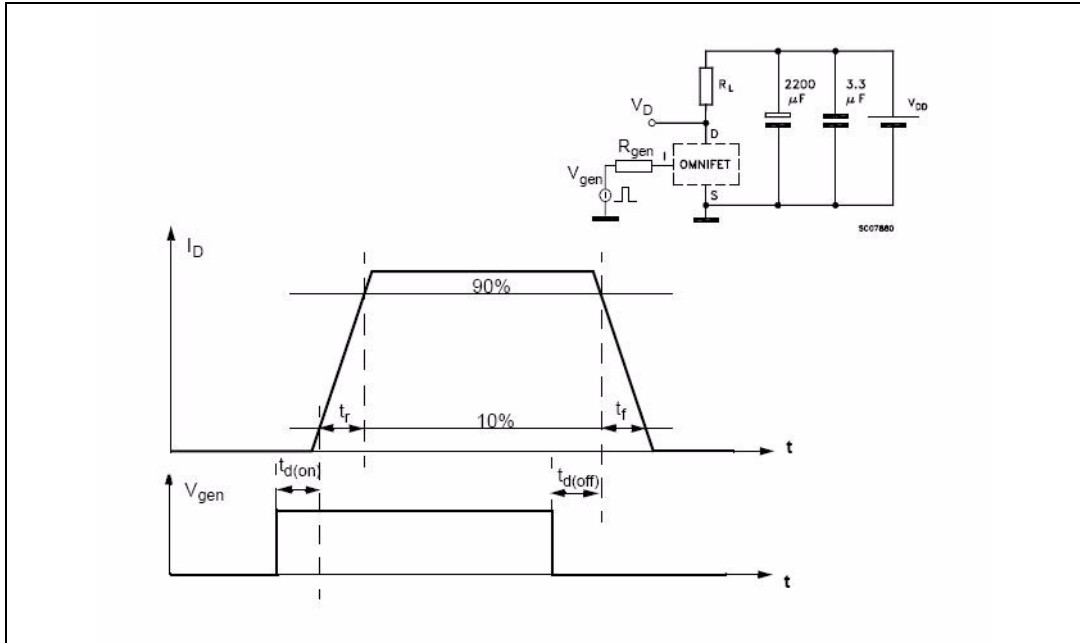


Figure 4. Test circuit for diode recovery times

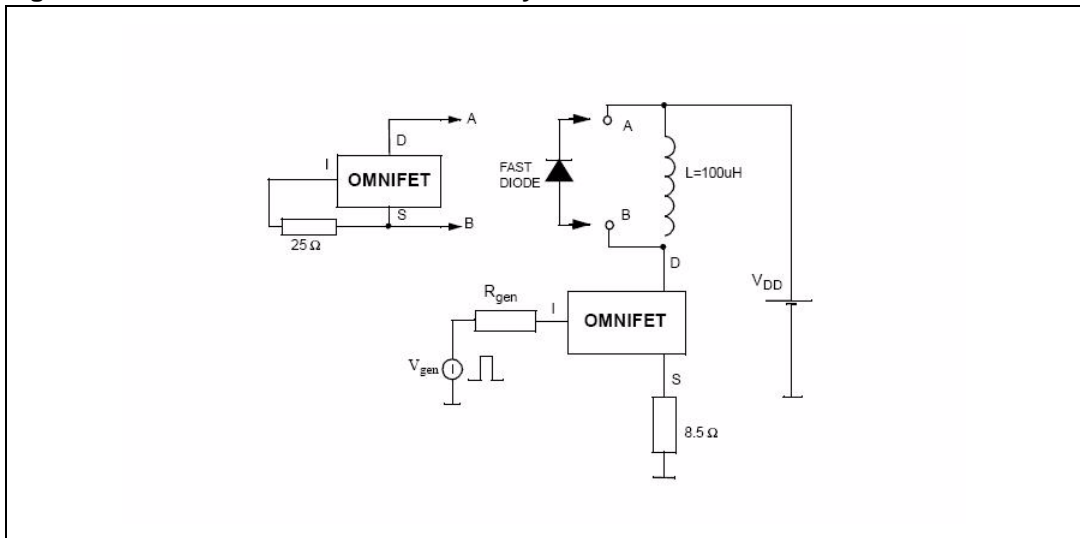


Figure 5. Unclamped inductive load test circuits

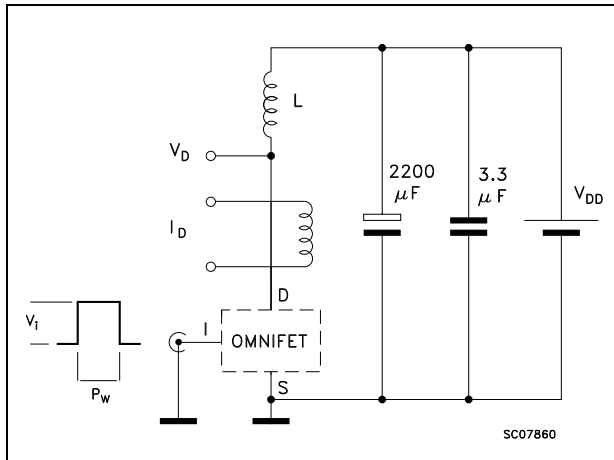


Figure 6. Unclamped inductive waveforms

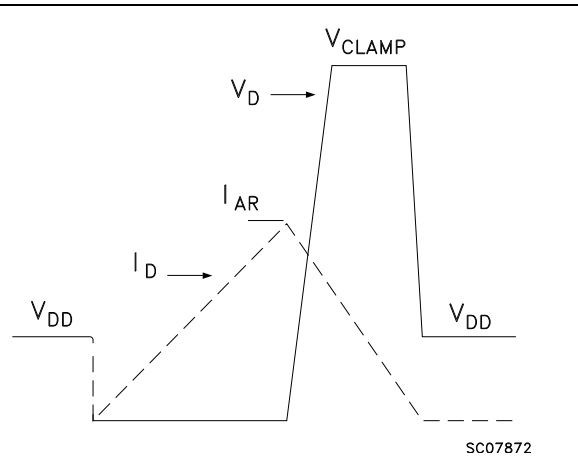


Figure 7. Input charge test circuit

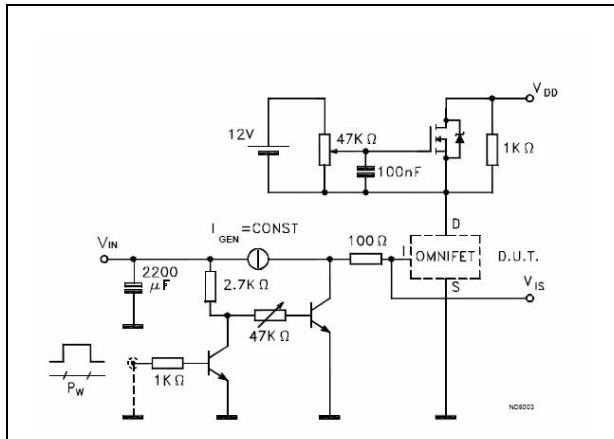


Figure 8. Source-drain diode forward characteristics

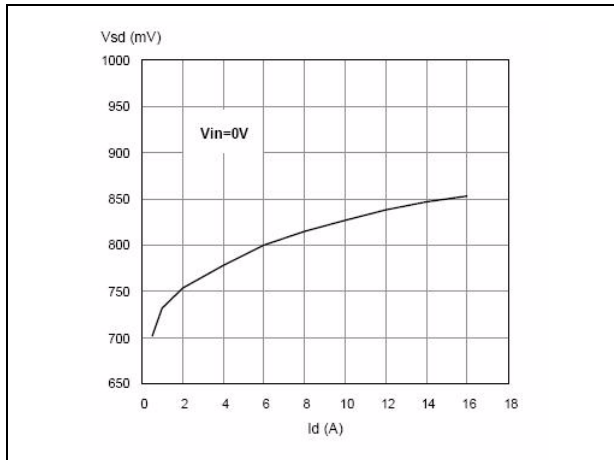


Figure 9. Static drain source on resistance

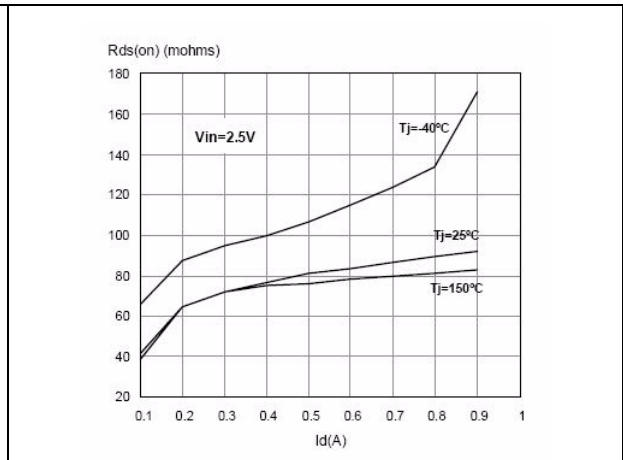


Figure 10. Derating curve

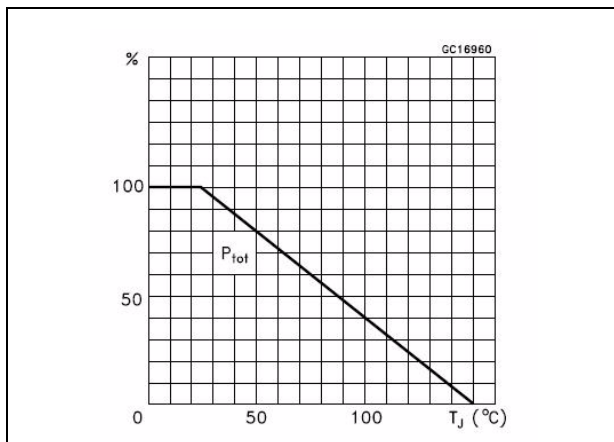


Figure 11. Static drain-source on resistance vs. input voltage (part 1/2)

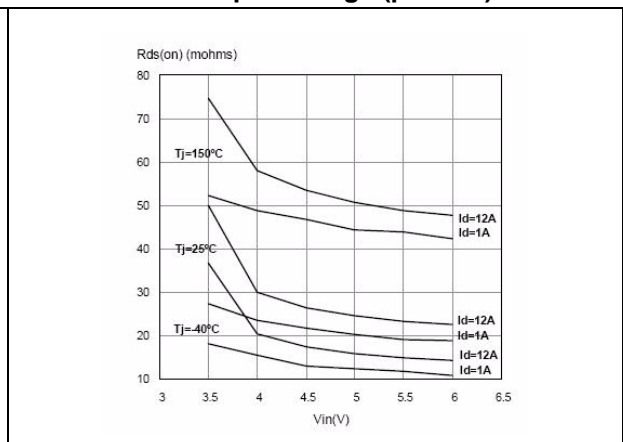


Figure 12. Static drain-source on resistance vs. input voltage (part 2/2)

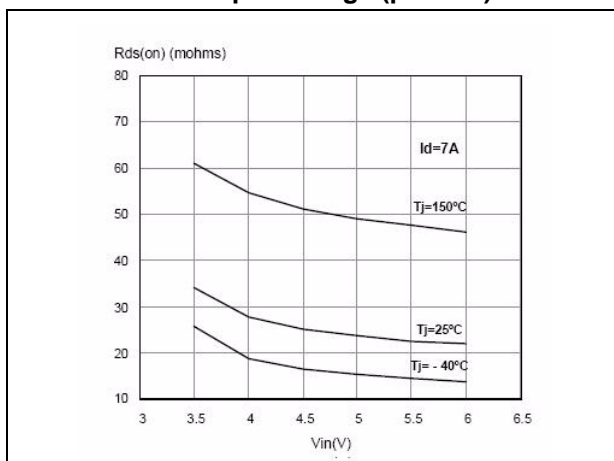


Figure 13. Transconductance

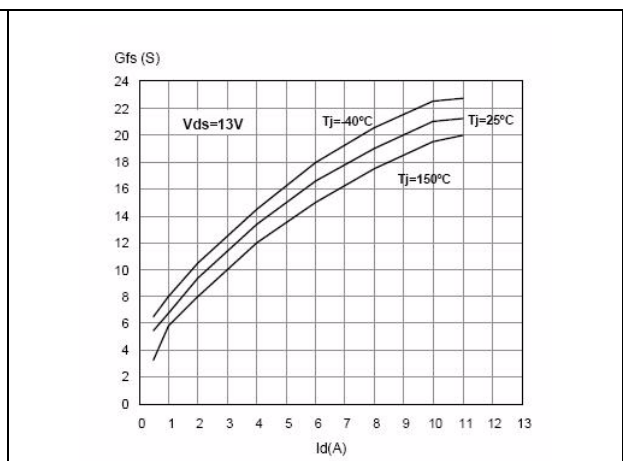


Figure 14. Static drain-source on resistance vs. id

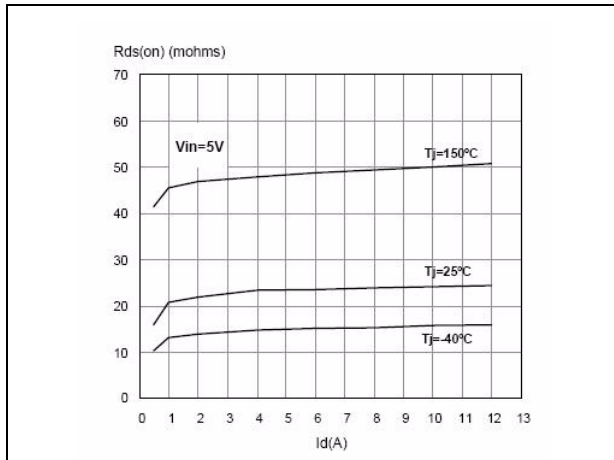


Figure 15. Transfer characteristics

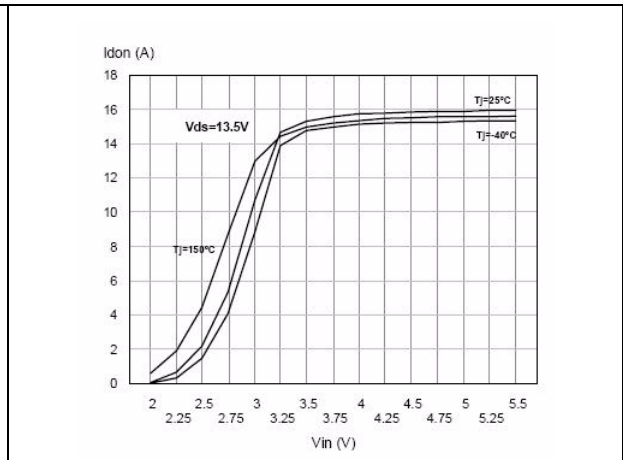


Figure 16. Turn-on current slope (part 1/2)

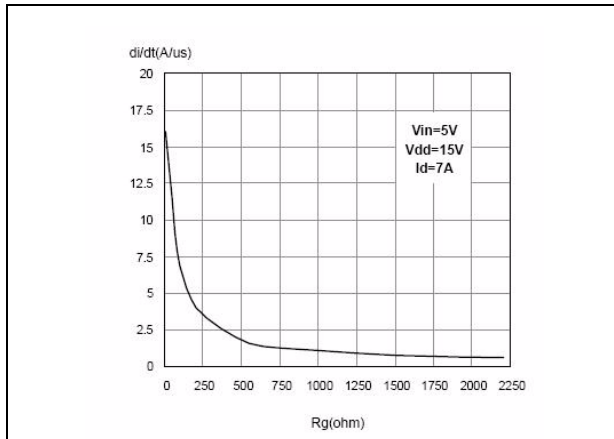


Figure 17. Turn-on current slope (part 2/2)

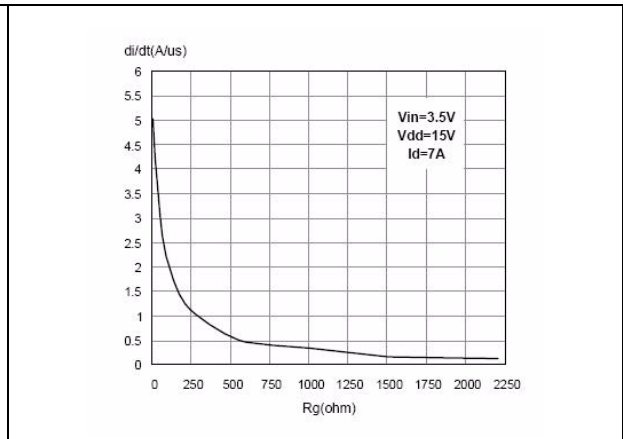


Figure 18. Input voltage vs. input charge

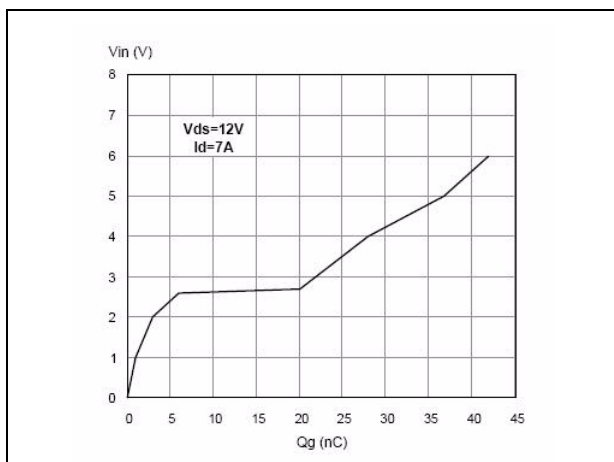


Figure 19. Turn-off drain source voltage slope (part 1/2)

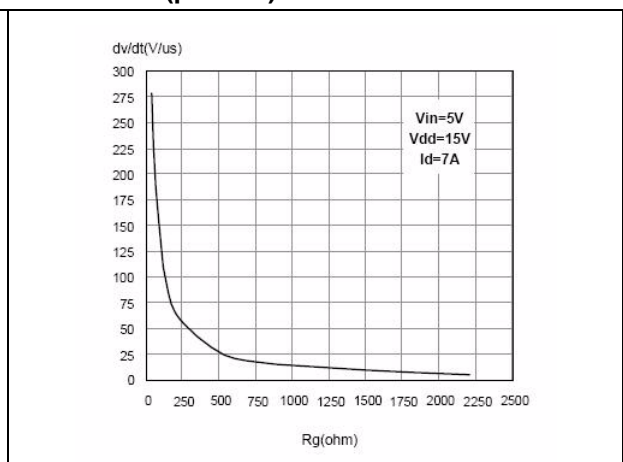


Figure 20. Turn-off drain source voltage slope Figure 21. Capacitance variations
(part 2/2)

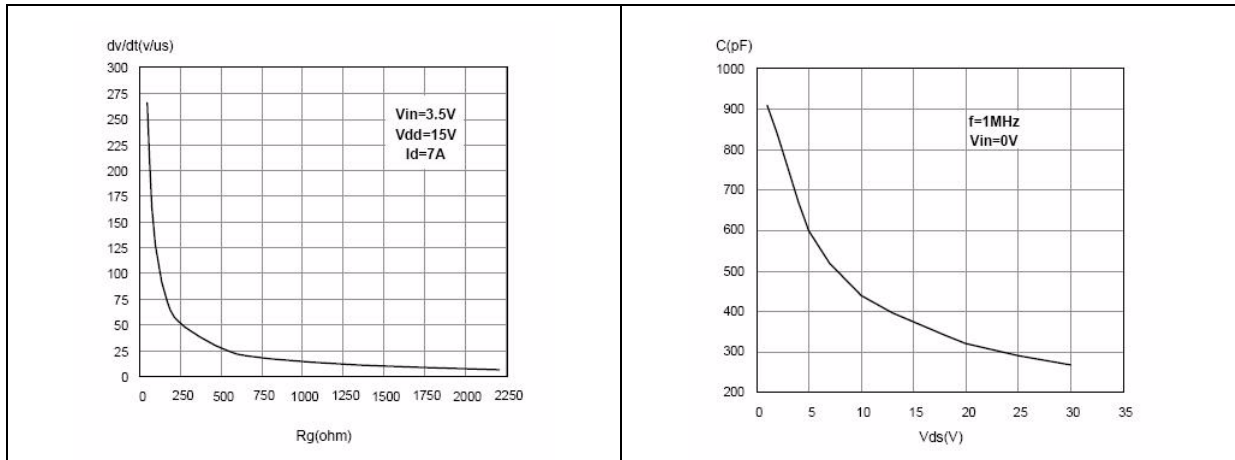


Figure 22. Switching time resistive load (part 1/2) Figure 23. Switching time resistive load (part 2/2)

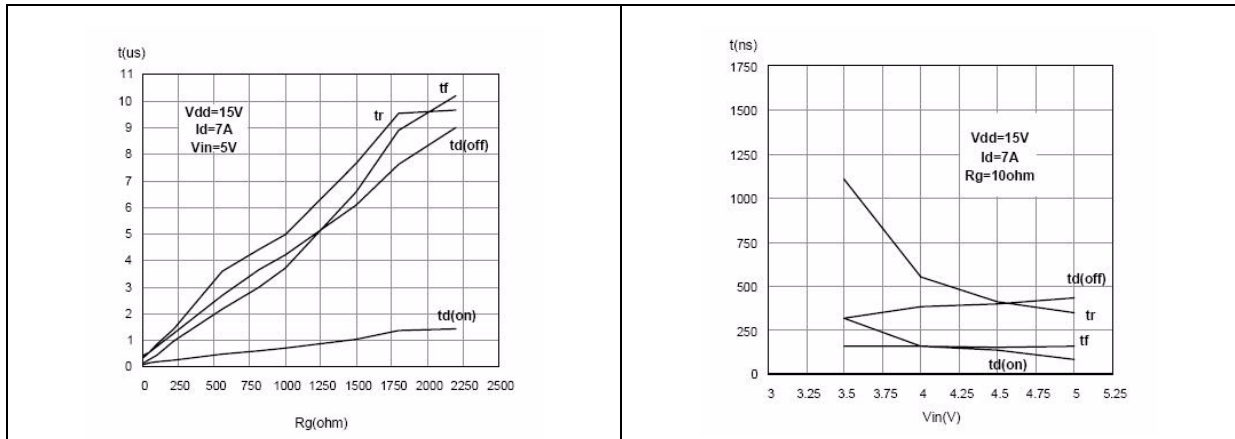


Figure 24. Output characteristics Figure 25. Normalized on resistance vs. temperature

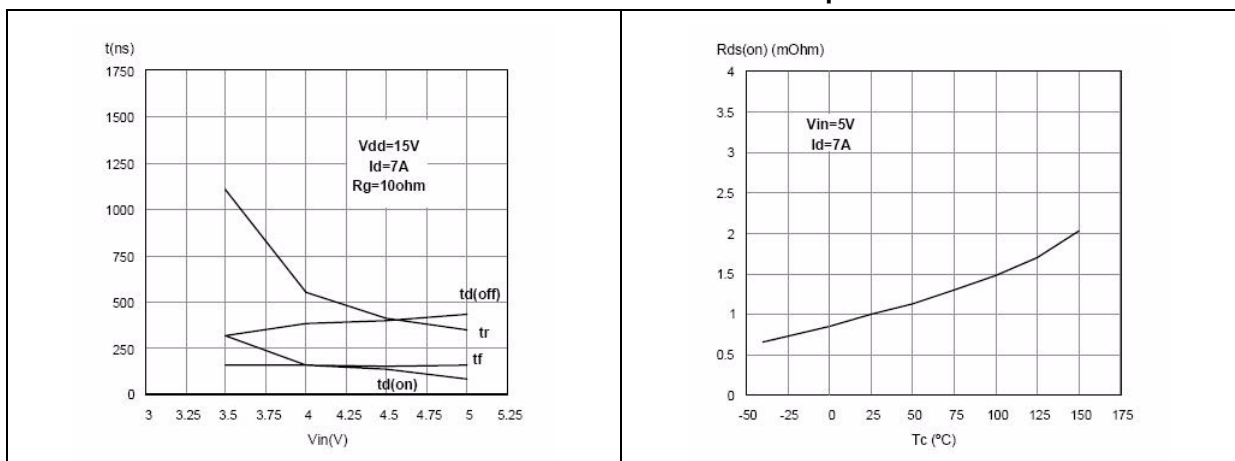


Figure 26. Normalized input threshold voltage vs. temperature **Figure 27. Current limit vs. junction temperatures**

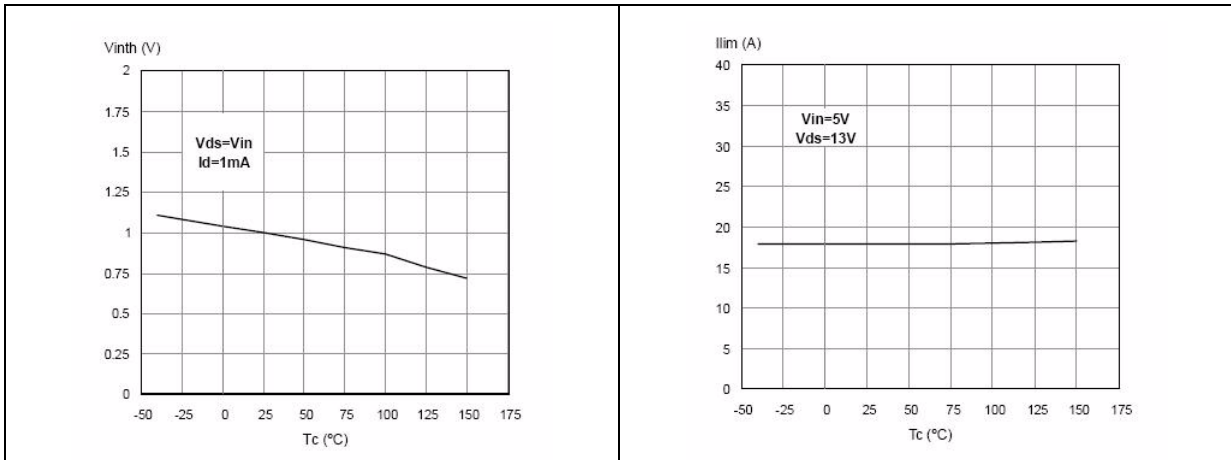


Figure 28. Step response current limit

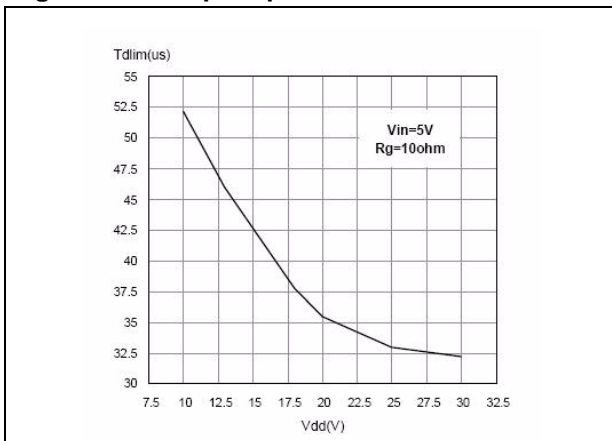
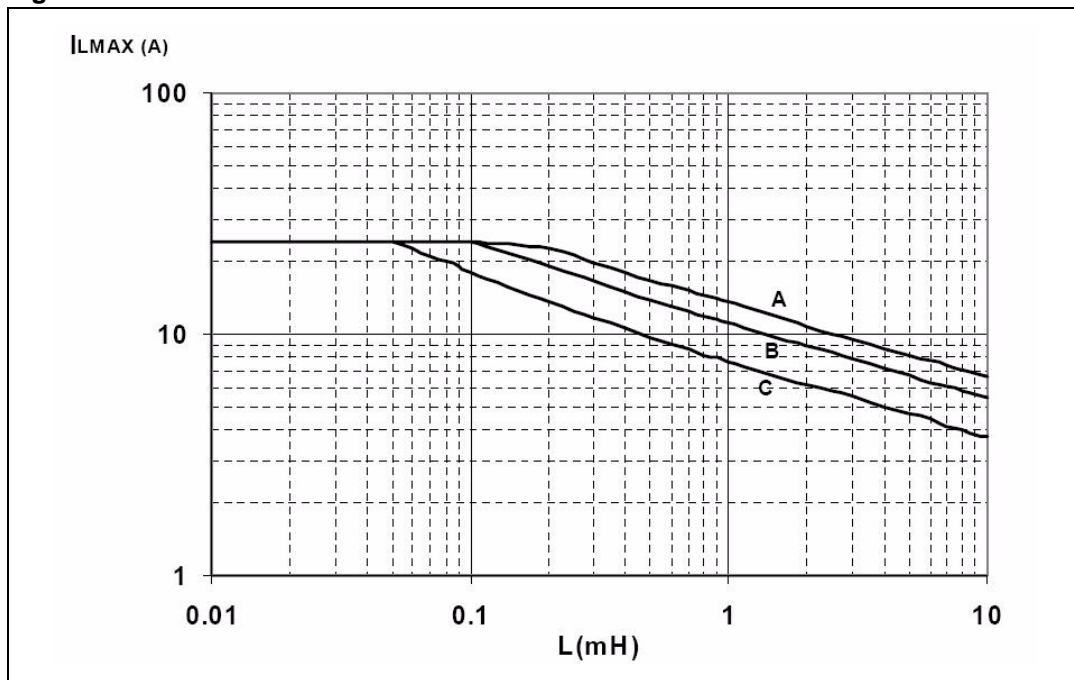


Figure 29. DPAK maximum turn-off current versus load inductance



Legend:

- A= Single pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive pulse at $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5\text{ V}$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Figure 30. DPAK demagnetization

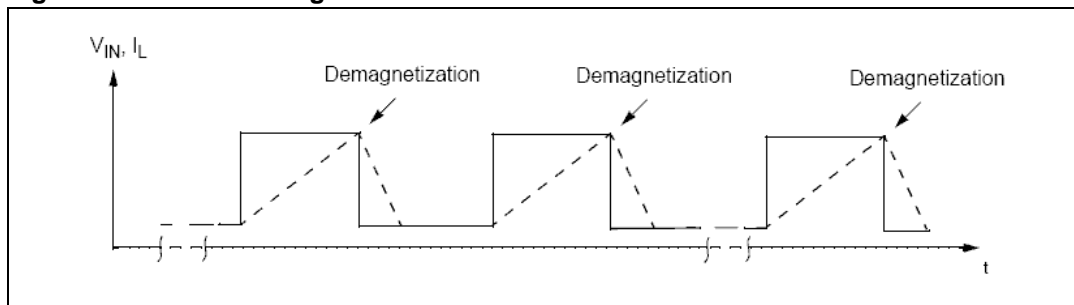
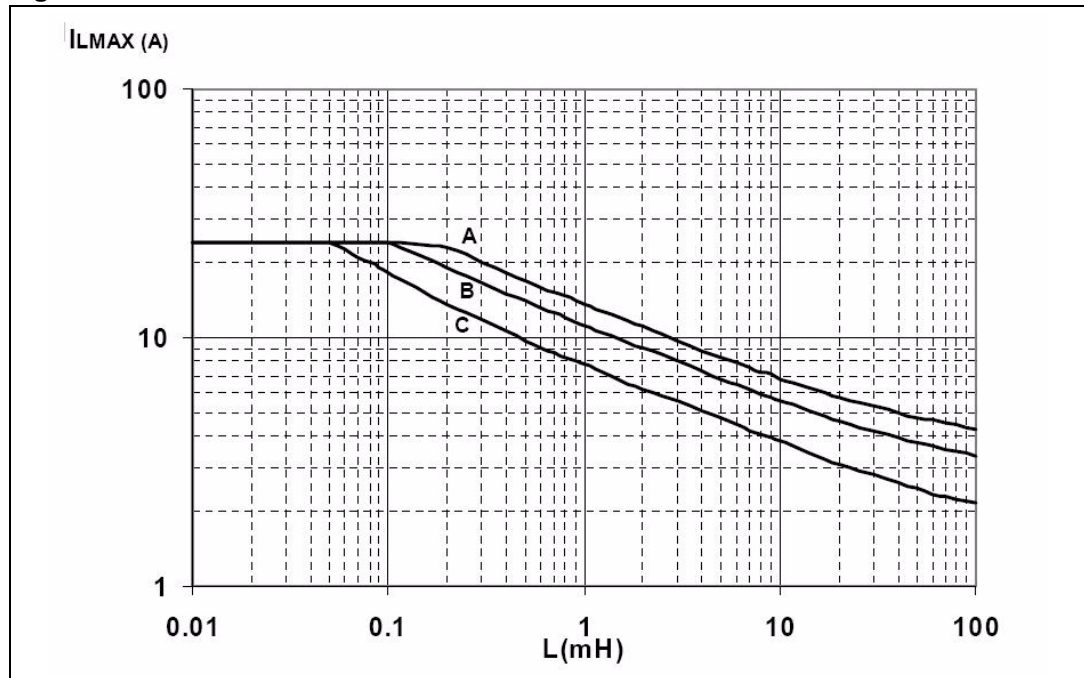


Figure 31. D²PAK maximum turn-off current versus load inductance



Legend:

A= Single pulse at $T_{Jstart}=150^{\circ}C$

B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$

C= Repetitive pulse at $T_{Jstart}=125^{\circ}C$

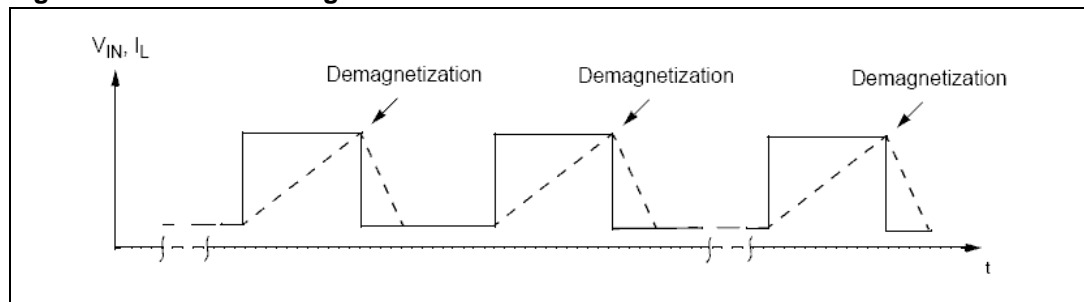
Conditions:

$V_{CC}=13.5\text{ V}$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

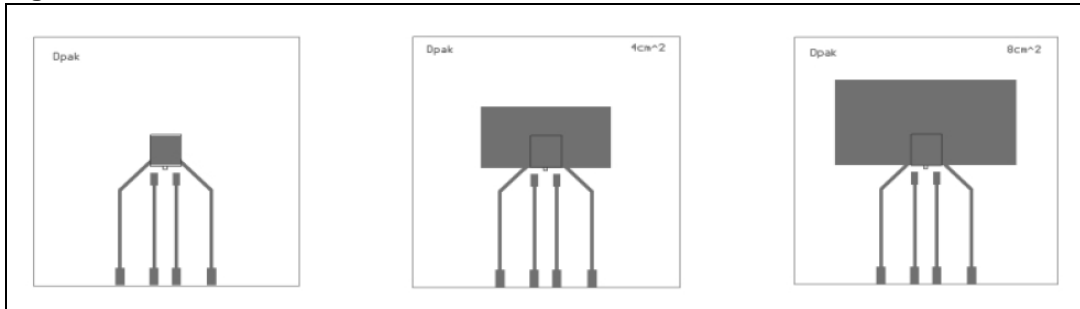
Figure 32. D²PAK demagnetization



4 Package thermal data

4.1 DPAK thermal data

Figure 33. DPAK PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness=2 mm, Cu thickness=35 μ m, Copper areas: from minimum pad lay-out to 8 cm²).

Figure 34. DPAK $R_{thj-amb}$ vs PCB copper area in open box free air condition

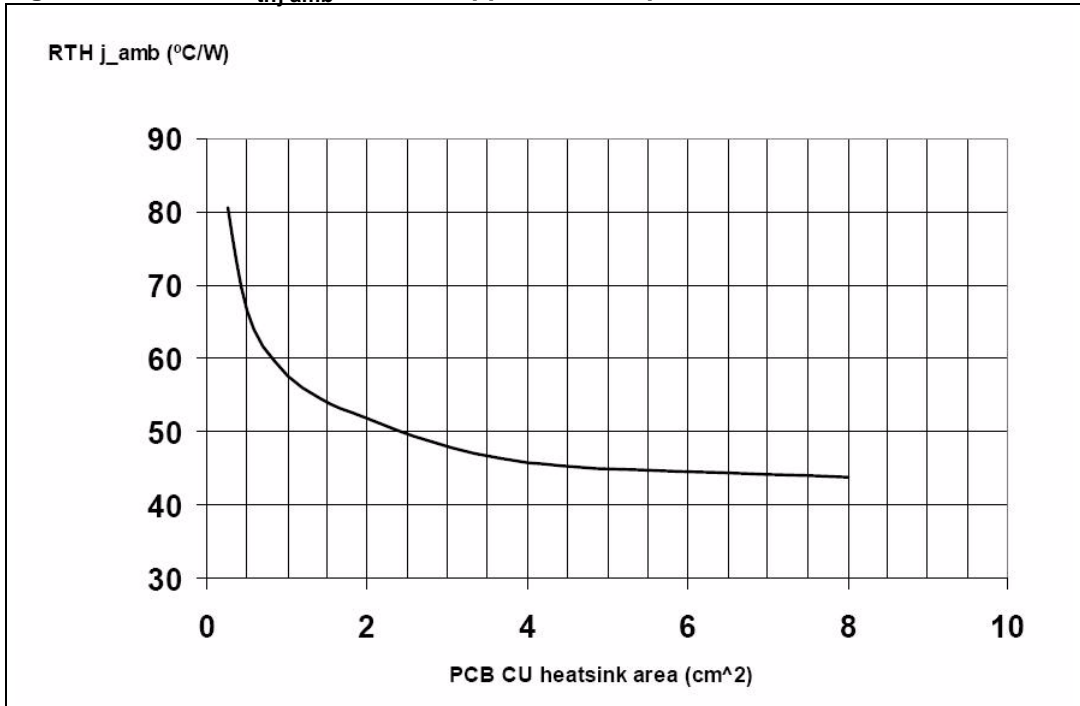


Figure 35. DPAK thermal impedance junction ambient single pulse

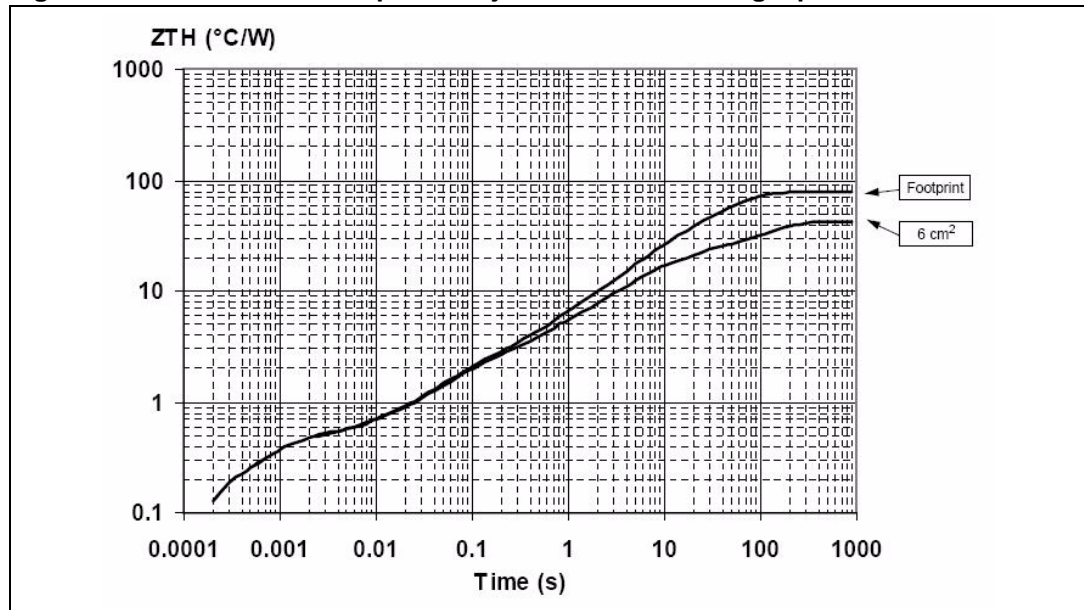
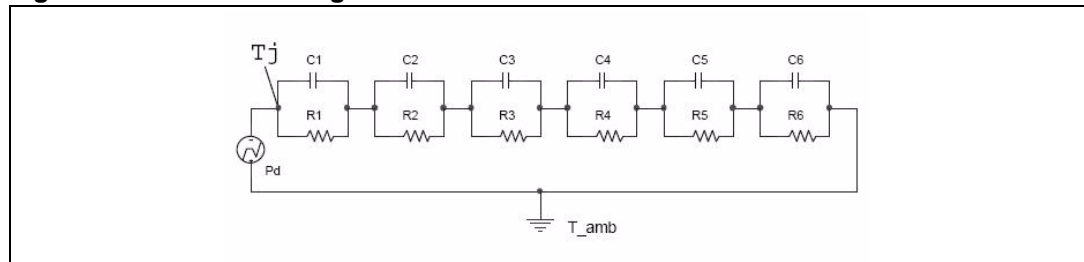


Figure 36. Thermal fitting model of an OMNIFET II in DPAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 5. DPAK thermal parameter

Area/island(cm ²)	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	1.20	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0021	
C3 (W.s/°C)	0.05	

Table 5. DPAK thermal parameter (continued)

Area/island(cm ²)	Footprint	6
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

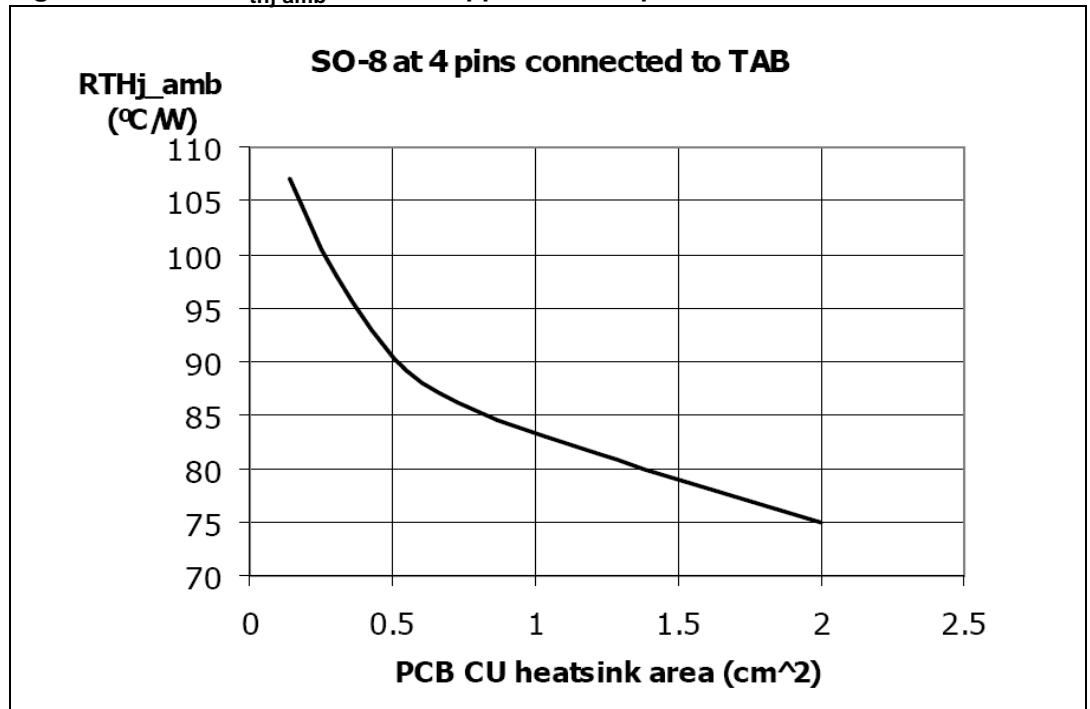
4.2 SO-8 thermal data

Figure 37. SO-8 PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35 μm, Copper areas: 0.14 cm², 0.6 cm², 1.6 cm²).

Figure 38. SO-8 R_{thj-amb} vs PCB copper area in open box free air condition



4.3 D²PAK thermal data

Figure 39. D²PAK PC board⁽¹⁾



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness=2 mm, Cu thickness=35 μ m, Copper areas: from minimum pad lay-out to 8 cm²).

Figure 40. D²PAK $R_{thj-amb}$ vs PCB copper area in open box free air condition

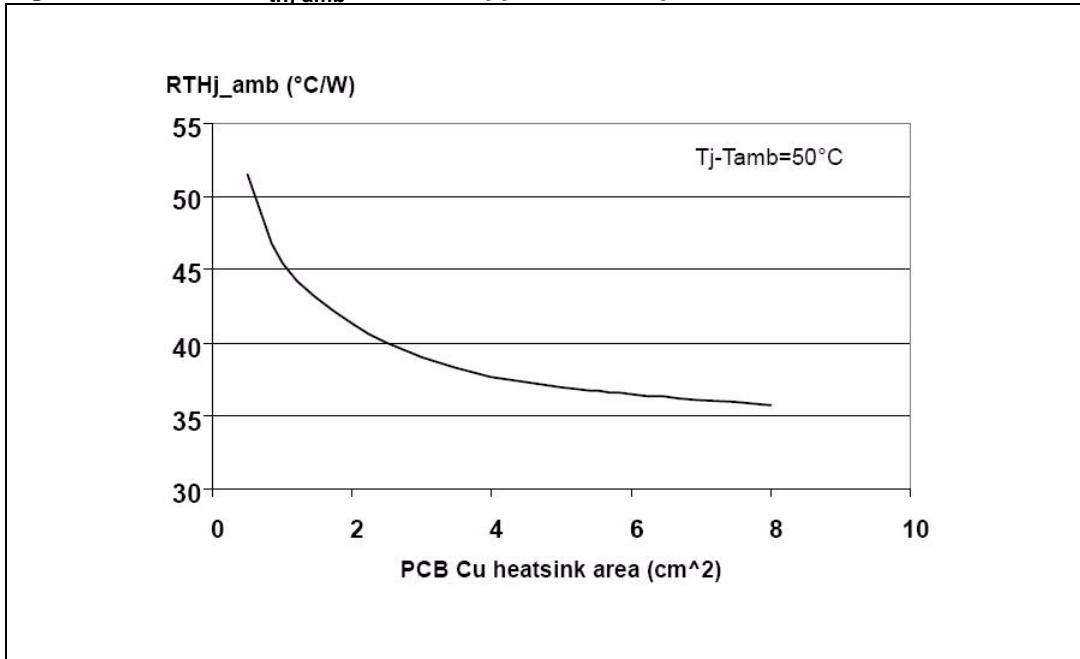


Figure 41. D²PAK thermal impedance junction ambient single pulse

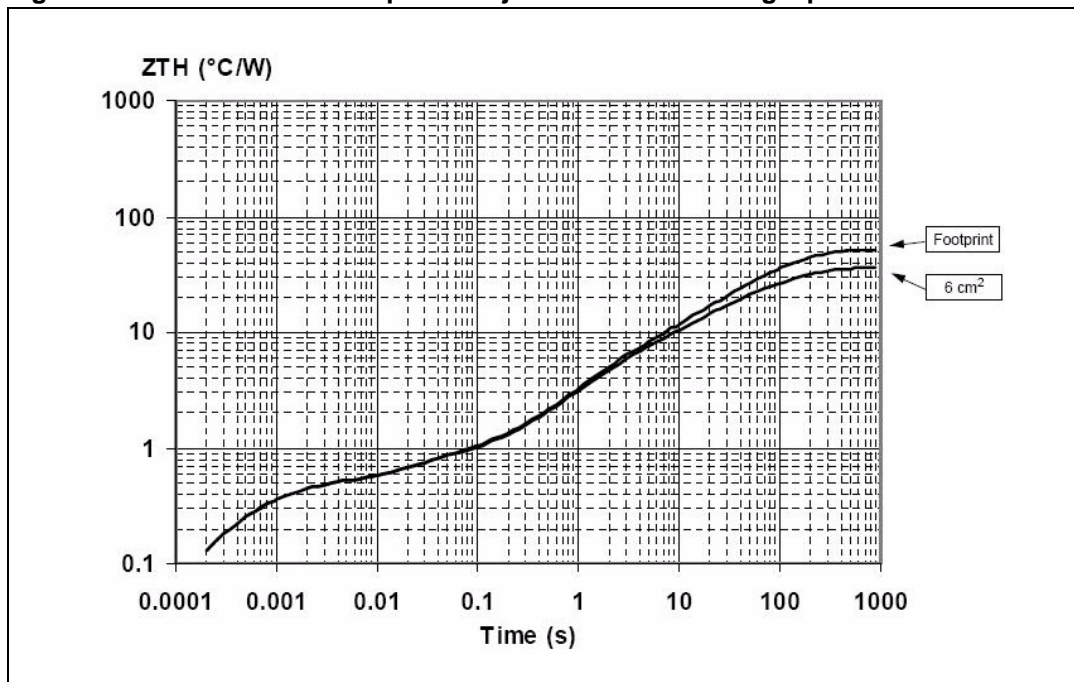
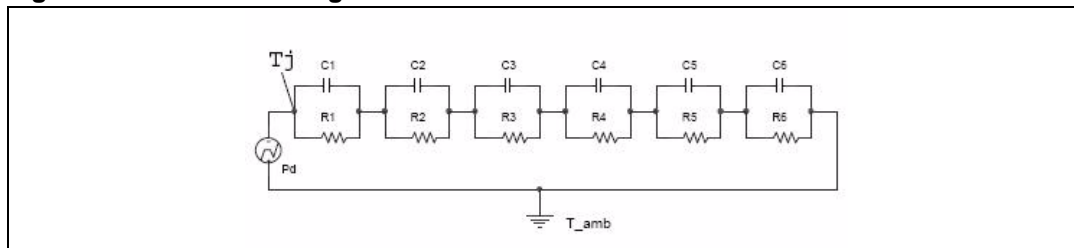


Figure 42. Thermal fitting model of an OMNIFET II in D²PAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 6. D²PAK thermal parameter

Area/island(cm ²)	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.10E-03	

Table 6. D²PAK thermal parameter (continued)

Area/island(cm ²)	Footprint	6
C3 (W.s/°C)	8.00E-02	
C4 (W.s/°C)	0.45	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 TO-251 (IPAK) mechanical data

Figure 43. TO-251 (IPAK) package dimension

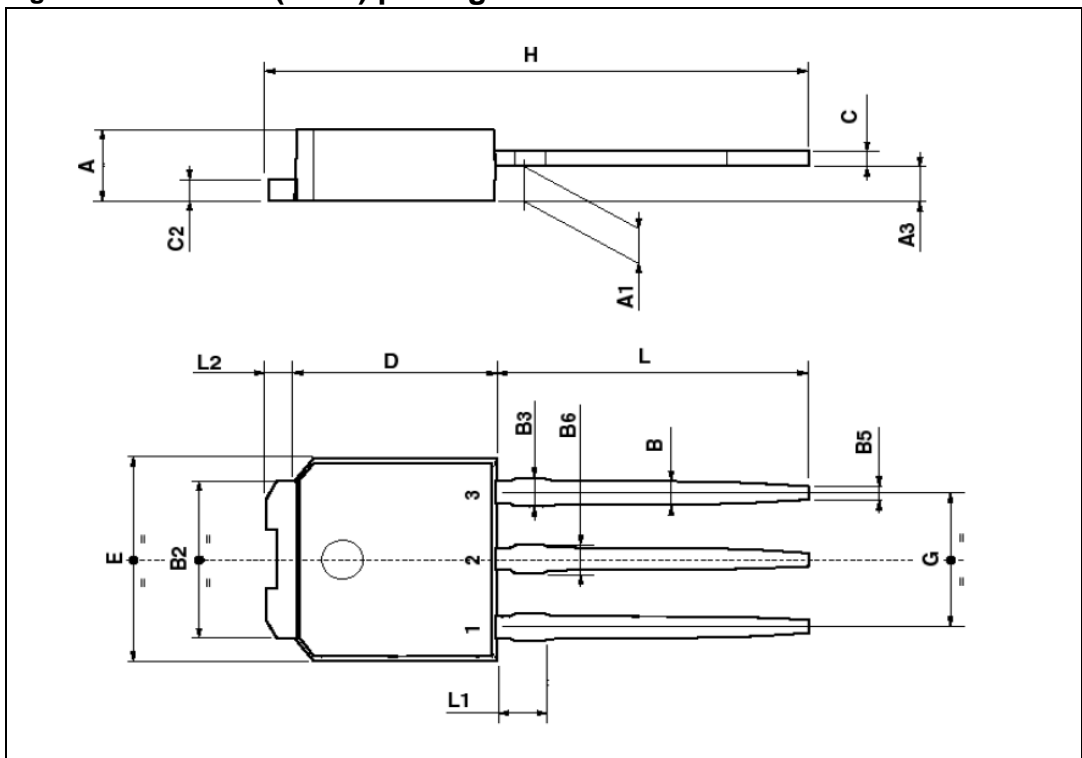


Table 7. TO-251 (IPAK) mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4

Table 7. TO-251 (IPAK) mechanical data (continued)

Dim.	Millimeters		
	Min.	Typ.	Max.
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

5.3 D²PAK mechanical data

Figure 44. D²PAK package dimension

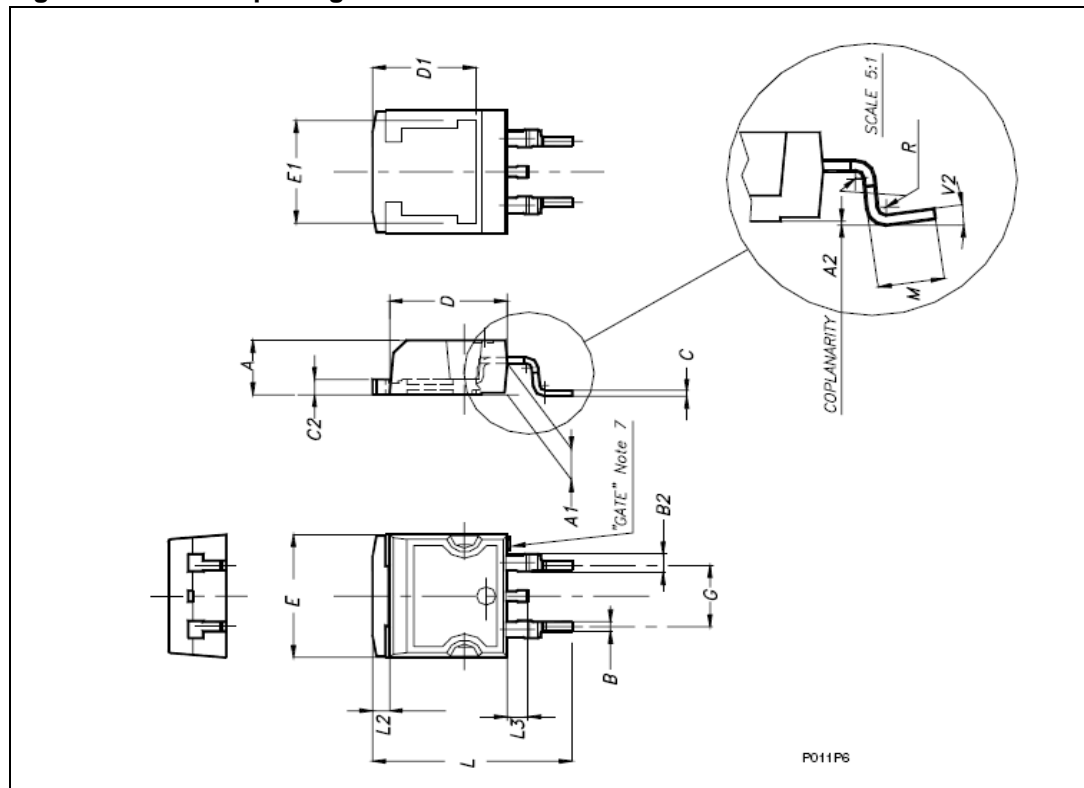


Table 8. D²PAK mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	4.4		4.6
A1	2.49		2.69
A2	0.03		0.23
B	0.7		0.93
B2	1.14		1.7
C	0.45		0.6
C2	1.23		1.36
D	8.95		9.35
D1		8	
E	10		10.4
E1		8.5	
G	4.88		5.28
L	15		15.85
L2	1.27		1.4
L3	1.4		1.75
M	2.4		3.2
R		0.4	
V2	0°		8°

5.4 TO-252 (DPAK) mechanical data

Figure 45. TO-252 (DPAK) package dimension

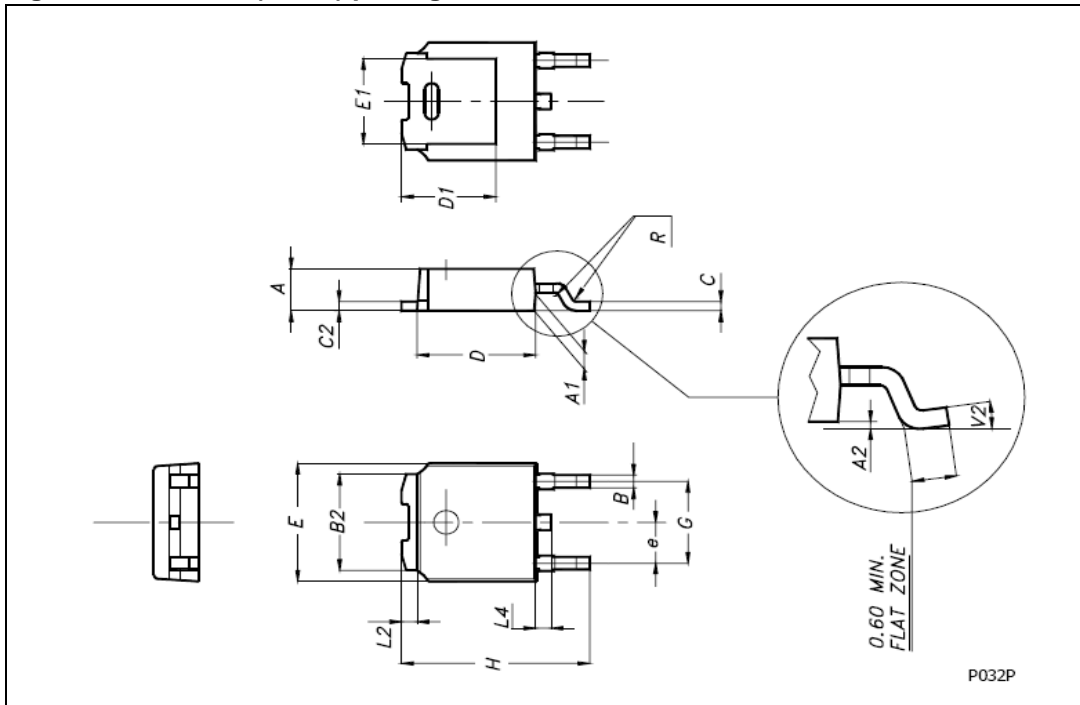


Table 9. TO-252 (DPAK) mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.6
C2	0.48		0.6
D	6		6.20
D1		5.1	
E	6.4		6.6
E1		4.7	
e		2.28	
G	4.4		4.6
H	9.35		10.1
L2		0.8	

Table 9. TO-252 (DPAK) mechanical data (continued)

Dim.	Millimeters		
	Min.	Typ.	Max.
L4	0.6		1
R		0.2	
V2	0°	8°	
Package weight	Gr. 0.29		

5.5 SO-8 mechanical data

Figure 46. SO-8 package dimension

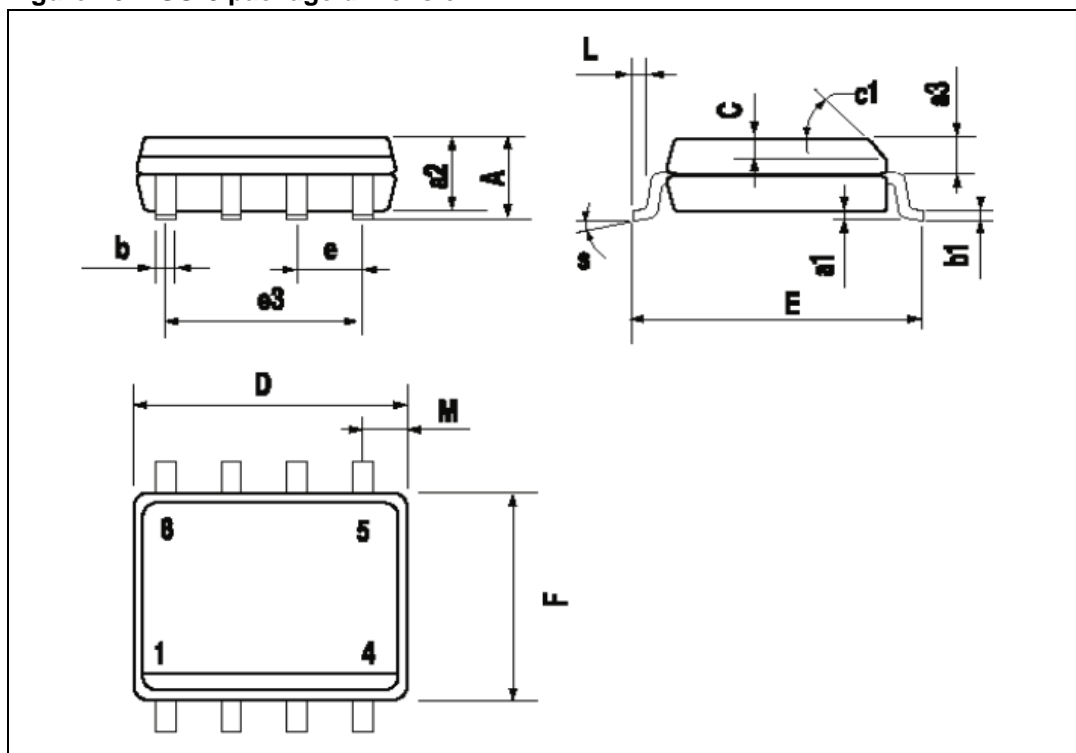


Table 10. SO-8 mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	1.75		2.40
a1	0.25		0.1
a2	1.65		
b	0.85		0.35
b1	0.25		0.19

Table 10. SO-8 mechanical data (continued)

Dim.	Millimeters		
	Min.	Typ.	Max.
C	0.5		0.25
c1		45	
D	5		4.8
E	6.2		5.8
e		1.27	
e3		3.81	
F	4		3.8
L	1.27		0.4
M	0.6		
F			8

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
21-Jun-2004	6	Initial release.
03-Apr-2009	7	Document reformatted. Added Table 1: Device summary on page 1 . Updated Section 5: Package information on page 24
06-Apr-2010	8	Added part number VNS14NV04. Added SO-8 package: – Updated Table 1: Device summary – Updated Table 2: Absolute maximum rating – Updated Table 3: Thermal data – Updated Chapter 4: Package thermal data – Updated Chapter 5: Package information
20-Sep-2013	9	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com