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- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 3-State Version of 'HC153
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Inverting Outputs Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 9 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Permit Multiplexing From n Lines to One Line
- Perform Parallel-to-Serial Conversion

D PACKAGE (TOP VIEW) 16 V_{CC} 10E [15 20E B 🛮 2 1C3 🛮 3 14 🛮 A 1C2 ∏ 4 13 2C3 12 **1** 2C2 1C1 ∏ 5 1C0 ∏ 6 11 2C1 1Y 🛮 7 10 2C0 9 2Y GND [8]

description/ordering information

Each data selector/multiplexer contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable (\overline{OE}) input. The outputs are disabled when their respective \overline{OE} is high.

ORDERING INFORMATION[†]

T _A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC - D	Tape and reel	SN74HC253QDRQ1	HC253Q1

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

SN74HC253-Q1 **DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER** WITH 3-STATE OUTPUTS SCLS519A - AUGUST 2003 - REVISED APRIL 2008

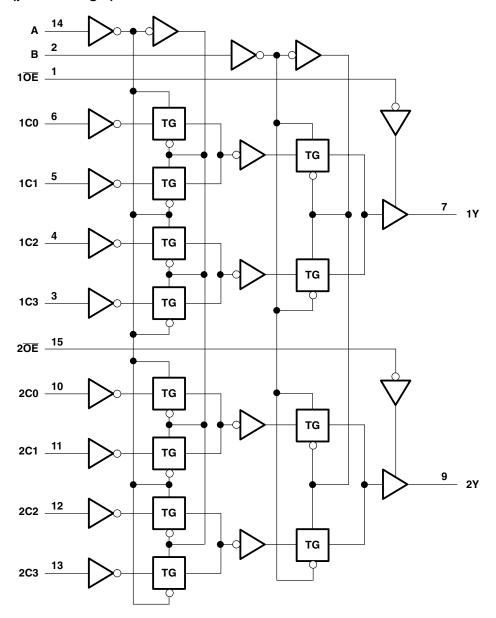
FUNCTION TABLE

	INPUTS										
SELI	ECT†		DA	TA		ΔF.	OUTPUT V				
В	Α	C0	C1	C2	СЗ	OE	•				
Х	Х	Х	Χ	Х	Х	Н	Z				
L	L	L	Χ	X	X	L	L				
L	L	Н	Χ	X	Χ	L	Н				
L	Н	Х	L	X	X	L	L				
L	Н	Х	Н	X	X	L	Н				
Н	L	Х	Χ	L	X	L	L				
Н	L	Χ	Χ	Н	Χ	L	Н				
Н	Н	Х	Χ	Χ	L	L	L				
Н	Н	Χ	Χ	Χ	Н	L	Н				

[†] Select inputs A and B are common to both sections.



logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	\dots –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	$\dots \dots \pm 20 \ mA$
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	$\dots \dots \pm 20 \ mA$
Continuous output current, I_O ($V_O = 0$ to V_{CC})	$\dots \dots \pm 25 \text{ mA}$
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2)	73°C/W
Storage temperature range, T _{sto}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
		V _{CC} = 2 V	1.5			
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15			V
		V _{CC} = 6 V	4.2			
		V _{CC} = 2 V			0.5	
V_{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V}$			1.35	V
		V _{CC} = 6 V			1.8	
VI	Input voltage		0		V_{CC}	V
Vo	Output voltage		0		V_{CC}	V
		V _{CC} = 2 V			1000	
Δt/Δν	Input transition rise/fall time	$V_{CC} = 4.5 \text{ V}$			500	ns
		V _{CC} = 6 V			400	
T _A	Operating free-air temperature		-40		125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		.,	T	_A = 25°C	;			
PARAMETER	TEST CONDITIO	v _{cc}	MIN	TYP	MAX	MIN MA	MAX	UNIT	
			2 V	1.9	1.998		1.9		
		$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		
V _{OH}	$V_{I} = V_{IH}$ or V_{IL}		6 V	5.9	5.999		5.9		V
		$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		
		$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		
	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1	
			4.5 V		0.001	0.1		0.1	
V_{OL}			6 V		0.001	0.1		0.1	V
		$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4	
		$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4	
I _I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000	nA
I _{OZ}	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10	μΑ
I _{CC}	$V_I = V_{CC}$ or 0,	I _O = 0	6 V			8		160	μΑ
C _i			2 V to 6 V		3	10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

24244555	FROM	то	1,,	T _A = 25	°C		
PARAMETER	(INPUT)	(OUTPUT)	v _{cc}	MIN TYP	MAX	MIN MAX	UNIT
			2 V	62	150	225	
	A or B	Any Y	4.5 V	19	30	45	
			6 V	16	26	38	
t _{pd}			2 V	54	126	210	ns
	Data (Any C)	Υ	4.5 V	16	3 28	42	
			6 V	10	3 23	36	
	ŌĒ		2 V	28	3 100	150	
t _{en}		Υ	4.5 V	11	20	30	
			6 V	Ç	17	26	
			2 V	2	135	203	
t _{dis}	ŌĒ	Υ	4.5 V	14	30	45	ns
			6 V	12	2 35	38	
			2 V	28	8 60	90	
t _t		Υ	4.5 V	8	3 12	18	ns
			6 V	6	10	15	

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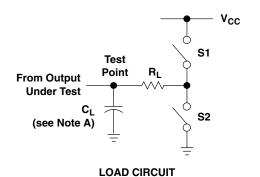
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	\ \ \	T,	գ = 25°C	;	BAIN! BAA	/ LINUT
PARAMETER	(INPUT)	(OUTPUT)	v _{cc}	MIN	TYP	MAX	MIN MA	K UNIT
			2 V		76	235	35	5
	A or B	Any Y	4.5 V		23	47	7	1
			6 V		20	41	6	
t _{pd}	Data (Any C)	Y	2 V		68	220	33	ns 5
			4.5 V		20	44	6	7
	(Ally O)		6 V		17	38	5	7
	ŌĒ	Y	2 V		44	185	28	0
t _{en}			4.5 V		16	37	5	6 ns
			6 V		14	32	4	В
t _t			2 V		45	210	31	5
		Υ	4.5 V		17	42	6	3 ns
			6 V		13	36	5	3

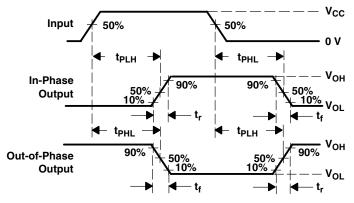
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per multiplexer	No load	45	pF

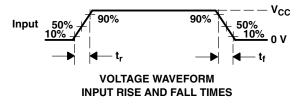
PARAMETER MEASUREMENT INFORMATION

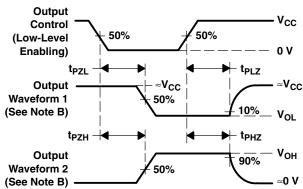


PARAI	PARAMETER		C _L	S1	S2
	t _{PZH}	1 k Ω	50 pF or	Open	Closed
t _{en}	t _{PZL}	1 K22	150 pF	Closed	Open
	t _{PHZ}	1 k Ω	50 pF	Open	Closed
t _{dis}	t _{PLZ}	1 K22	50 pr	Closed	Open
t _{pd} or	t _t		50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



17-Aug-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC253QDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC253QDRQ1	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74HC253-Q1:

Catalog: SN74HC253

Enhanced Product: SN74HC253-EP



17-Aug-2012

• Military: SN54HC253

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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