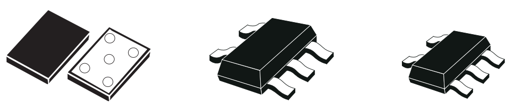
LD3985

Ultra low drop and low noise BiCMOS voltage regulators

Datasheet - production data



Flip-chip (1.57 x 1.22) | SOT23-5L | TSOT23-5L

Features

- Input voltage from 2.5 V to 6 V
- Stable with low ESR ceramic capacitors
- Ultra low-dropout voltage (60 mV typ. at 150 mA load, 0.4 mV typ. at 1 mA load)
- Very low quiescent current (85 µA typ. at no load, 170 µA typ. at 150 mA load; max.1.5 µA in OFF mode)
- Guaranteed output current up to 150 mA
- Wide range of output voltage: 1.22 V; 1.8 V; 2.5 V; 2.6 V; 2.7 V; 2.8 V; 2.9 V; 3 V; 3.3 V; 4.7 V
- Fast turn-on time: typ. 200 µs [C_O = 1 µF, C_{BYP} = 10 nF and I_O = 1 mA]
- Logic-controlled electronic shutdown
- Internal current and thermal limit
- Output low noise voltage 30 μV_{RMS} over 10 Hz to 100 kHz
- SVR of 60 dB at 1 kHz, 50 dB at 10 kHz
- Temperature range: - 40 °C to 125 °C

Description

The LD3985 provides up to 150 mA, from 2.5 V to 6 V input voltage. The ultra low drop voltage, low quiescent current and low noise make it suitable for low power applications and in battery-powered systems. Regulator ground current increases slightly in dropout only, prolonging the battery life. Power supply rejection is better than 60 dB at low frequencies and rolls off at 10 kHz. High power supply rejection is maintained down to low input voltage levels common to battery operated circuits. Shutdown logic control function is available, this means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD3985 is designed to work with low ESR ceramic capacitors. Typical applications are in mobile phones and similar battery-powered wireless systems.

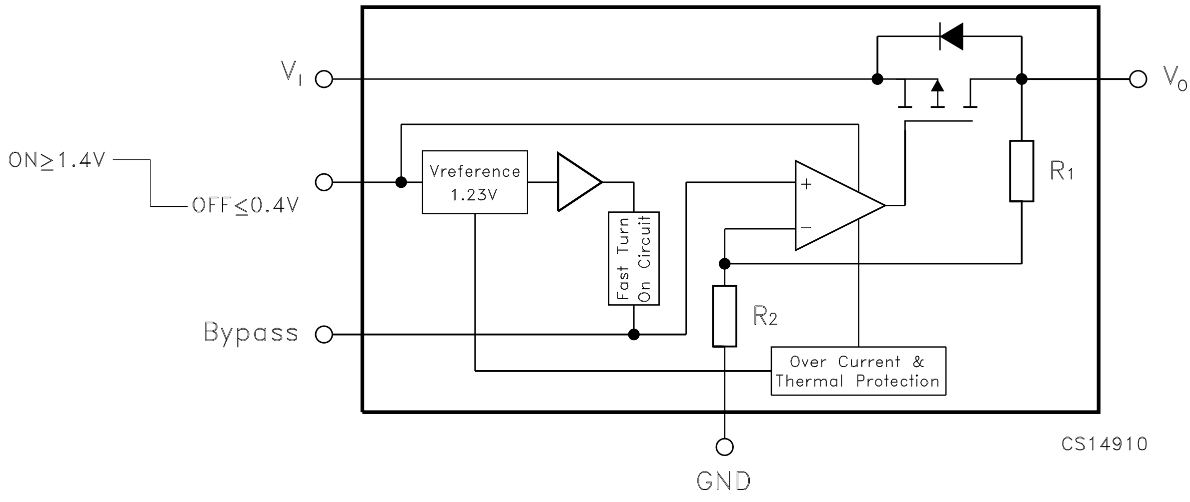
Table 1. Device summary

Part numbers	
LD3985XX122	LD3985XX28
LD3985XX18	LD3985XX29
LD3985XX25	LD3985XX30
LD3985XX26	LD3985XX33
LD3985XX27	LD3985XX47

Contents

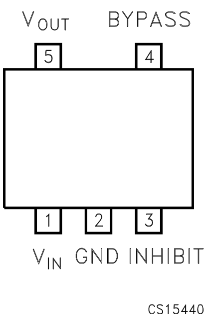
1 Diagram

Figure 1. Schematic diagram

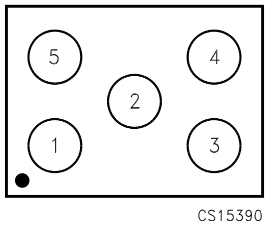


2 Pin configuration

Figure 2. Pin connections (SOT and TSOT top view, Flip-chip top view)



SOT23-5L/TSOT23-5L



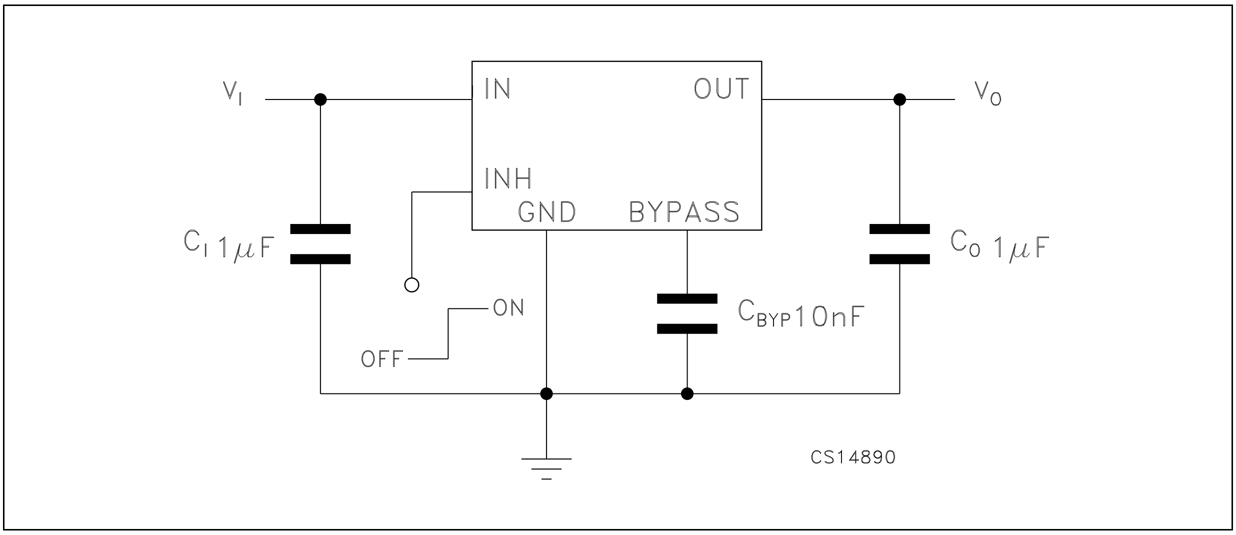
Flip-chip

Table 2. Pin description

Pin n° for SOT23-5L/ TSOT23-5L	Pin n° for Flip-chip	Symbol	Name and function
1	4	V_I	Input voltage of the LDO
2	2	GND	Common ground
3	1	V_{INH}	Inhibit input voltage: ON mode when $V_{INH} \geq 1.2$ V, OFF mode when $V_{INH} \leq 0.4$ V (Do not leave it floating, not internally pulled down/up)
4	5	BYPASS	Bypass pin: an external capacitor (usually 10 nF) has to be connected to minimize noise voltage
5	3	V_O	Output voltage of the LDO

3 Typical application

Figure 3. Typical application circuit



4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.3 to 6 (1)	V
V_O	DC output voltage	-0.3 to V_I+0.3	V
V_{INH}	Inhibit input voltage	-0.3 to V_I+0.3	V
I_O	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-65 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

1. The input pin is able to withstand non repetitive spike of 6.5 V for 200 ms.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	SOT23-5L/ TSOT23	Flip-chip	Unit
R_{thJC}	Thermal resistance junction-case	81		°C/W
R_{thJA}	Thermal resistance junction-ambient	255	170	°C/W

5 Electrical characteristics

T_J = 25 °C, V_I = $V_{O(NOM)}$ +0.5 V, C_I = 1 µF, C_{BYP} = 10 nF, I_O = 1 mA, V_{INH} = 1.4 V, unless otherwise specified.

Table 5. LD3985 electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage		2.5		6	V
V_O	Output voltage accuracy, $V_{O(NOM)}$ < 2.5 V	I_O = 1 mA	-50		50	mV
		T_J = -40 to 125 °C	-75		75	
V_O	Output voltage accuracy, $V_{O(NOM)} \geq$ 2.5V	I_O = 1 mA	-2		2	% of $V_{O(NOM)}$
		T_J= -40 to 125 °C	-3		3	
ΔV_O	Line regulation (1)	V_I = $V_{O(NOM)}$ + 0.5 to 6 V T_J = -40 to 125 °C	-0.1		0.1	%/V
		$V_{O(NOM)}$ = 4.7 to 5V	-0.19		0.19	
ΔV_O	Load regulation	I_O = 1 mA to 150mA, $V_{O(NOM)}$ < 2.5 V T_J= -40 to 125 °C		0.002	0.008	%/mA
ΔV_O	Load regulation	I_O = 1 mA to 150 mA, $V_{O(NOM)} \geq$ 2.5 V T_J = -40 to 125 °C (for flip-chip)		0.0004	0.002	%/mA
		I_O = 1 mA to 150mA, T_J = -40 to 125°C (for SOT23-5L/TSOT23-5L), $V_{O(NOM)} \geq$ 2.5 V		0.0025	0.005	
ΔV_O	Output AC line regulation (2)	V_I = $V_{O(NOM)}$ + 1 V, I_O = 150 mA, t_R= t_F = 30 µs		1.5		mV_{PP}
I_Q	Quiescent current ON mode: V_{INH} = 1.2 V	I_O = 0		85		µA
		I_O = 0, T_J= -40 to 125 °C			150	
		I_O = 0 to 150 mA		170		
		I_O = 0 to 150 mA, T_J= -40 to 125 °C			250	
	OFF mode: V_{INH} = 0.4 V			0.003		
		T_J= -40 to 125 °C			1.5	
V_{DROP}	Dropout voltage (3)	I_O = 1 mA		0.4		mV
		I_O = 1 mA, T_J= -40 to 125 °C			2	
		I_O = 50 mA		20		
		I_O = 50 mA, T_J= -40 to 125 °C			35	
		I_O = 100 mA		45		
		I_O = 100 mA, T_J= -40 to 125 °C			70	
		I_O = 150 mA		60		
		I_O = 150 mA, T_J= -40 to 125 °C			100	
I_{SC}	Short-circuit current	R_L = 0		600		mA

Table 5. LD3985 electrical characteristics (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	$V_I = V_{O(NOM)}$+0.25 V ± V_{RIPPLE} = 0.1 V, I_O= 50 mA $V_{O(NOM)}$ < 2.5 V, V_I = 2.55 V	f = 1kHz		60		dB
			f = 10kHz		50		
$I_{O(PK)}$	Peak output current	$V_O \geq V_{O(NOM)}$ - 5%		300	550		mA
V_{INH}	Inhibit input logic low	V_I = 2.5 V to 6 V, T_J= -40 to 125 °C				0.4	V
	Inhibit input logic high			1.2			
I_{INH}	Inhibit input current	V_{INH} = 0.4 V, V_I = 6 V			±1		nA
eN	Output noise voltage	B_W = 10 Hz to 100 kHz, C_O = 1 µF			30		μV_{RMS}
t_{ON}	Turn-on time (4)	C_{BYP} = 10 nF			100	250	µs
T_{SHDN}	Thermal shutdown	(5)			160		°C
C_O	Output capacitor	Capacitance (6)		1		22	µF
		ESR		5		5000	mΩ

1. For $V_{O(NOM)}$ < 2 V, V_I = 2.5 V
2. For $V_{O(NOM)}$ = 1.25 V, V_I = 2.5 V
3. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to input voltages below 2.5 V
4. Turn-on time is time measured between the enable input just exceeding V_{INH} high value and the output voltage just reaching 95% of its nominal value
5. Typical thermal protection hysteresis is 20 °C
6. The minimum capacitor value is 1 µF, anyway the LD3985 is still stable if the compensation capacitor has a 30% tolerance in all temperature range

6 Typical performance characteristics

T_J = 25 °C, $V_I = V_{O(NOM)}$ +0.5 V, $C_I = C_O$ = 1 µF, C_{BYP} = 10 nF, I_O = 1 mA, V_{INH} = 1.4 V, unless otherwise specified.

Figure 4. Output voltage vs. temperature (V_0=1.35 V)

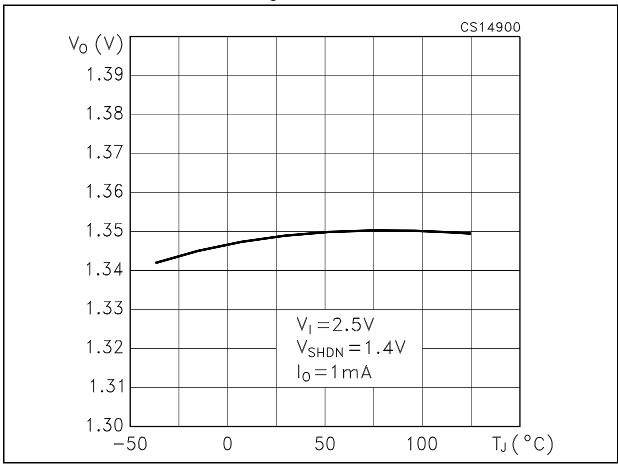


Figure 5. Output voltage vs. temperature (V_0=2.7 V)

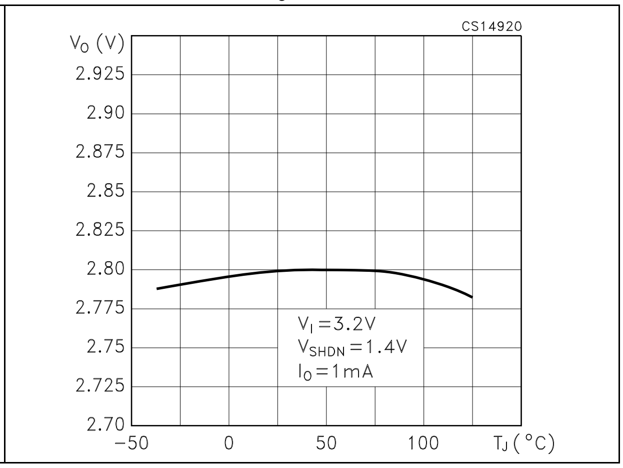


Figure 6. Output voltage vs. temperature (V_0=3.3 V)

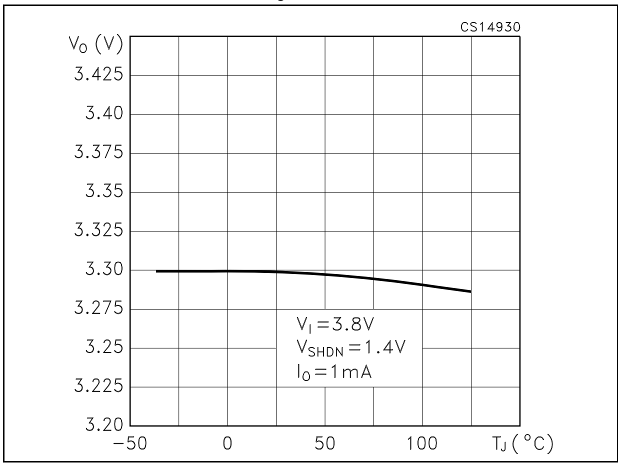


Figure 7. Shutdown voltage vs. temperature (V_0=1.35 V)

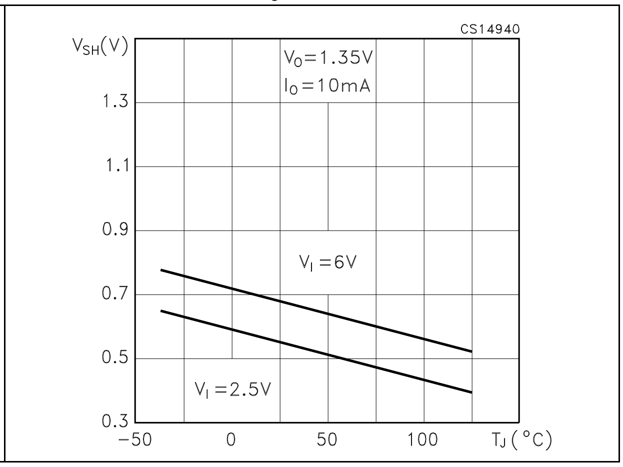


Figure 8. Shutdown voltage vs. temperature (V_0=3.3 V)

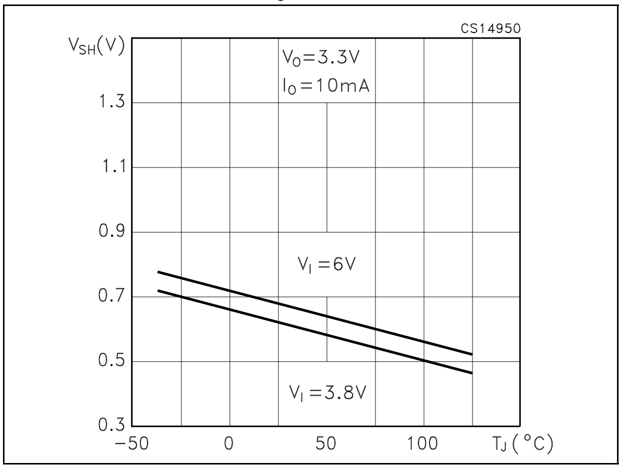


Figure 9. Line regulation vs. temperature (V_0=1.35 V)

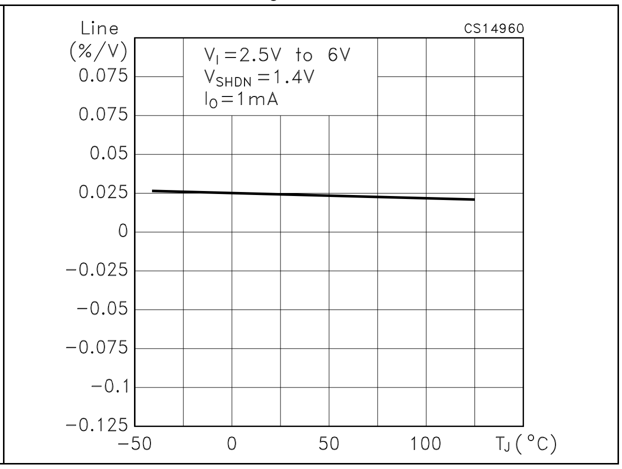


Figure 10. Line regulation vs. temperature (V_0=2.7 V)

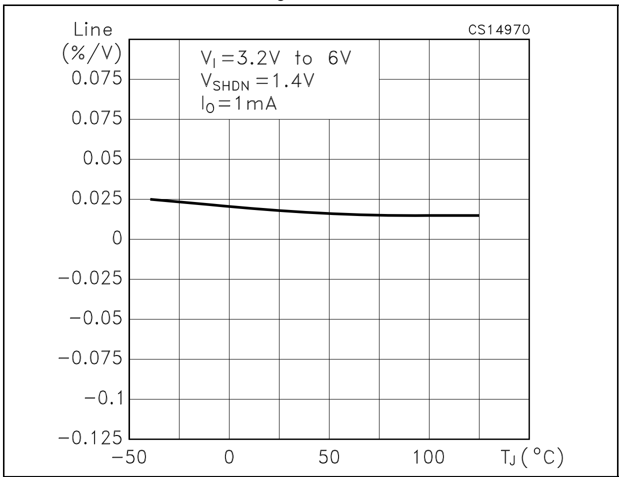


Figure 11. Line regulation vs. temperature (V_0=3.3 V)

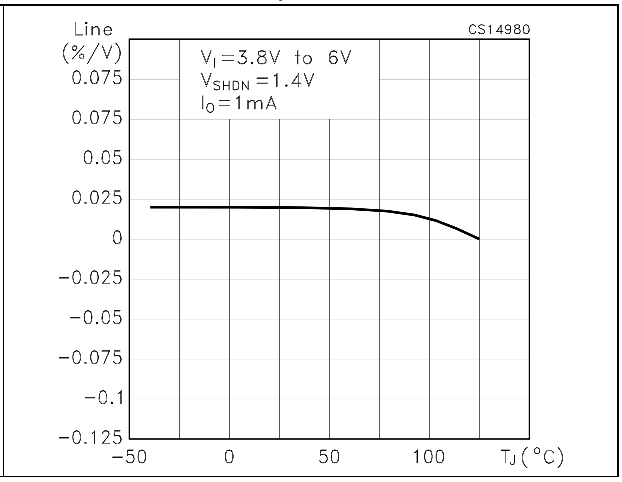


Figure 12. Load regulation vs. temperature (V_0=1.35 V)

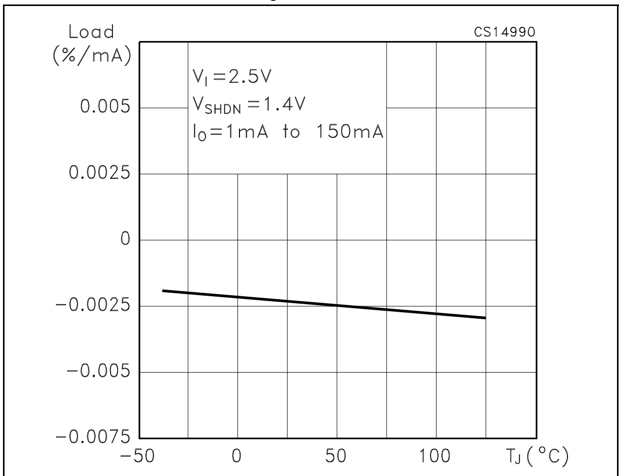


Figure 13. Load regulation vs. temperature (V_0=2.7 V)

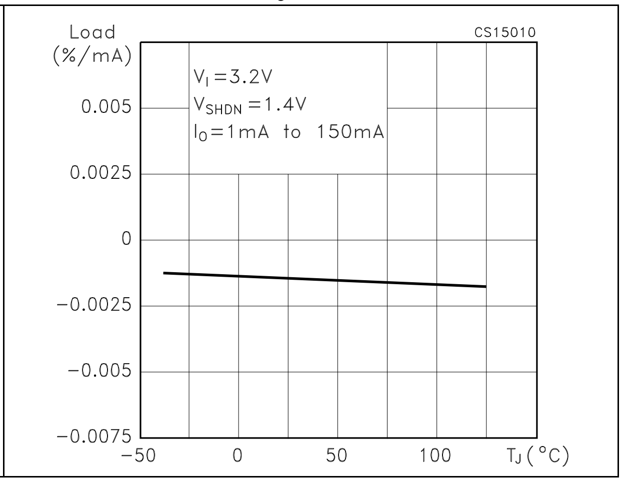


Figure 14. Load regulation vs. temperature (V_O=3.3 V)

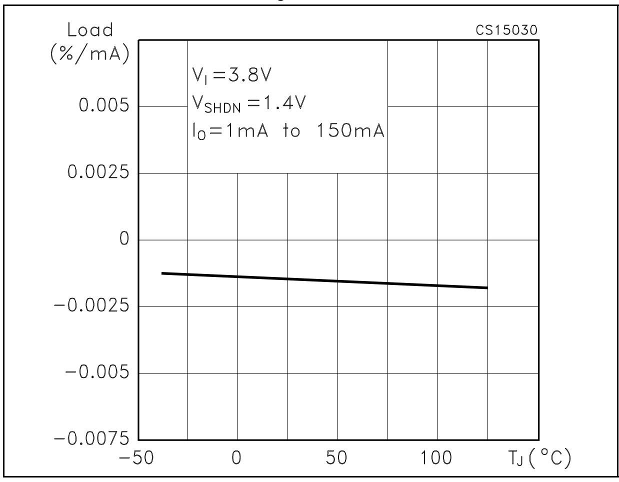


Figure 15. Quiescent current vs. temperature (V_I=2.5 V)

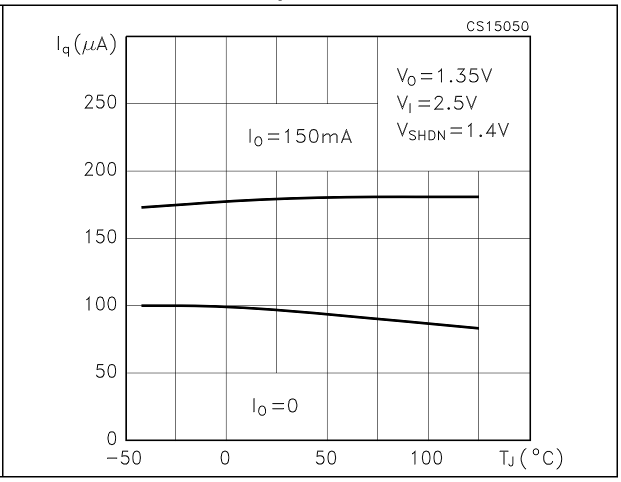


Figure 16. Quiescent current vs. temperature (V_I=6 V)

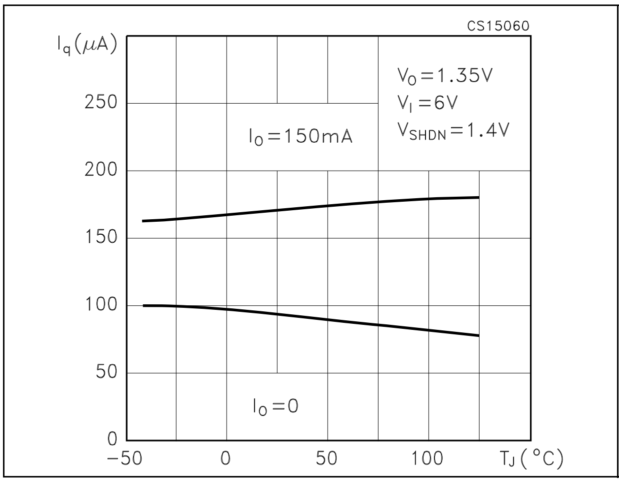


Figure 17. Quiescent current vs. load current

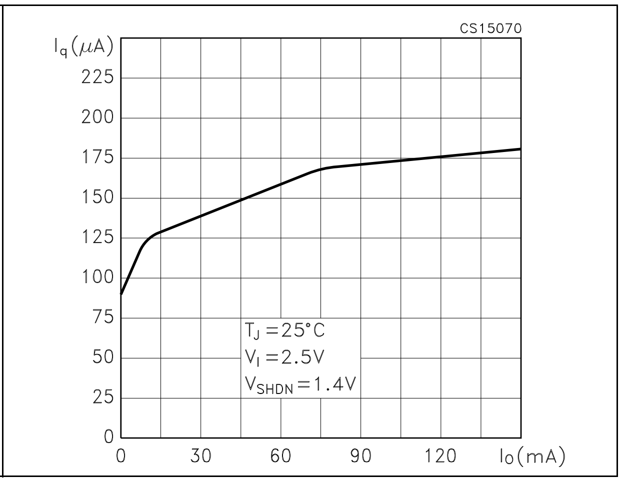


Figure 18. Supply voltage rejection vs. frequency

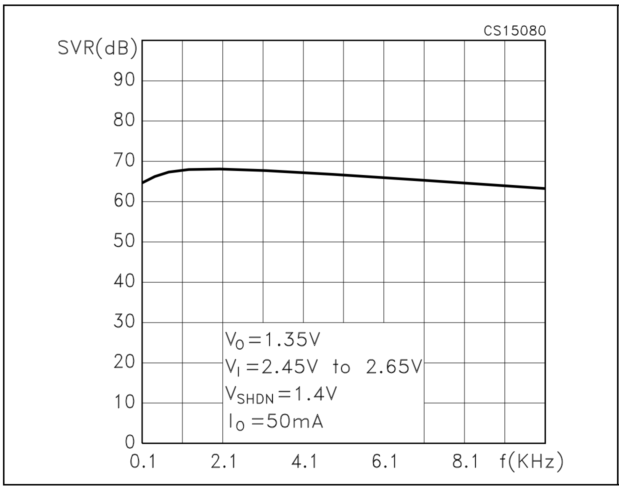
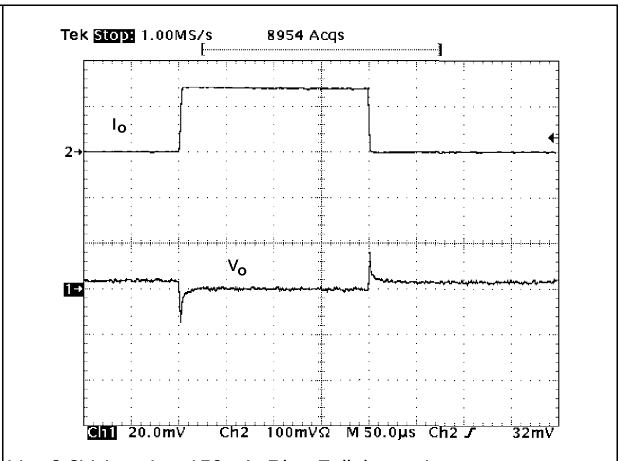
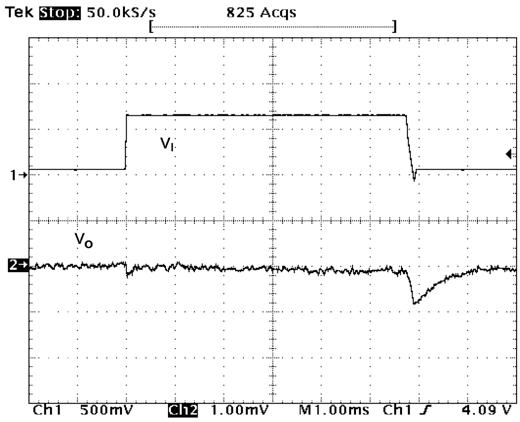


Figure 19. Load transient response



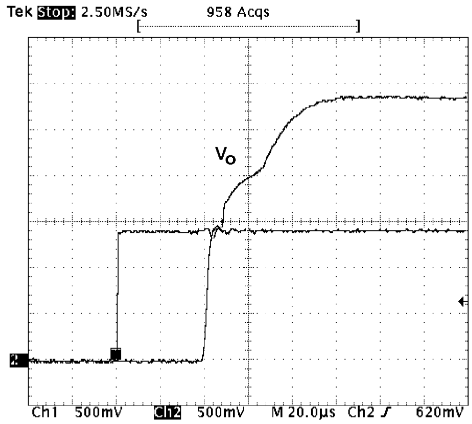
V_I = 3.2V, I_O = 1 to 150mA, Rise-Fall time = 1μsec

Figure 20. Line transient response



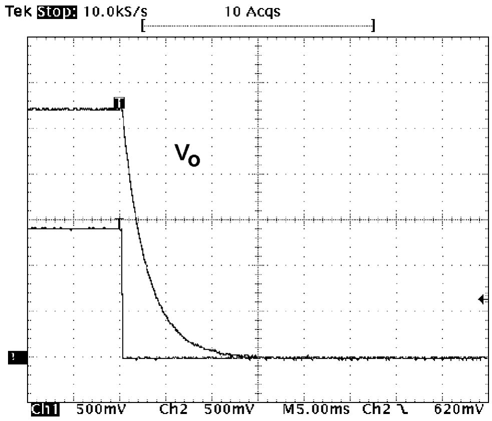
V_I = 3.8V to 4.4V, T_J = 25°C, I_O = 150mA, C_I = C_O = 1µF (X7R), C_{BYP} = 10nF, Rise-Fall time = 1µsec, V_O = 2.7V

Figure 21. Start-up



V_I = 3.3V, I_O = 1mA, C_I = C_O = 1µF (cer), C_{BYP} = 10nF, T_r = 20ns, V_O = 2.8V

Figure 22. Turn-off



V_I = 3.3V, I_O = 1mA, C_I = C_O = 1mF (cer), C_{BYP} = 10nF, T_f = 20ns, V_O = 2.8V

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 23. Flip-chip 5 drawings

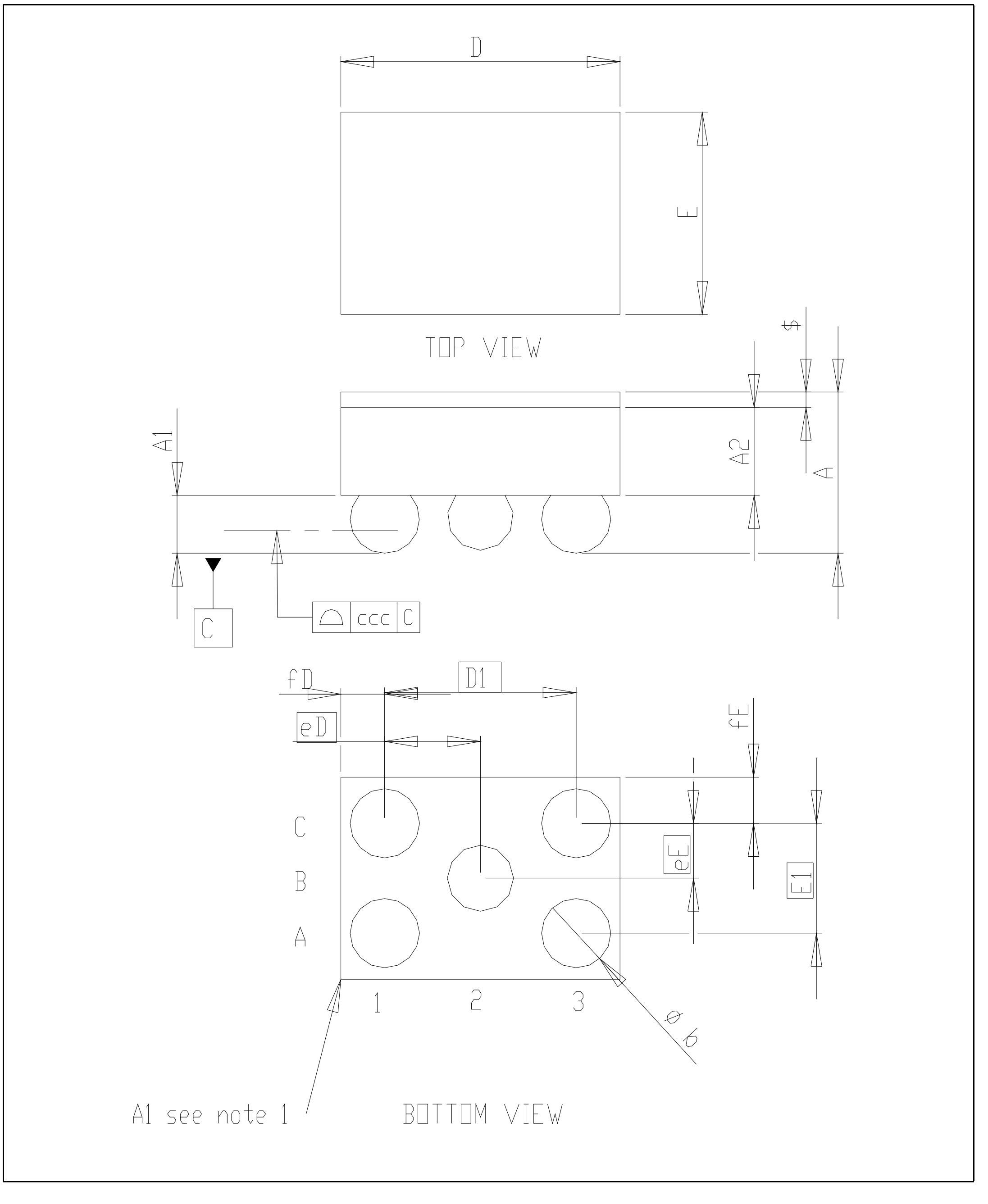


Table 6. Flip-chip 5 mechanical data

mm			
Dim.	**Min.**	**Typ.**	**Max.**
A	0.54	0.65	0.66
A1	0.21	0.25	0.29
A2	0.33	0.35	0.37
b	0.265	0.315	0.365
D	1.54	1.59	1.64
D1	0.83	0.87	0.91
E	1.19	1.24	1.29
E1	0.46	0.5	0.54
eD	0.395	0.435	0.475
eE	0.21	0.25	0.29
fD		0.360	
fE		0.370	
ccc		0.080	
$		0.05	

Figure 24. SOT23-5L drawings

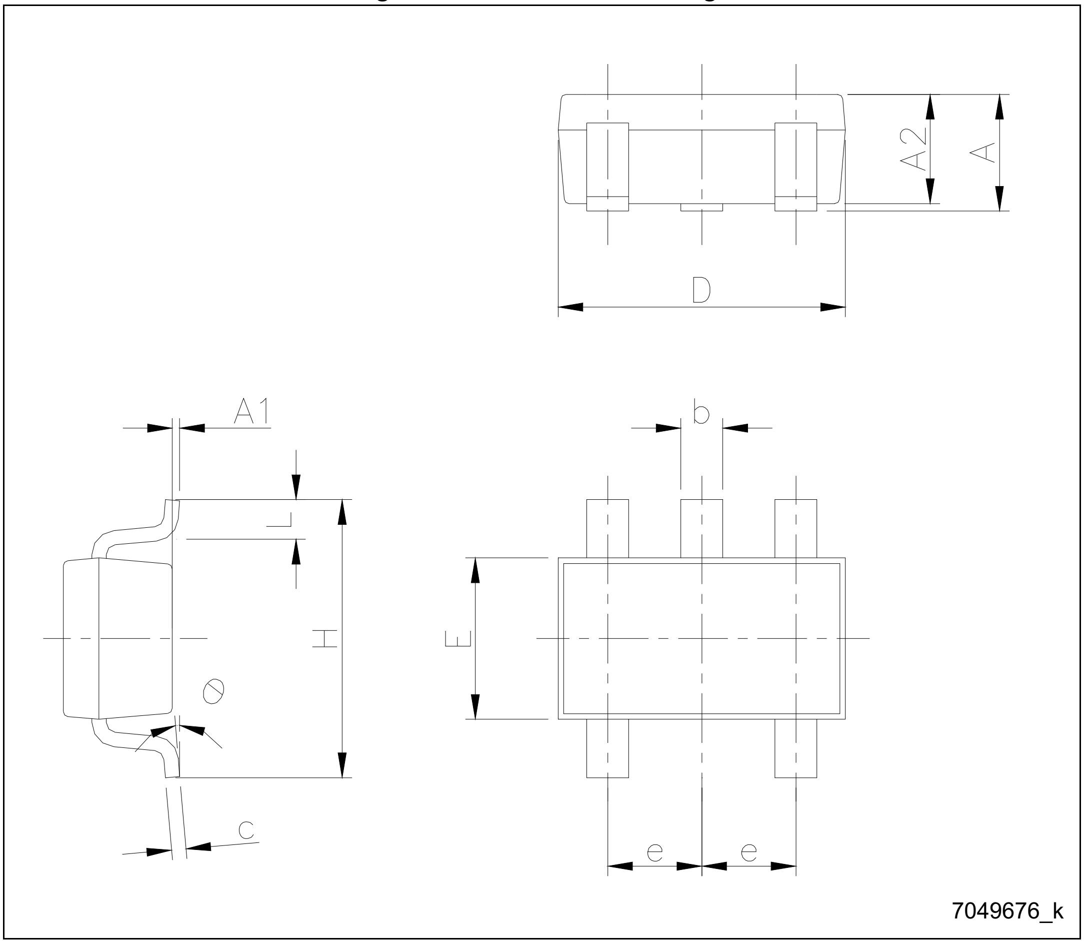


Figure 25. SOT23-5L recommended footprint (dimensions in mm)

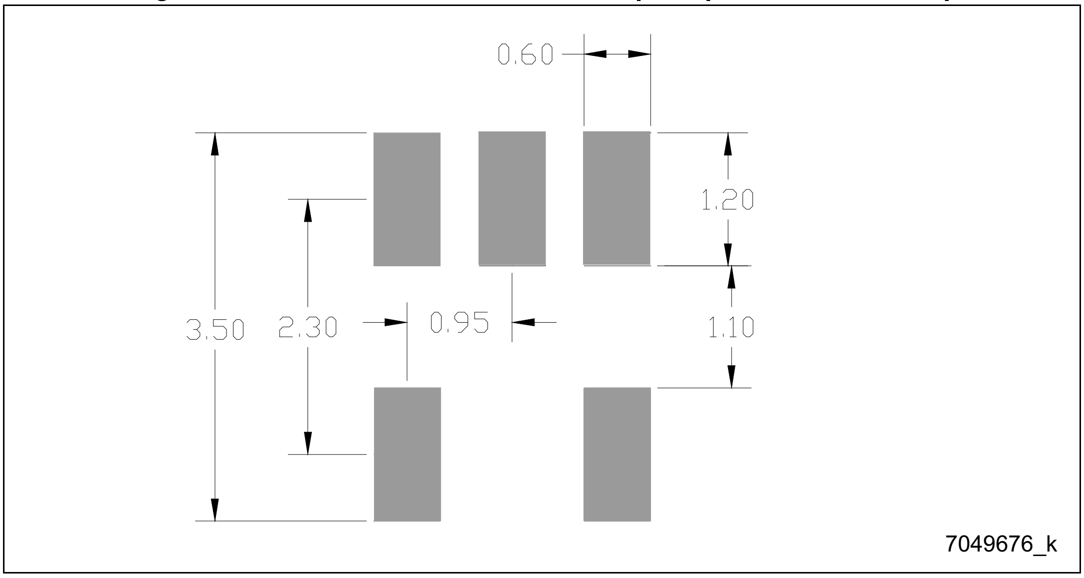


Table 7. SOT23-5L mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
b	0.30		0.50
c	2.09		0.20
D		2.95	
E		1.60	
e		0.95	
H		2.80	
L	0.30		0.60
θ	0		8

Figure 26. TSOT23-5L drawings

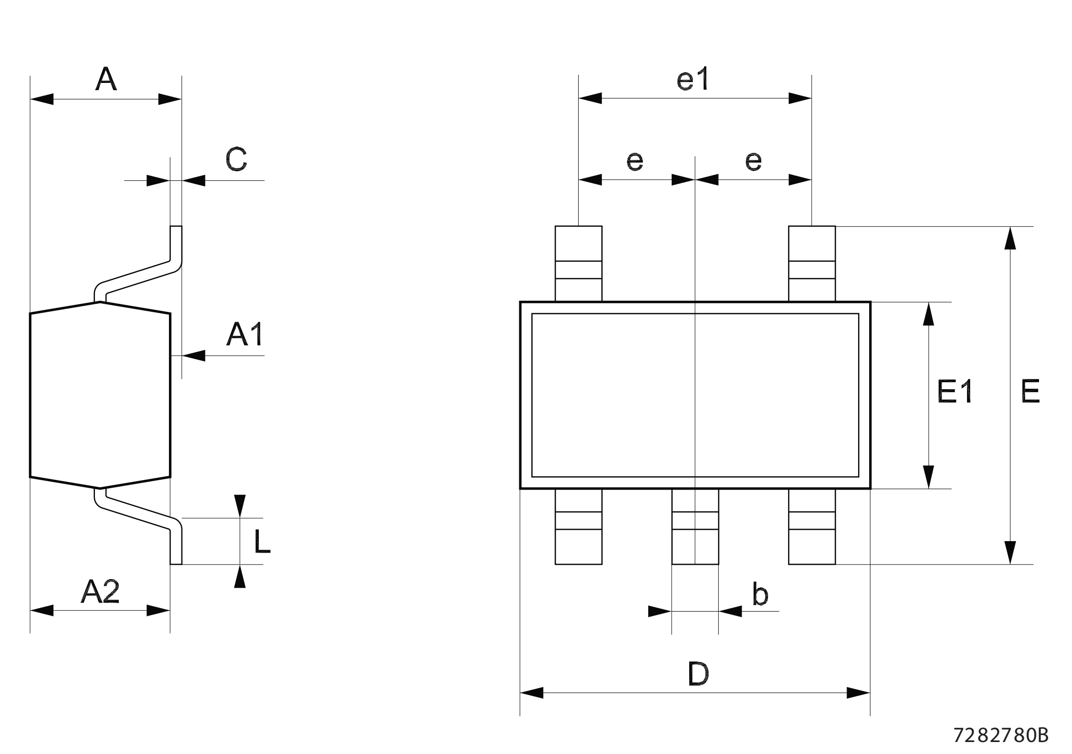


Table 8. TSOT23-5L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0		0.1
A2	0.7		1.0
b	0.3		0.5
C	0.08		0.2
D		2.9	
E		2.8	
E1		1.6	
e		0.95	
e1		1.9	
L	0.3		0.6

8 Packaging mechanical data

Figure 27. TSOT23-5L tape and reel drawings

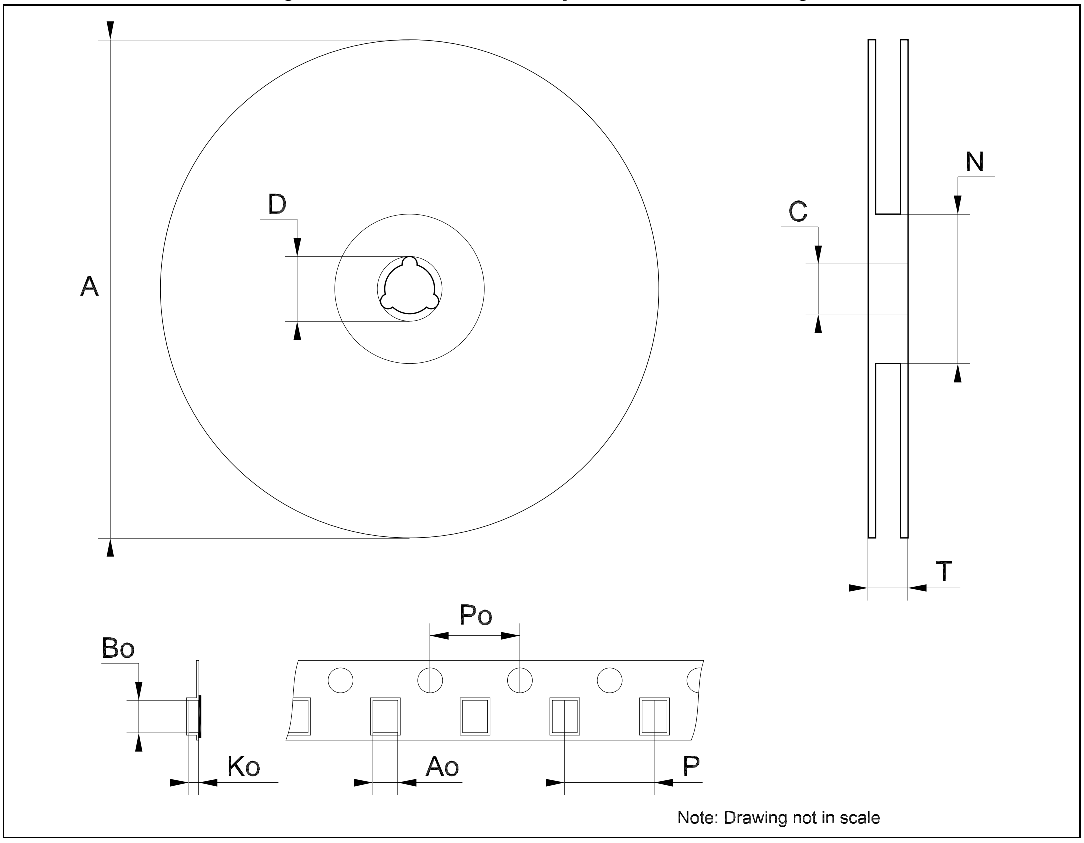


Table 9. Flip-chip 5 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			178
C	12.8		13.2
D	20.2		
N	49	50	51
T			12.4
Ao	1.60	1.65	1.70
Bo	1.27	1.32	1.37
Ko	0.76	0.81	0.86
Po	3.9	4	4.1
P	3.9	4	4.1

Table 10. SOT23-5L tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13.0	13.2
D	20.2		
N	60		
T			14.4
Ao	3.13	3.23	3.33
Bo	3.07	3.17	3.27
Ko	1.27	1.37	1.47
Po	3.9	4.0	4.1
P	3.9	4.0	4.1

Table 11. TSOT23-5L tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13.0	13.2
D	20.2		
N	60		
T			14.4
Ao	3.13	3.23	3.33
Bo	3.07	3.17	3.27
Ko	1.27	1.37	1.47
Po	3.9	4.0	4.1
P	3.9	4.0	4.1

9 Order codes

Table 12. Order codes

Packages			
SOT23-5L	**TSOT23-5L**	**Flip-chip**	**Output voltage**
LD3985M122R	LD3985G122R [1]		1.22 V
LD3985M18R	LD3985G18R	LD3985J18R	1.8 V
LD3985M25R	LD3985G25R	LD3985J25R	2.5 V
		LD3985J26R	2.6 V
LD3985M27R	LD3985G27R		2.7 V
LD3985M28R	LD3985G28R	LD3985J28R	2.8 V
LD3985M29R		LD3985J29R	2.9 V
LD3985M30R	LD3985G30R	LD3985J30R	3.0 V
LD3985M33R	LD3985G33R	LD3985J33R	3.3 V
LD3985M47R	LD3985G47R		4.7 V

1. Available on request.

10 Revision history

Table 13. Document revision history

Date	Revision	Changes
07-May-2004	6	Part number status changed on table 3.
05-Oct-2004	7	t_{ON} values are changed on table 5.
27-Oct-2004	8	Order codes changed - table 3.
17-Mar-2005	9	Improved drawing quality for figures 19 - 20 - 21 - 22.
10-Apr-2007	10	Order codes updated.
08-Jun-2007	11	Order code change.
20-Dec-2007	12	Modified: *Table 1*, *Table 12*, mechanical data for Flip-chip.
02-Dec-2008	13	Modified: *Table 6 on page 14* and *Figure 23 on page 17*.
03-Jan-2011	14	Modified: *Features on page 1* and *Table 12 on page 20*.
08-Jan-2014	15	Part number LD3985XX changed to LD3985. Modified title in cover page. Updated the description and *Section 7: Package mechanical data*. Added *Section 8: Packaging mechanical data*. Minor text changes.