

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

These miniature surface mount MOSFETs utilize high cell density process. Low  $R_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

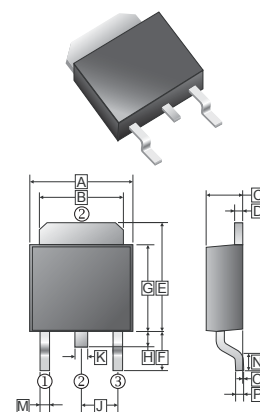
## FEATURES

- Low  $R_{DS(on)}$  provides higher efficiency and extends battery life.
- Miniature TO-252 surface mount package saves board space.
- High power and current handling capability.
- Low side high current DC-DC converter applications.

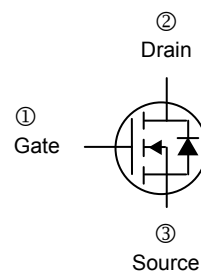
## PACKAGE INFORMATION

Package	MPQ	LeaderSize
TO-252	2.5K	13' inch

## TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30	REF.
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			



## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup>	$I_D @ T_C=25^\circ\text{C}$	75	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	40	A
Continuous Source Current (Diode Conduction) <sup>1</sup>	$I_S$	30	A
Total Power Dissipation <sup>1</sup>	$P_D @ T_C=25^\circ\text{C}$	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 ~ 175	$^\circ\text{C}$
<b>Thermal Resistance Ratings</b>			
Maximum Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	50	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	$^\circ\text{C} / \text{W}$

Notes :

- 1 Surface Mounted on 1" x 1" FR4 Board.
- 2 Pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	-	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
Gate-Body Leakage	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{DS}=0\text{V}$ , $V_{GS}=20\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=32\text{V}$ , $V_{GS}=0\text{V}$
		-	-	25		$V_{DS}=32\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=55^\circ\text{C}$
On-State Drain Current <sup>1</sup>	$I_{D(on)}$	34	-	-	A	$V_{DS}=5\text{V}$ , $V_{GS}=10\text{V}$
Drain-Source On-Resistance <sup>1</sup>	$R_{DS(ON)}$	-	-	6	m $\Omega$	$V_{GS}=10\text{V}$ , $I_D=75\text{A}$
		-	-	8		$V_{GS}=4.5\text{V}$ , $I_D=65\text{A}$
Forward Transconductance <sup>1</sup>	$g_{fs}$	-	22	-	S	$V_{DS}=15\text{V}$ , $I_D=75\text{A}$
Diode Forward Voltage	$V_{SD}$	-	1.1	-	V	$I_S = 34\text{A}$ , $V_{GS} = 0\text{V}$
<b>Dynamic <sup>2</sup></b>						
Total Gate Charge	$Q_g$	-	4.0	-	nC	$V_{DS}= 15\text{V}$ $V_{GS}= 4.5\text{V}$ $I_D= 75\text{A}$
Gate-Source Charge	$Q_{gs}$	-	1.1	-		
Gate-Drain Charge	$Q_{gd}$	-	1.4	-		
Turn-on Delay Time	$T_{d(on)}$	-	16	-	nS	$V_{DD}=25\text{V}$ $I_D=34\text{A}$ $V_{GEN}=10\text{V}$ $R_L=25\Omega$
Rise Time	$T_r$	-	5	-		
Turn-off Delay Time	$T_{d(off)}$	-	23	-		
Fall Time	$T_f$	-	3	-		
Source-Drain Reverse Recovery Time	$T_{RR}$	-	50	-		$I_F=34\text{A}$ , $di/dt = 100\text{A}/\mu\text{S}$

Notes :

- 1 Pulse test : Pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- 2 Guaranteed by design, not subject to production testing.