

Dual Synchronous Buck PWM Controllers and One Linear Controller

Features

- Two Synchronous Buck Converters and a Linear Regulator
- VIN range up to 12V
- Input Power Supplies Require 12V and 5V or use 12V to generate a Shunt Regulator 5.8V
- 0.6V Reference for VOUT1 and VOUT3 with 0.8% accurate
- 3.3V Reference for VOUT2 with 0.8% accurate
- Buffered VTT Reference Output
- Three Outputs have Independent Soft-Start and Enable
- Internal 300kHz Oscillator and Programmable Frequency range from 70 kHz to 800kHz
- Synchronous Switching Frequency
- DDR mode or Independent Mode Selection
- Phase Shift Selection
- Power Good Function
- Short-Circuit Protection for VOUT1 and VOUT2
- Thermally Enhanced TSSOP-24 and QFN-32 Package
- Lead Free Available (RoHS Compliant)

Applications

- Graphic Cards
- DDR memory Power Supplies
- Low-Voltage Distributed Power Supplies

General Description

The APW7066 has two synchronous buck PWM controllers and one linear controller with high precision internal references voltage to offer accurate outputs. The PWM controllers are designed to drive two N-channel MOSFETs in synchronous buck topology, and the linear controller drives an external N-channel MOSFET. The device requires 12V and 5V power supplies, if the 5V supply is not available, VCC12 can offer an optional shunt regulator 5.8V for 5V supply.

All outputs have independent soft-start and enable functions by SS/EN pins to control. Connect a capacitor from each SS/EN pin to the ground for setting the soft-start time, and pulling the SS/EN pin below 1V to disable regulator. Pull the SS2/EN2 to VCC, enter the DDR mode, the SS1/EN1 controls both VOUT1 and VOUT2, and allows VOUT2 to track VOUT1. It also offers the phase shift function by REFOUT pin to select the phase shift between VOUT1 and VOUT2 in DDR mode or Independent mode. When all SS/EN pins exceed 3.3V and no faults are detected, the PGOOD pin goes high to indicate the regulators are ready. If any of the SS/EN pins goes below 3.2V or any of the outputs has a fault condition, the PGOOD pin will be pulled low.

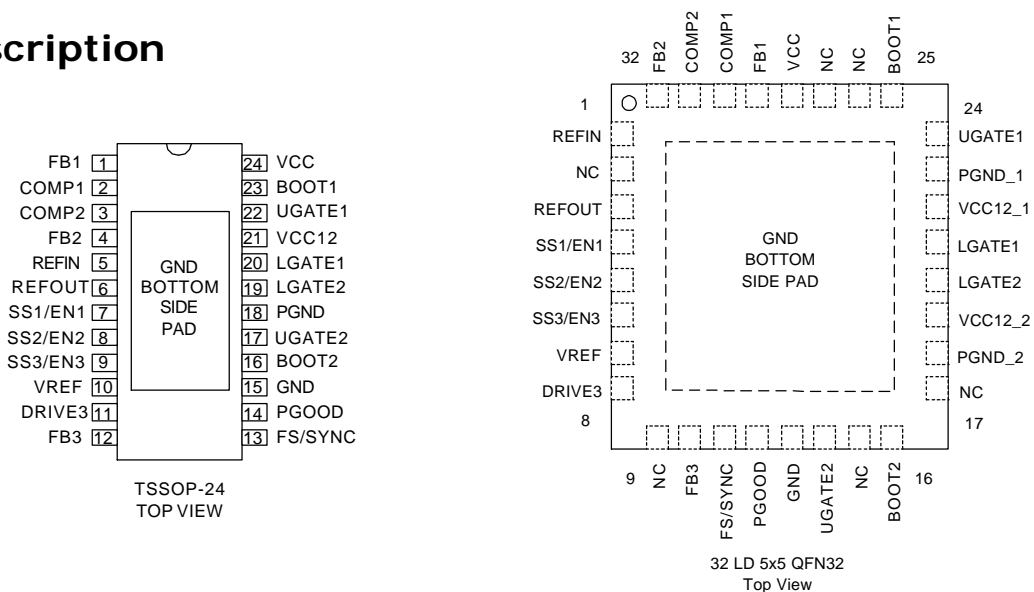
The internal oscillator is nominally 300kHz (keep the FS/SYNC pin open or short to GND), and it offers the programmable frequency function from 70kHz to 800kHz; connecting a resistor from FS/SYNC to VCC to decrease the frequency, conversely, connect a resistor from FS/SYNC to GND to increase the frequency. The IC also provides the synchronous frequency function. Connect the LGATE signal of another converter to FS/SYNC pin; forcing the switching frequency to follow

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General Description (Cont.)

the external clock. The possible synchronous frequency is from 150kHz to 800kHz. There is no Rds(on) sensing or under-voltage sensing on APW7066. However, it provides a simple short-circuit protection by monitoring the COMP1 and COMP2 for over-voltage. When any of two pins exceeds their trip point and the condition persists for 1-2 internal clock cycle (3-6us at 300kHz), then it will shut down all regulators.

Pin Description

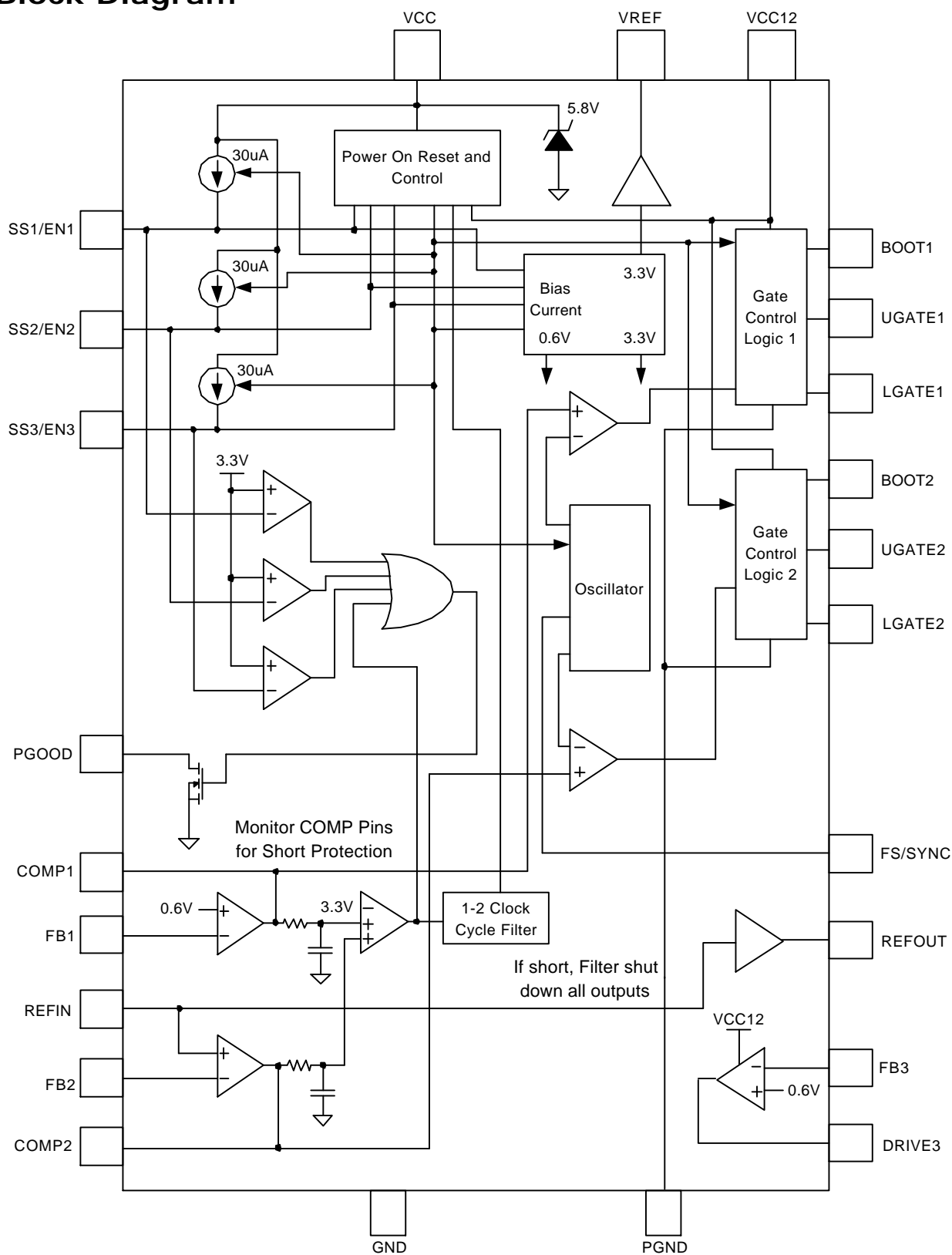


Ordering and Marking Information

| | |
|---|--|
| <p>APW7066 □□-□□□</p> <p>Lead Free Code</p> <p>Handling Code</p> <p>Temp. Range</p> <p>Package Code</p> | <p>Package Code</p> <p>R : TSSOP-P * QA : QFN-32</p> <p>Operating Ambient Temp. Range</p> <p>C : 0 to 70°C</p> <p>Handling Code</p> <p>TU : Tube TR : Tape & Reel</p> <p>TY : Tray (for QFN only)</p> <p>Lead Free Code</p> <p>L : Lead Free Device Blank : Original Device</p> |
| <p>APW7066 R :</p> <p>APW7066 XXXXX</p> | <p>XXXXX - Date Code</p> |
| <p>APW7066 QA :</p> <p>APW7066 XXXXX</p> | <p>XXXXX - Date Code</p> |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|------------------------------|-------------------------------------|--------------|------|
| VCC12 | VCC12 to GND | -0.3 to 15 | V |
| VCC, separate supply | VCC, separate supply | -0.3 to 5.5 | V |
| VCC, shunt regulator | VCC, shunt regulator to GND | -0.3 to 6 | V |
| UGATE1, UGATE2, BOOT1, BOOT2 | UGATE1, UGATE2, BOOT1, BOOT2 to GND | -0.3 to 30 | V |
| LGATE1, LGATE2, DRIVE3 | LGATE1, LGATE2, DRIVE3 to GND | -0.3 to 15 | V |
| FS/SYNC | FS/SYNC to GND | -0.3 to 15 | V |
| REFIN, REFOUT, PGOOD, VREF | REFIN, REFOUT, PGOOD, VREF to GND | -0.3 to VCC | V |
| FB1, COMP1, FB2, COMP2, FB3 | FB1, COMP1, FB2, COMP2, FB3 to GND | -0.3 to VCC | V |
| SS1/EN1, SS2/EN2, SS3/EN3 | SS1/EN, SS2/EN2, SS3/EN3 to GND | -0.3 to VCC | V |
| PGND | PGND to GND | -0.3 to +0.3 | V |
| T _A | Operating Temperature Range | 0 to +70 | °C |
| T _J | Maximum Junction Temperature | +150 | °C |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature (Soldering, 10sec) | 260 | °C |

Electrical Characteristics

Operating Conditions: V_{CC} = 5V, V_{CC12} = 12V, T_A = 0 to 70°C, Unless Otherwise Specified.

| Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------------------------------|---|------|------|------|-------|
| INPUT SUPPLY POWER | | | | | |
| Input Supply Current (Quiescent) | VCC; outputs disabled | | 4 | | mA |
| | VCC12; outputs disabled | | 6 | | mA |
| Input Supply Current (Dynamic) | VCC12; UGATEs, LGATEs CL = 1nF, 300KHz | | 50 | | mA |
| | VCC; UGATEs, LGATEs CL = 1nF, 300KHz | | 7 | | mA |
| Shunt Regulator Output Voltage | 20mA current; ~Equivalent to 300Ω resistor VCC to 12V | 5.6 | 5.8 | 6.0 | V |
| Shunt Regulator Current | 300Ω resistor VCC to 12V | | 20 | 60 | mA |

Electrical Characteristics (Cont.)

Operating Conditions: $V_{CC} = 5V$, $V_{CC12} = 12V$, $T_A = 0$ to $70^\circ C$, Unless Otherwise Specified.

| Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|--|------|-------|------|--------------|
| INPUT SUPPLY POWER | | | | | |
| Power-On Reset Threshold | VCC Rising | 4.15 | 4.23 | 4.4 | V |
| | VCC Falling | 3.9 | 4.0 | 4.15 | V |
| | VCC12 Rising | 7.55 | 7.8 | 8 | V |
| | VCC12 Falling | 7.1 | 7.3 | 7.55 | V |
| SYSTEM ACCURACY | | | | | |
| Outputs 1 and 3 Reference Voltage | | | 0.6 | | V |
| Output 2 Reference Voltage | | | 3.3V | | |
| Outputs 1 and 2 System Accuracy | | -0.8 | | 0.8 | % |
| Output 3 System Accuracy | | -0.8 | | 0.8 | % |
| OSCILLATOR | | | | | |
| Accuracy | | -20 | | 20 | % |
| Frequency | FS/SYNC pin open | 240 | 300 | 360 | KHz |
| Adjustment Range | FS/SYNC pin: resistor to GND; resistor to VCC12 | 70 | | 800 | KHz |
| Sawtooth Amplitude | | | 2.1 | | V |
| Duty-Cycle Range | | 0 | | 85 | % |
| ERROR AMPLIFIER (OUT1 and OUT2) | | | | | |
| Open-Loop Gain | $R_L = 10k\Omega$ to ground | | 85 | | dB |
| Open-Loop Bandwidth | $C_L = 100pF$, $R_L = 10k\Omega$ to ground | | 15 | | MHz |
| Slew Rate | $C_L = 100pF$, $R_L = 10k\Omega$ to ground | | 4 | | V/ μs |
| EA Offset | COMP1/2 to FB1/2; compare to internal VREF/REFIN | | 2 | | mV |
| Maximum Output Voltage | $R_L = 10k\Omega$ to ground; (may trip short-circuit) | | VCC | | V |
| Output High Source Current | COMP1/2, VCOMP=2V | | -50 | | mA |
| Output Low Sink Current | COMP1/2, VCOMP=2V | | 45 | | mA |
| PROTECTION AND MONITOR | | | | | |
| Under-Voltage Threshold (COMP1 and COMP2) | Causes PGOOD to go low; if there for a filter time, implies the COMP pin(s) is out-of-range, and shuts down IC | | 3.3 | | V |
| UV filter time | Based on internal oscillator clock frequency (nominal 300kHz = 3.3 μs clock period) | 1 | | 2 | Clock pulses |
| PGOOD Low Voltage | IPGOOD = 2mA | | 0.1 | 0.3 | V |
| LINEAR REGULATOR (OUT3) | | | | | |
| EA Offset | DRIVE3 to FB3; compare to internal VREF | | 2 | | mV |
| DRIVE3 High Output Voltage | | | VCC12 | | |

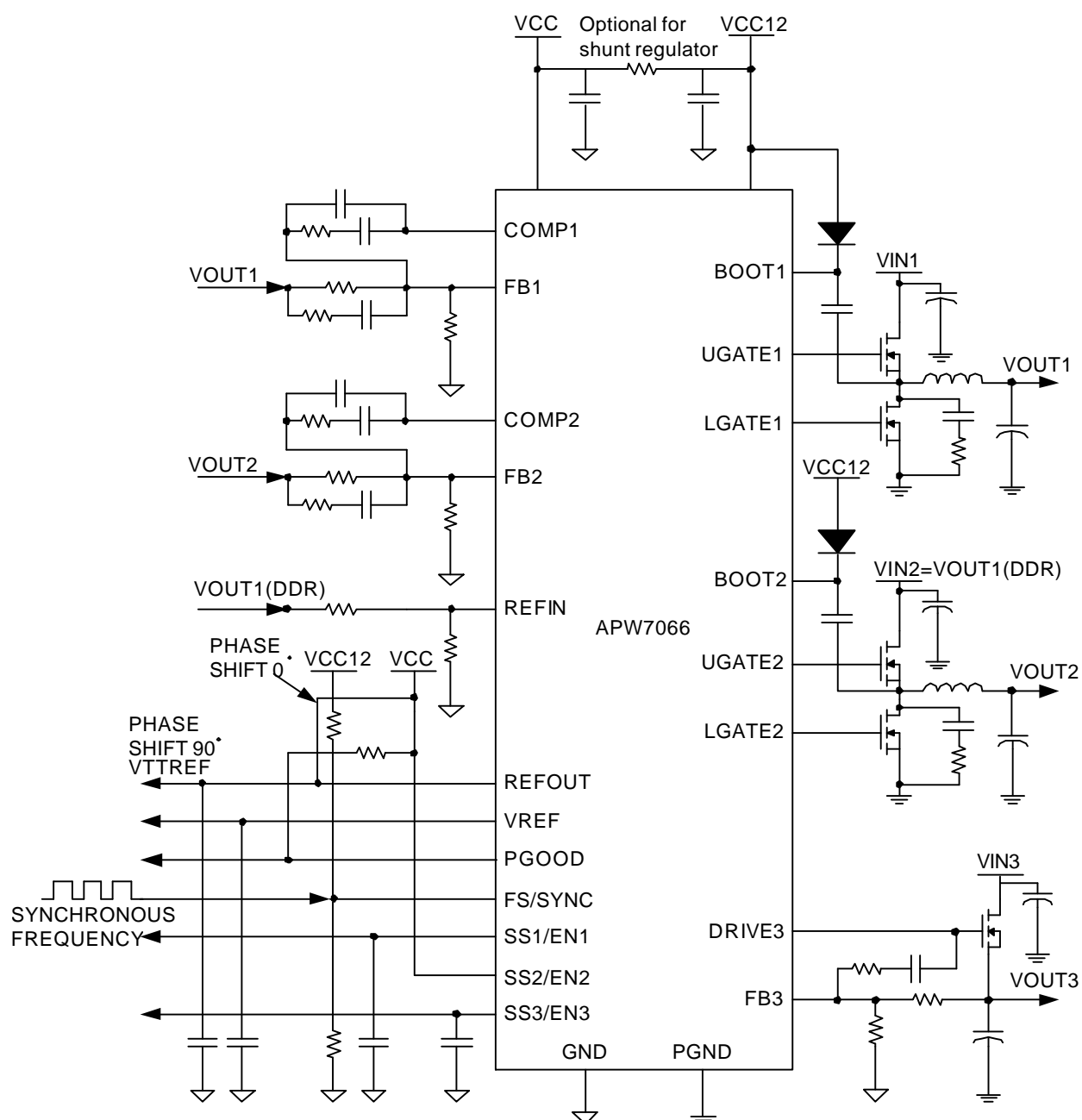
Electrical Characteristics (Cont.)

Operating Conditions: $V_{CC} = 5V$, $V_{CC12} = 12V$, $T_A = 0$ to $70^\circ C$, Unless Otherwise Specified.

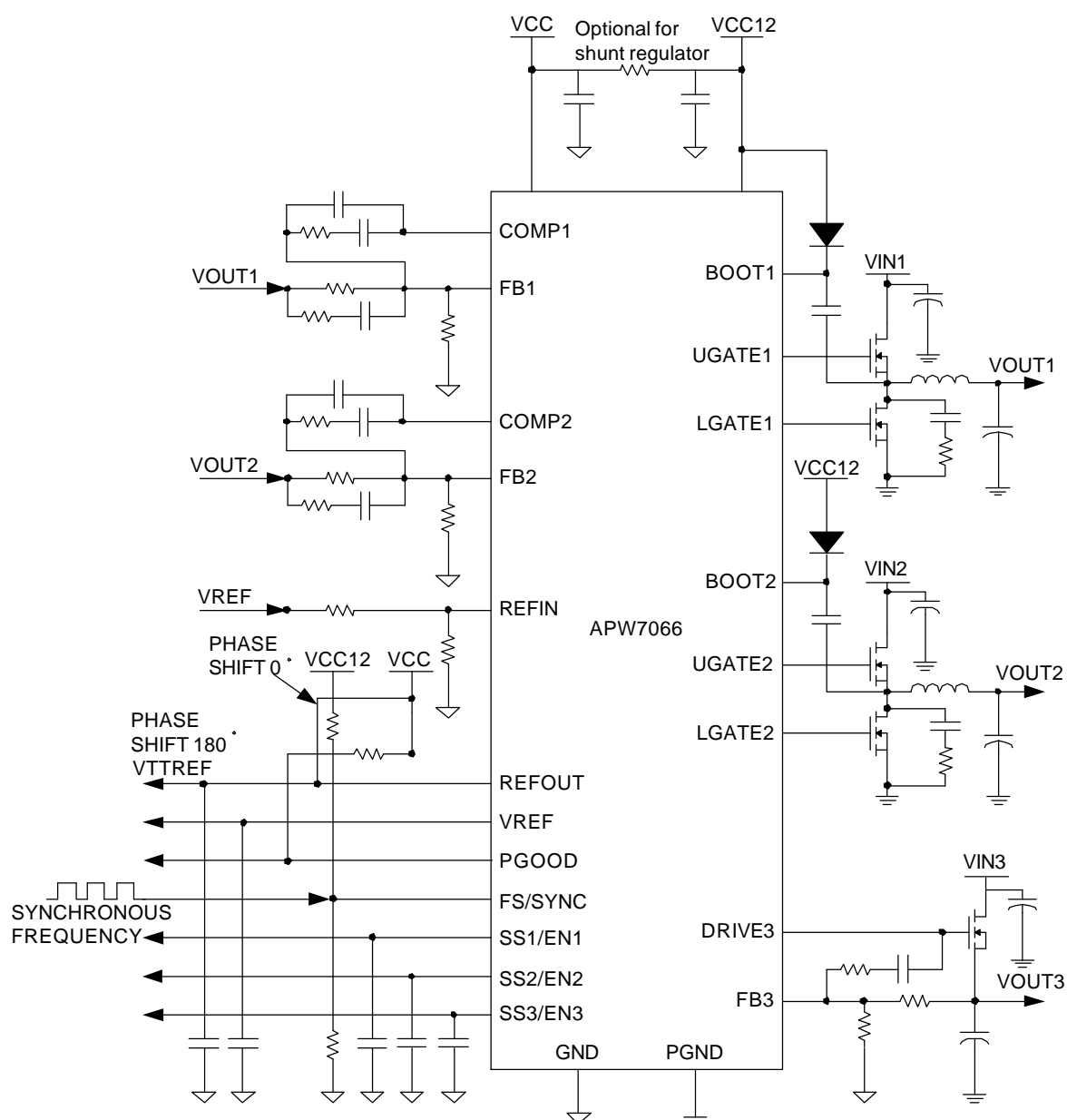
| Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---------------------------------------|---|------|------|------|----------|
| LINEAR REGULATOR (OUT3) | | | | | |
| DRIVE3 High Output Source Current | | | 1.5 | | mA |
| DRIVE3 Low Output Sink Current | | | 2.5 | | mA |
| VREF | | | | | |
| Output Voltage | 1.1 μ F max capacitance | | 3.3 | | V |
| Output Accuracy | | -0.8 | | +0.8 | % |
| Source Current | | | | 2.0 | mA |
| REFOUT (VTTREF) | | | | | |
| Output Voltage | Determined by REFIN voltage | 0.6 | | 3.3 | V |
| Offset Voltage | | -10 | | +10 | mV |
| Source Current | | 0.2 | | 20 | mA |
| Sink Current | | | | 0.48 | mA |
| Output Capacitance | | | 0.1 | | μ F |
| Output High Voltage Minimum | To select 0 degree phase; see Table 1 | | 3.8 | VCC | V |
| ENABLE/SOFTSTART (SS/EN 1,2,3) | | | | | |
| Enable Threshold | EN Rising | | 1.05 | | V |
| | EN falling | | 0.95 | | |
| Soft-Start Current | | | -30 | | μ A |
| Soft-Start High Voltage | End of ramp | | 3.5 | | V |
| Output High Voltage | To select DDR mod; see Table 1 | | 3.8 | VCC | V |
| FS/SYNC PLL | | | | | |
| Frequency range of Lock-in | | 150 | | 800 | KHz |
| High Voltage | (from LG pin of another IC, for example) | | | 12 | V |
| GATE DRIVERS | | | | | |
| Output1 GATE Driver Source | UGATE1, LGATE1=3V, BOOT=12V | | 1.8 | | A |
| Output2 GATE Driver Source | UGATE2, LGATE2=3V, BOOT=12V | | 1 | | A |
| Output1 GATE Driver Sink | UGATE1, LGATE1=3V, BOOT=12V | | 2.5 | | Ω |
| Output2 GATE Driver Sink | UGATE2, UGATE2=3V, BOOT=12V | | 4 | | Ω |
| Output Voltage | UGATE1, UGATE2 | | | 30 | V |
| Output Voltage | LGATE1, LGATE2 | | 12 | | V |

Typical Application Circuit

APW7066
DDR MODE



APW7066
INDEPENDENT MODE



Function Pin Descriptions

VCC

Power supply input pin. Connect a nominal 5V power supply to this pin for the control circuit, or connect a resistor (nominally 300Ω) to VCC12 for a shunt regulator function (typical 5.8V). It is recommended that a decoupling capacitor (1 to 10uF) is connected to the GND for noise decoupling.

GND

This pin is the signal ground pin. The metal thermal pad under the package is the IC substrate; connects the GND pin and metal thermal pad together on the board, and ties to the good GND plane for electrical and thermal conduction.

VCC12

Power supply input pin. Connect a nominal 12V power supply to this pin for the gate driver. It is recommended that a decoupling capacitor (1 to 10uF) is connected to the GND for noise decoupling.

PGND

This pin is the power ground pin for the gate driver and linear driver circuit. It should be tied to the GND.

FB1, FB2, FB3

These pins are the inverting inputs of the error amplifiers of their respective regulators. They are used to set the output voltage and the compensation components.

SS1/EN1, SS2/EN2, SS3/EN3

These pins provide two functions. Connect a capacitor to the GND for setting the soft-start time. Use an open drain logic signal to pull the SS/EN pin low to disable the respective output, leave open to enable the respective output.

COMP1, COMP2

These pins are the outputs of error amplifiers of their respective regulators. They are used to set the compensation components.

UGATE1, UGATE2

These pins provide the gate driver for the upper MOSFETs of VOUT1 and VOUT2.

LGATE1, LGATE2

These pins provide the gate driver for the lower MOSFETs of VOUT1 and VOUT2.

BOOT1, BOOT2

These pins provide the bootstrap voltage to the gate driver for driving the upper MOSFETs. It can be connected to a power voltage directly, but the difference voltage between the BOOT and VIN must be high enough to drive the upper MOSFETs.

REFIN

This pin is the reference input voltage of error amplifier of the VOUT2. It also provides the voltage into a buffer, which is out on the REFOUT pin.

REFOUT

This pin provides a buffered voltage, which is from REFIN pin. In Independent mode, it can be used by other ICs. In DDR mode, it is from the VOUT1, and can be used as the VTT buffer.

This pin also uses to select the phase shift (see table1). When this pin pulls to VCC, the buffer is disabled and the REFOUT is not available for use. It is recommended that a 0.1uF capacitor is connected to the ground for stability.

VREF

This pin provides a 3.3V reference voltage, which can be used by the REFIN pin or other ICs as a voltage reference. It is recommended that a 1uF capacitor is connected to ground for stability.

DRIVE3

This pin drives the gate of an external N-channel MOSFET for linear regulator.

PGOOD

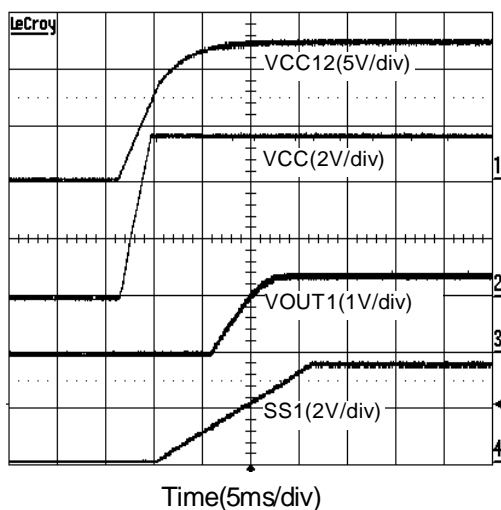
This pin is an open drain device; connect a pull up resistor to the VCC for PGOOD function.

FS/SYNC

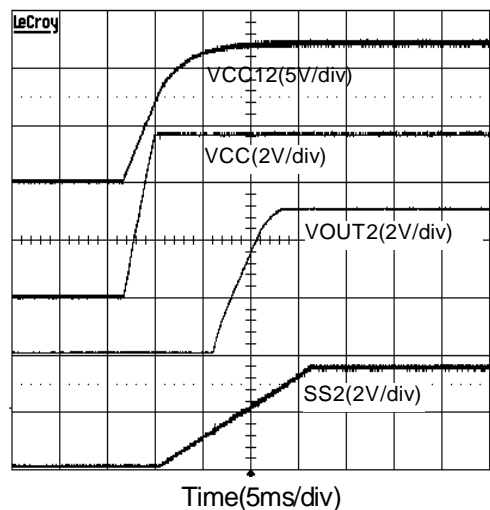
This pin is used to adjust the switching frequency. Connecting a resistor from FS/SYNC pin to the ground increases the switching frequency. Conversely, connecting a resistor from this pin to the VCC12 reduces the switching frequency. In addition, this pin also provides synchronous frequency function. An external clock can be fed into this pin, and force the switching frequency to follow the external clock.

Typical Characteristics

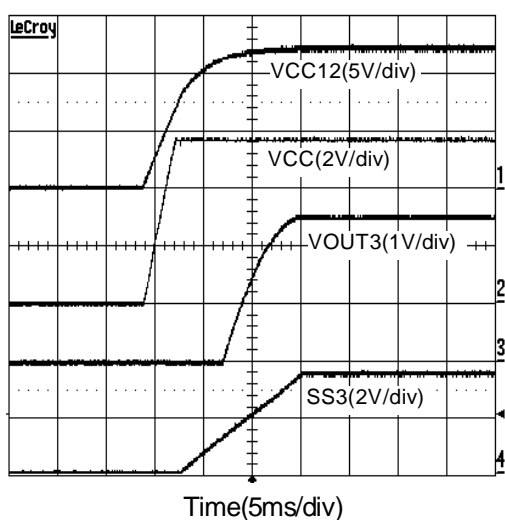
VOUT1 Power Up



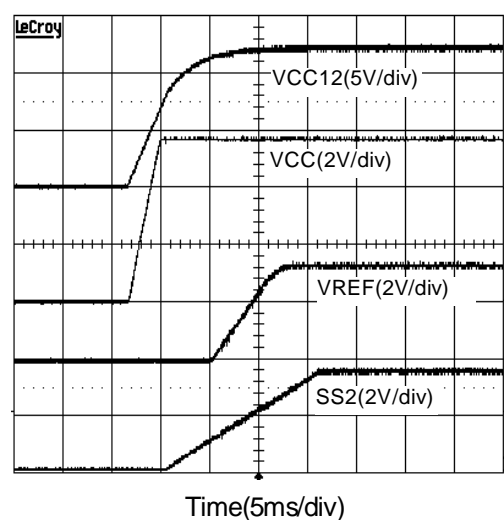
VOUT2 Power Up



VOUT3 Power Up

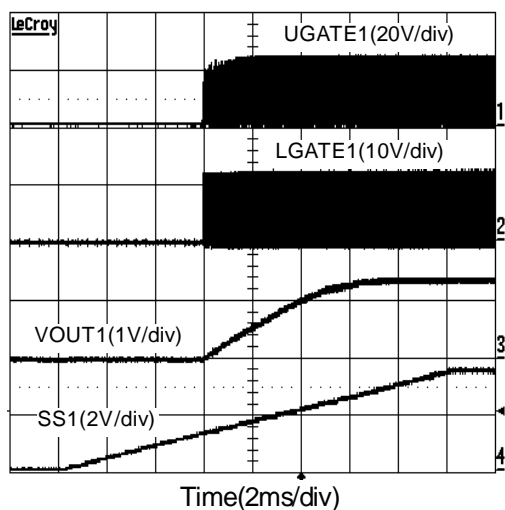


VREF Power Up

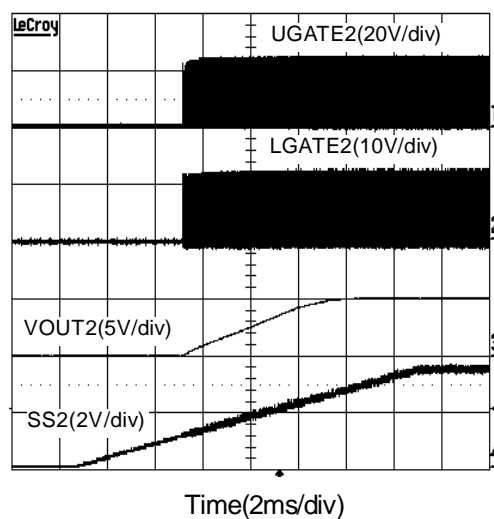


Typical Characteristics (Cont.)

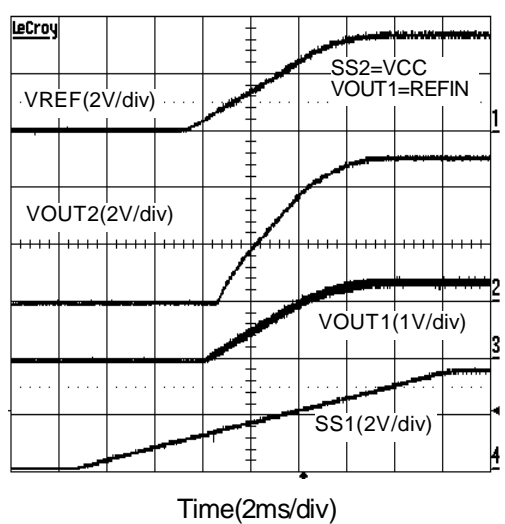
VOUT1 Power Up



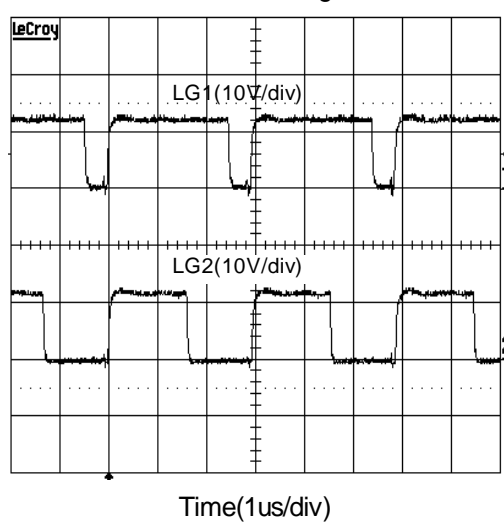
VOUT2 Power Up



DDR Mode Power Up

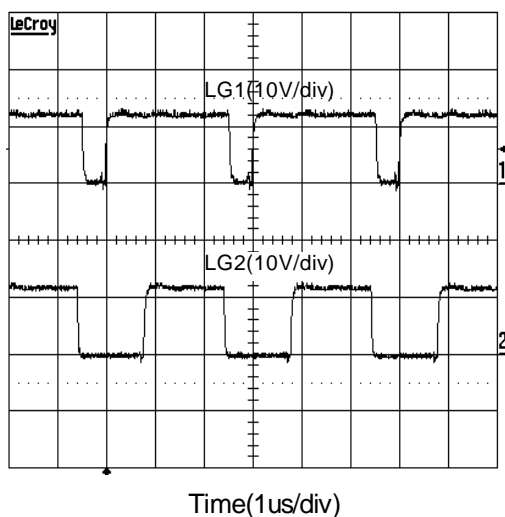


Phase Shift 0 degrees

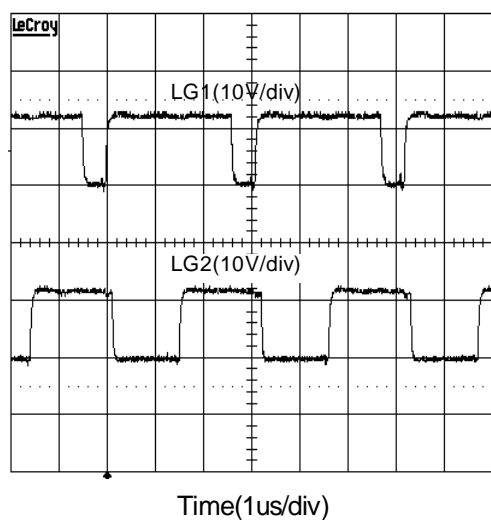


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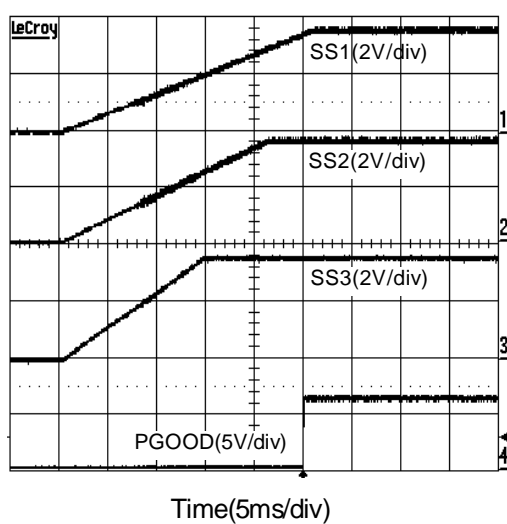
Phase Shift 90 degrees



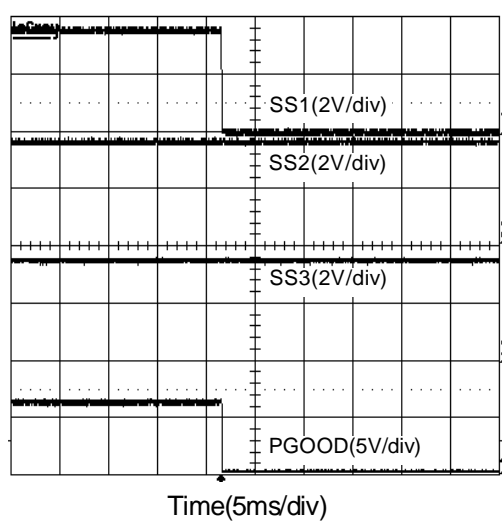
Phase Shift 180 degrees



PGOODHigh

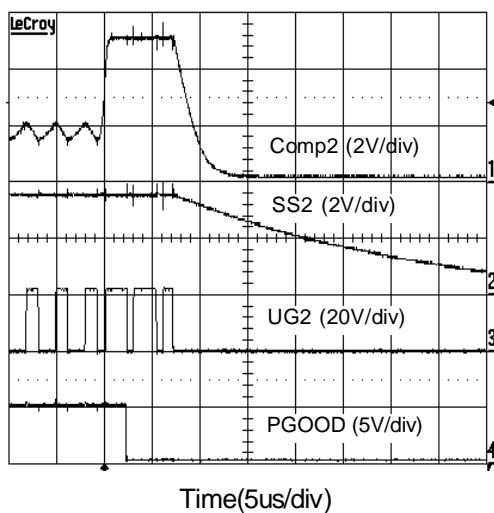


PGOODLow

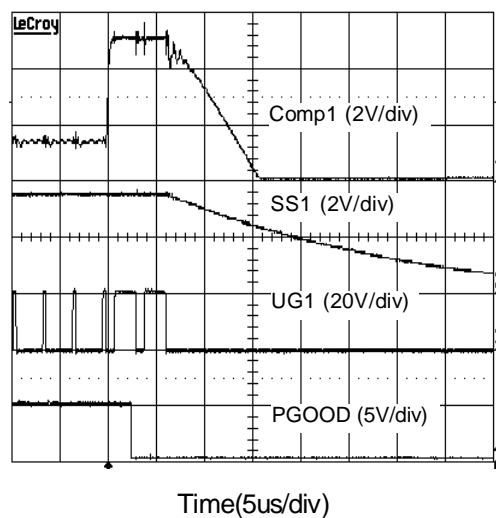


Typical Characteristics (Cont.)

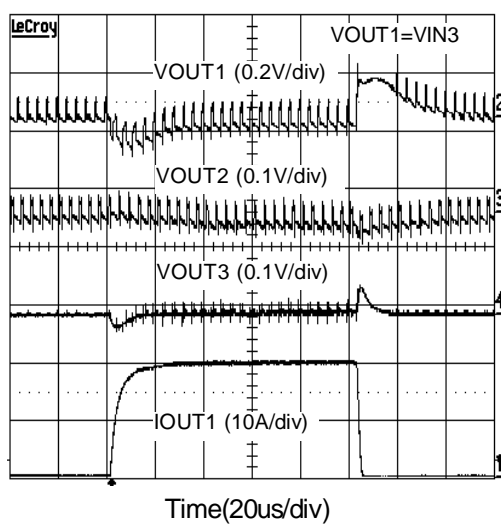
VOUT2 Short Circuit Protection



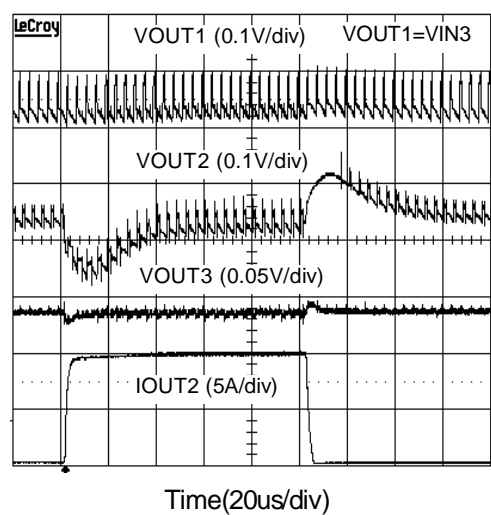
VOUT1 Short Circuit Protection



VOUT1 Load Transient

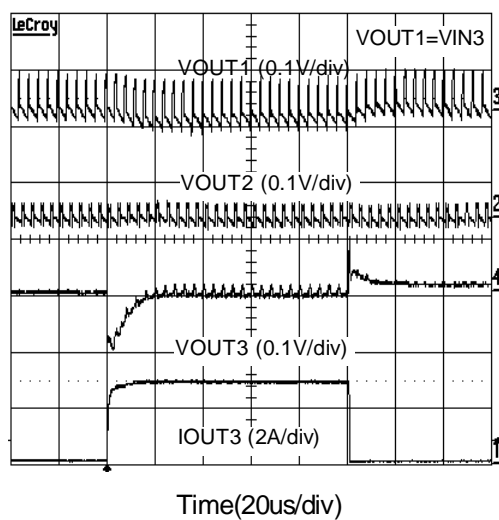


VOUT2 Load Transient

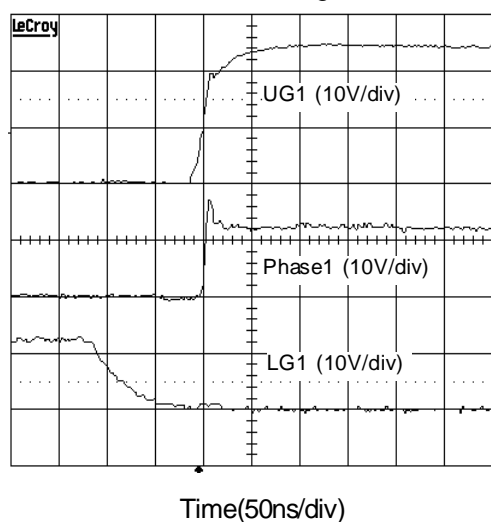


Typical Characteristics (Cont.)

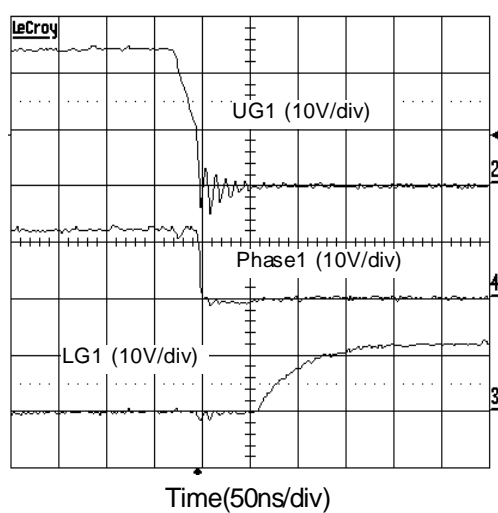
VOUT3 Load Transient



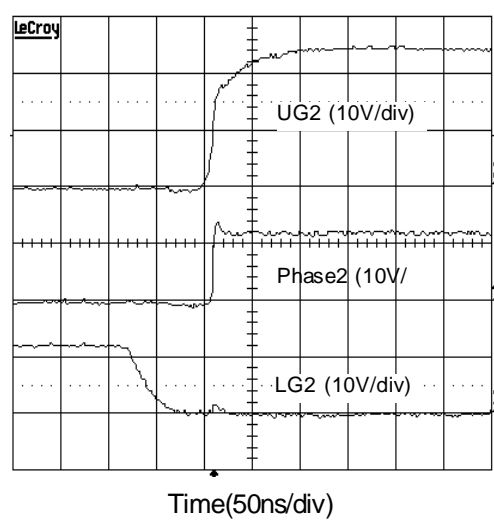
UG1 Rising



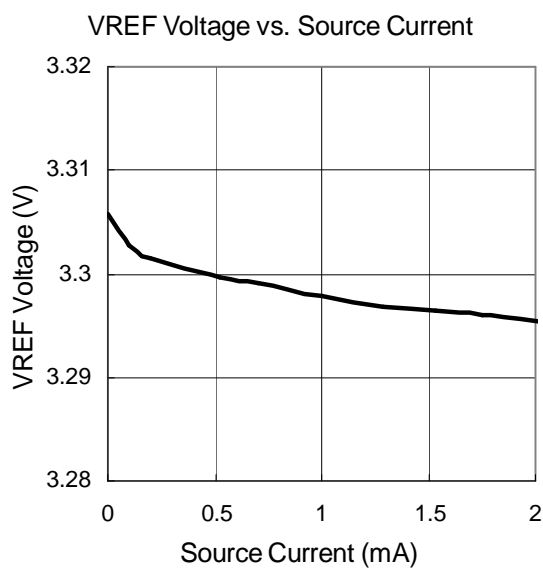
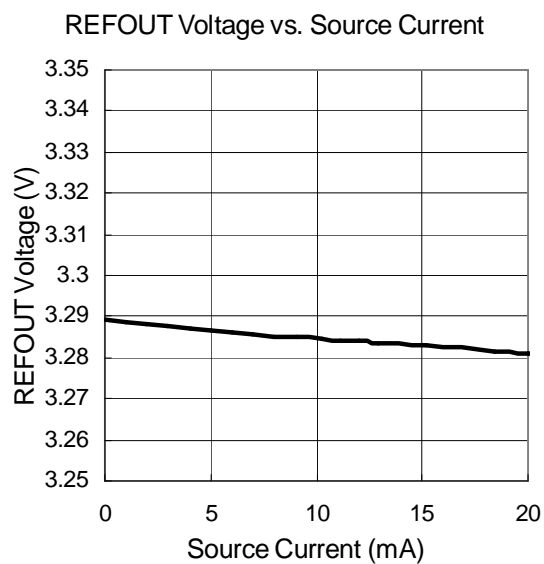
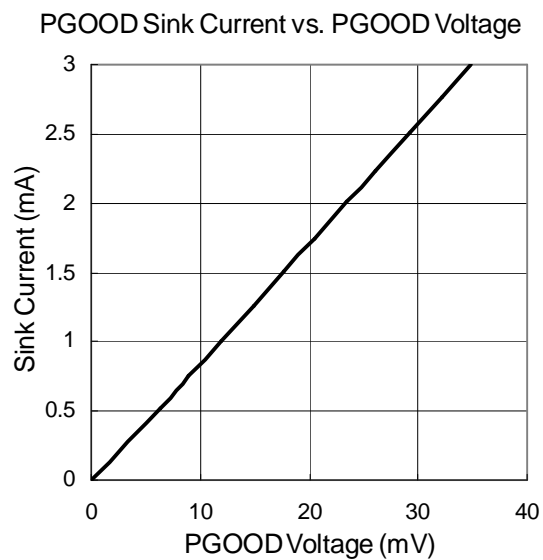
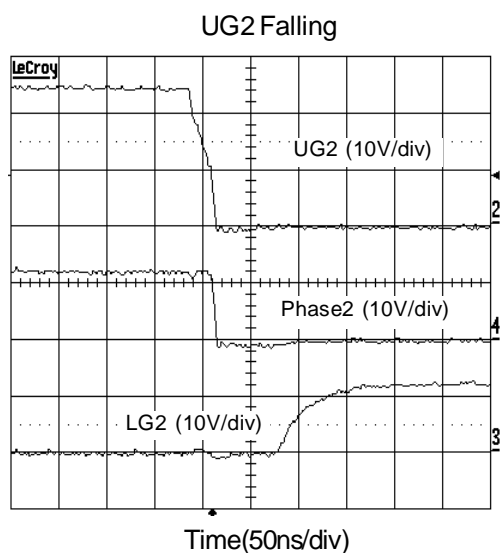
UG1 Falling



UG2 Rising

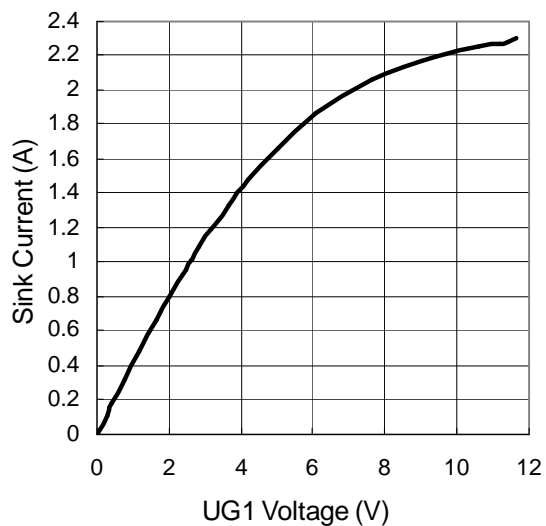


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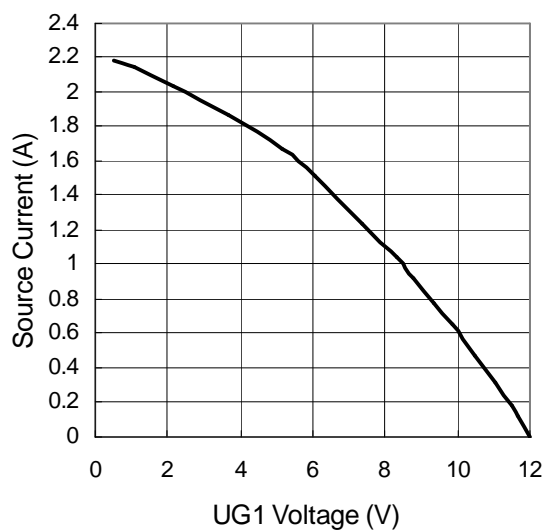


Typical Characteristics (Cont.)

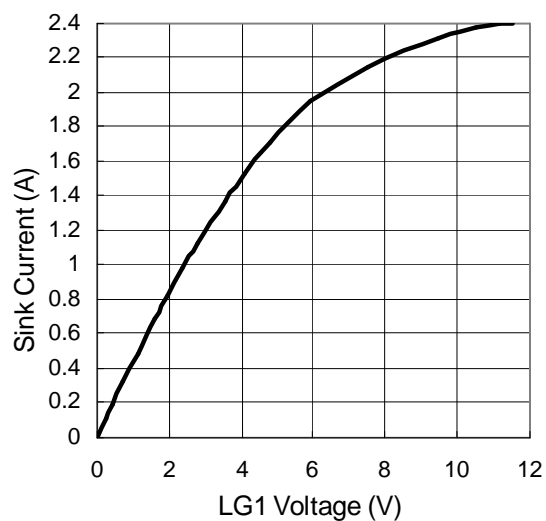
UG1 Sink Current vs. Voltage



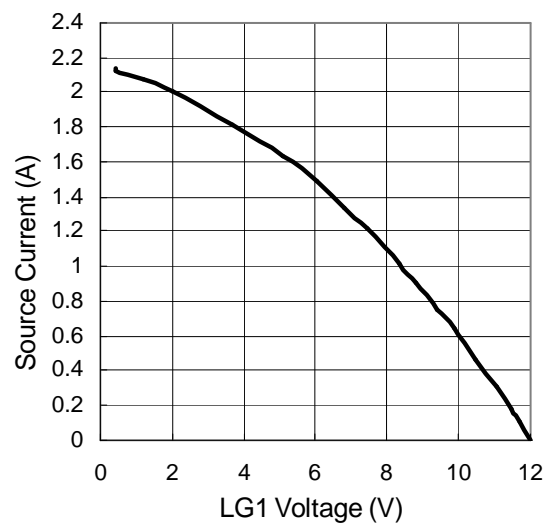
UG1 Source Current vs. Voltage



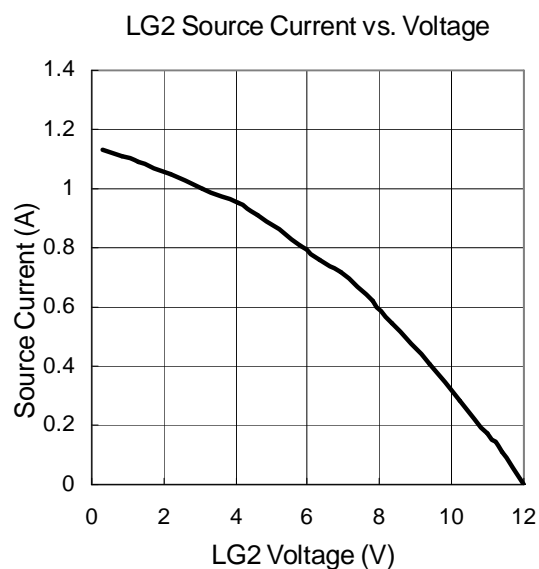
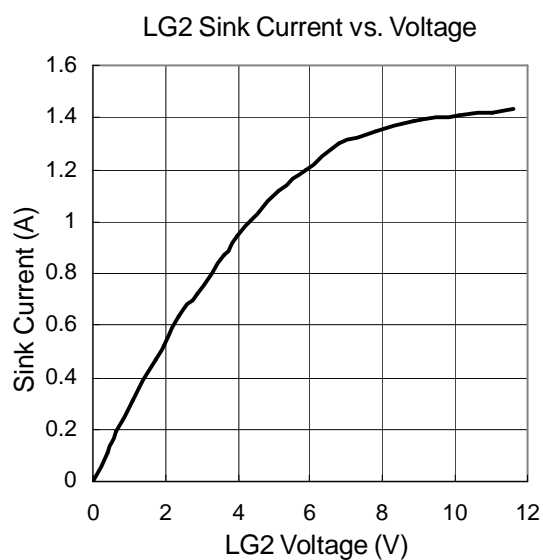
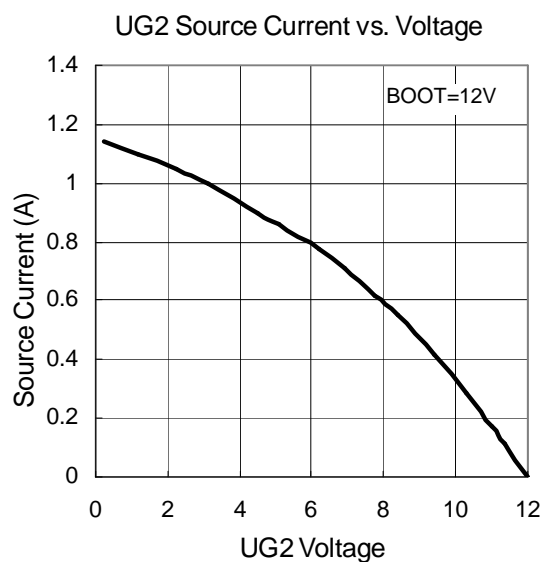
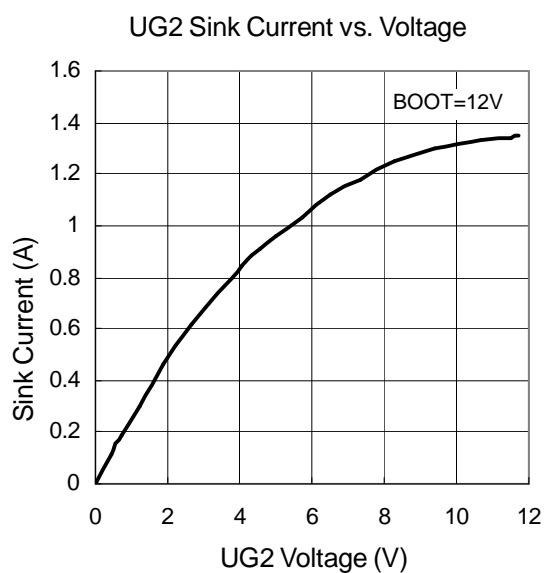
LG1 Sink Current vs. Voltage



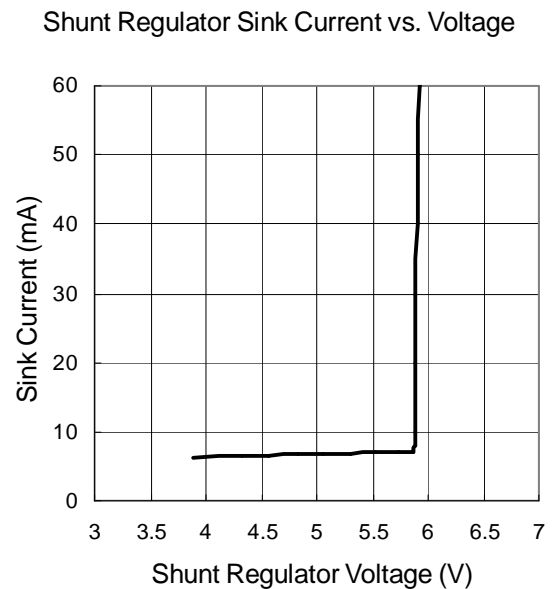
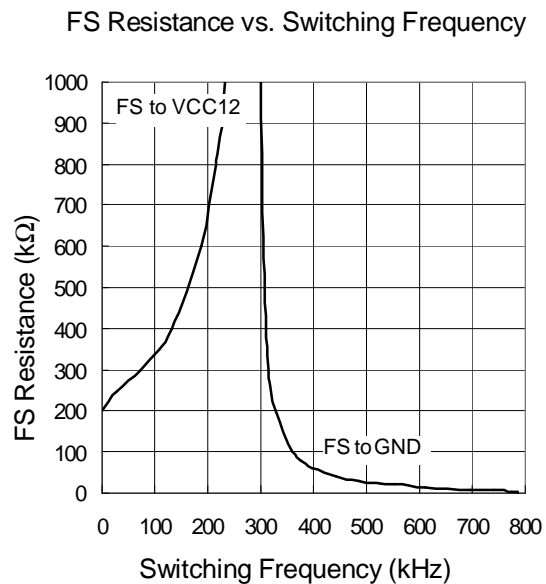
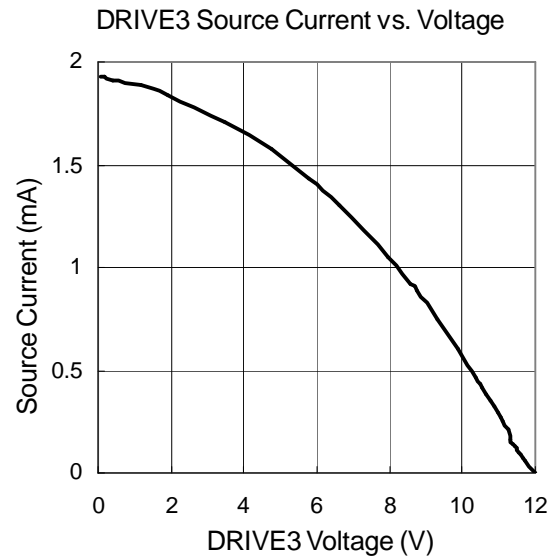
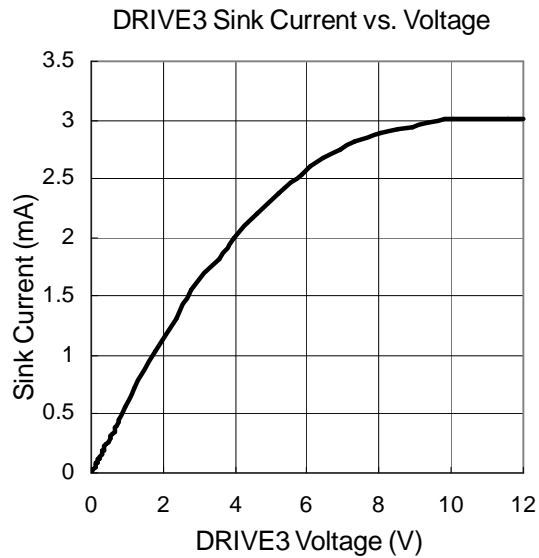
LG1 Source Current vs. Voltage



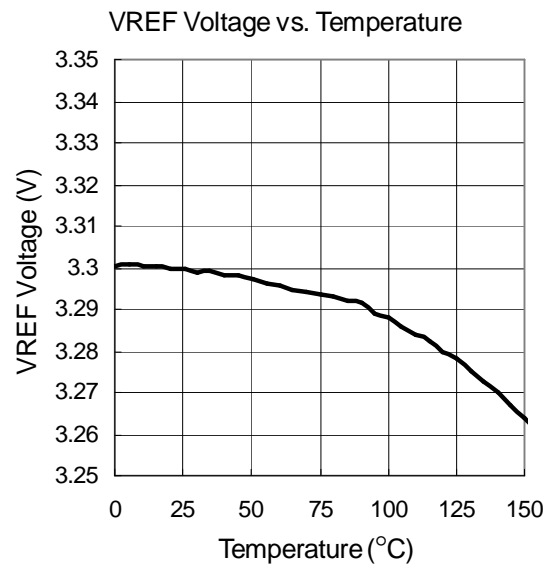
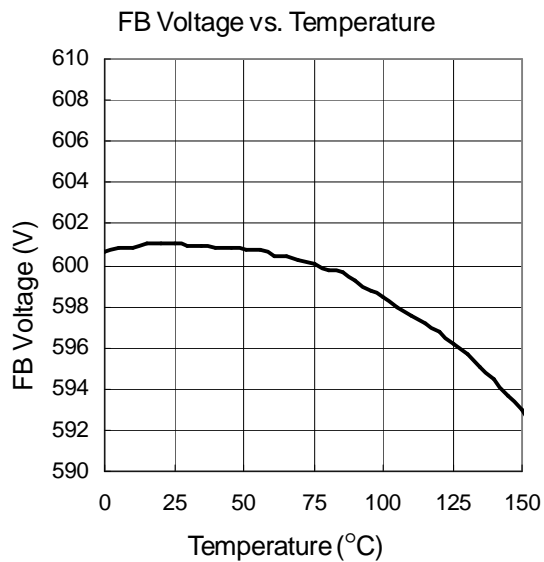
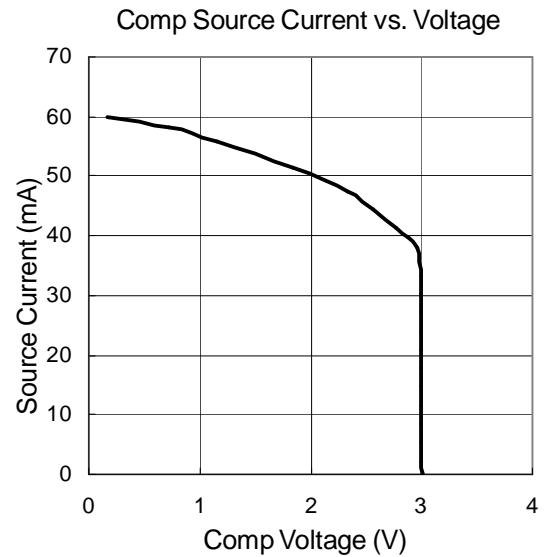
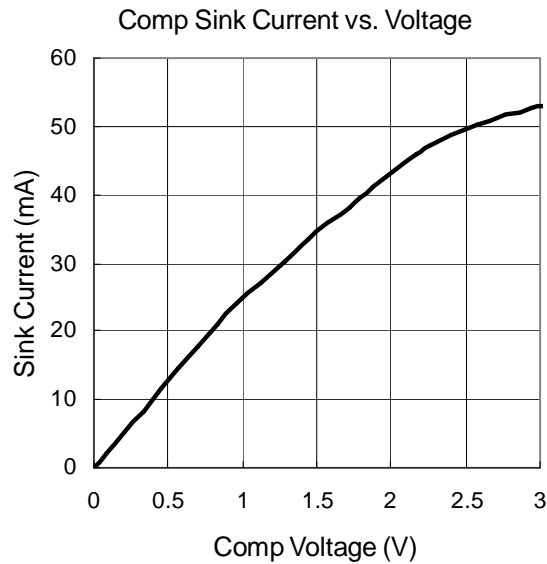
Typical Characteristics (Cont.)



Typical Characteristics (Cont.)



Typical Characteristics (Cont.)



Function Descriptions

Operational Modes

The APW7066 has two independent synchronous buck converters, and it also has DDR mode operation to allow VOUT2 to track VOUT1.

In independent mode operation, connect a capacitor from each SS/EN pin to the ground to set each regulator's soft-start time. The 3.3V reference VREF can be used directly, or divided by two resistors for REFIN, since the VREF is controlled by the SS2/EN2.

DDR mode is chosen by connecting the SS2/EN2 pin to VCC(5V). In this mode, SS2/EN2 function will be disabled, SS1/EN1 is used to control soft start and enable both VOUT1 and VOUT2. The VOUT1 is used as the REFIN for the VOUT2, that makes VOUT2 to track VOUT1.

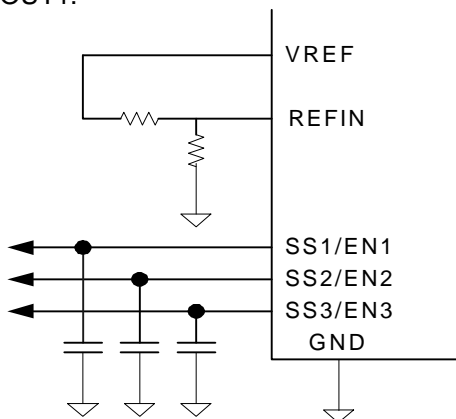


Figure 1. Independent Mode Circuit

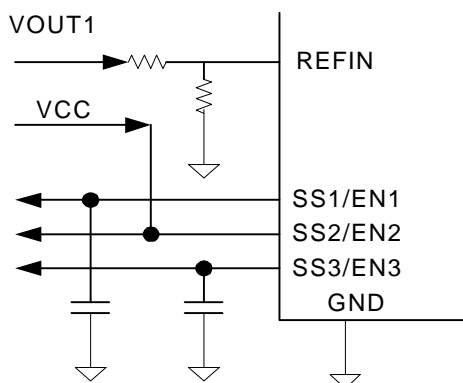


Figure 2. DDR Mode Circuit

Phase Shift

The APW7066 has phase shift function, use the REFOUT pin to select the phase shift between Independent mode and DDR mode. Connect the REFOUT to VCC to get the 0 degrees in either mode. In this case, the buffer of the REFOUT is disabled. Leave the REFOUT open shifts the phase 90 degrees in DDR mode, or 180 degrees in Independent mode, REFOUT can be used in this case (see Table 1.).

| MODE | SS2/EN2 | REFOUT | REFIN | PHASE SHIFT | CH1/CH2 |
|-------------|---------|--------|-------|-------------|------------------------------------|
| DDR | VCC | VCC | VOUT1 | 0 deg | SS1/EN1 for CH1 and CH2 |
| DDR | VCC | Open | VOUT1 | 90 deg | |
| Independent | SS2 cap | VCC | VREF | 0 deg | SS1/EN1 for CH1 SS2/EN2 for CH2 |
| Independent | SS2 cap | Open | VREF | 180 deg | |

Table1. Mode and Phase Selection

The advantage of Phase shift is to avoid overlapping the switching current spikes of the two channels, or interaction between the channels; it also reduces the RMS current of the input capacitors, allowing fewer caps to be employed. However, the phase shift between the rising edge of LGATE1 and LGATE2 (See figure 3.), depending on the duty cycles, the falling edges of the two channels might overlap; so the user should check it.

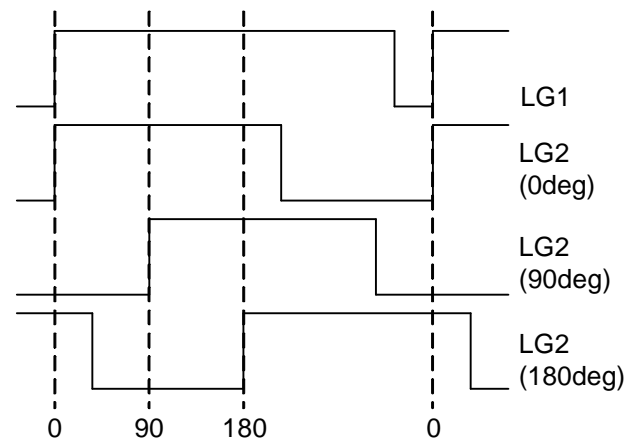


Figure 3. Phase of LG2 with respect to rising edge of LG1

Function Descriptions (Cont.)

Soft-Start/Enable

The three SS/EN pins control the soft-start and enable or disable the controller. In Independent mode, the three regulators all have independent soft-start and enable functions. Connect a soft-start capacitor from each SS/EN pin to the GND to set the soft-start interval, and an open drain logic signal for each SS/EN pin will enable or disable the respective output.

Figure 4. Shows the soft-start interval. When both VCC and VCC12 reach their Power-On-Reset threshold 4.23V and 7.8V, a 30uA current source starts to charge the capacitor. When the SS reaches the enabled threshold about 1V, the internal 0.6V reference starts to rise and follows the SS; the error amplifier output (COMP) suddenly raises to 1.1V, which is the valley of the oscillator's triangle wave, leads the VOUT to start up. Until the SS reaches about 3.0V, the internal reference completes the soft-start interval and reaches to 0.6V; then VOUT1 is in regulation. The SS1 still rises to 3.5V and then stops.

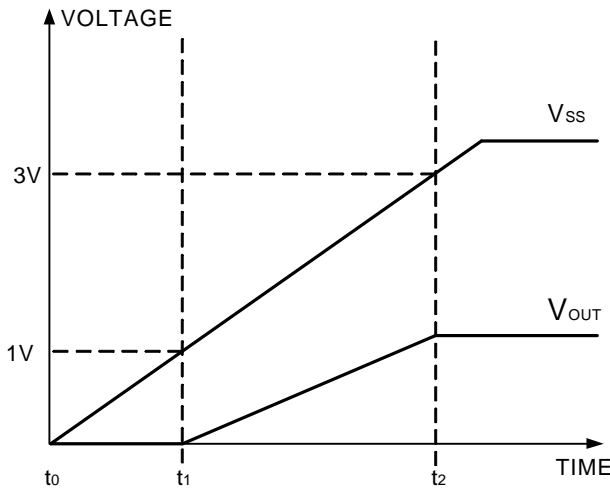


Figure 4. Soft-Start Interval

$$T_{\text{Soft-Start}} = t_2 - t_1 = \frac{C_{\text{SS}}}{I_{\text{SS}}} \cdot 2V$$

Where:

C_{SS} = external Soft-Start capacitor

I_{SS} = Soft-Start current = 30μA

PGOOD

The PGOOD output is an open-drain device, when the VCC is present; the gate of open-drain device will be high, forcing the PGOOD pin to go low. The three SS/EN pins and the SCP signals control the PGOOD signal (see block diagram), after the three SS/EN signals are over threshold high 3.3V and three outputs have no short-circuit, the PGOOD goes high to indicate all regulators are ready. If any of the SS/EN pins goes below threshold low 3.2V, the PGOOD will go low. Also, if any of the outputs has a short, the PGOOD pull low and if short-circuit condition continues for 1-2 clock pulses, all regulators will shut down. If the short-circuit is not long enough to shut down, it may still cause PGOOD to go low momentarily.

Because the PGOOD is an open-drain device, the typical range of the value to connect a pull high resistor to VCC will be 1kΩ to 10kΩ; if PGOOD is not used, leave it open.

Shunt Regulator

The APW7066 must have two power supplies VCC (5V) and VCC12 (12V) to drive the IC; VCC (5V) is for the control circuit and VCC12 (12V) is for the drivers of outputs. But it can also operate only VCC12, because the shunt regulator 5.8V was designed for VCC (5V); the range of the shunt regulator was designed over the usual range 4.5V to 5.5V of typical 5V power supplies.

Connect a resistor from VCC12 to VCC for shunt regulator and for the supply current. The input supply current of VCC is 7mA; minimum shunt regulator current is about 7mA, and therefore the 20mA shunt regulator current is enough; thus, the typical value, 300 of the resistor is recommended. The relation among minimum shunt regulator current, required shunt regulator current and supply current is:

Function Descriptions (Cont.)

PGOOD(Cont.)

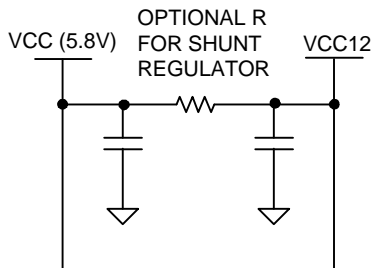
$$I_{SHUNT} = I_{CC} + I_{SHUNT(MIN)}$$

Where:

I_{SHUNT} = Required Shunt Regulator Current

I_{CC} = Supply Current

$I_{SHUNT(MIN)}$ = Minimum Shunt Regulator Current



Oscillator

The APW7066 provides the oscillator switching frequency adjustment. Connect a resistor from FS/SYNC pin to the ground, the nominally 300kHz oscillator switching frequency is increased according to the value of the resistor. The adjustment range of the switching frequency is 300kHz to 800kHz.

Conversely, connecting a resistor from FS/SYNC pin to the VCC12 reduces the switching frequency. The adjustment range of the switching frequency is 70kHz to 300kHz.

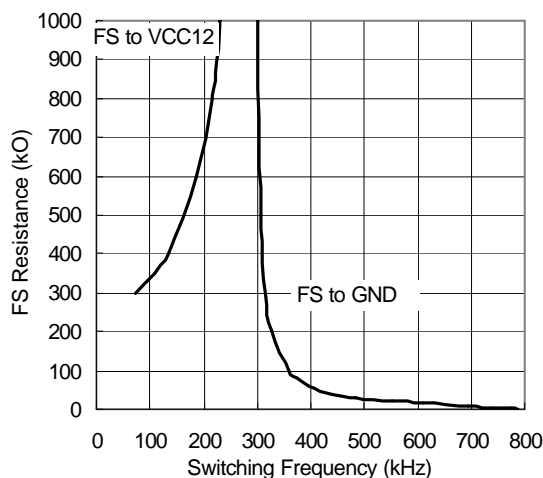


Figure 5. FS/SYNC Resistance vs. Frequency

SYNC

The switching frequency also can be synchronized to an external frequency. If there are two switching converters on the same board, taking the LGATE signal from another switching converter, go through a 10k resistor, and connecting to the FS/SYNC pin. The APW7066 will read another converter's frequency and after several milliseconds, the APW7066 will change to new frequency. If another converter's signal is lost, the APW7066 will return to internal oscillator. This allows the two switching converters for operating at the same frequency to avoid the interference from the independent frequencies between them. The acceptable frequency is a range of 150kHz to 800kHz.

Short-Circuit Protection

The APW7066 has a simple short-circuit protection to monitor COMP1 and COMP2 for VOUT1/2. When output voltage has a short, the FB pin should start to follow output, since it is a resistor divider from the output. The FB is the inverting input of Error-Amp, when FB pin is lower than the Error-Amp reference, then the COMP will rise to increase the duty-cycle of the upper MOSFET gate driver, this allows output to get higher voltage. If the short-circuit condition is long enough, the COMP pin will exceed the trip point 3.3V, and the duty circle will hit the maximum. This means that either Over-Current or Under-Voltage condition is detected. If any of the COMP1 and COMP2 exceeds their trip points, and holds over a filter time (1-2 clock cycle of switching frequency), then all regulators will shut down, and require a POR on either of VCC or VCC12 to restart. Note that the linear regulator has no short-circuit protection.

Application Information

Output Voltage Setting

The output voltage can be adjusted with a resistive divider, from output voltage to FB pin to the ground. Use 1% or better resistors for these resistor dividers is recommended. The reference voltages of VOUT1 and VOUT3 are 0.6V, the reference voltage of VOUT2 is REFIN voltage. The VREF voltage is for REFIN in independent mode. The following equations can be used to calculate the output voltage:

$$VOUT1 = \left(1 + \frac{R1}{R2}\right) \times 0.6V$$

$$VOUT2 = \left(1 + \frac{R1}{R2}\right) \times REFIN$$

$$VOUT3 = \left(1 + \frac{R1}{R2}\right) \times 0.6V$$

$$REFIN = \left(1 + \frac{R3}{R4}\right) \times VOUT1 \text{ (DDR Mode)}$$

$$REFIN = \left(1 + \frac{R3}{R4}\right) \times VREF \text{ (Independent Mode)}$$

Where:

R1 = resistor from VOUT to FB

R2 = resistor from FB to GND

R3 = resistor from VREF or VOUT1 to REFIN

R4 = resistor from REFIN to GND

Note that the R1 is part of the compensation. It should be conformed to the feedback compensation.

Linear Regulator Input/Output Capacitor Selection

The input capacitor is chosen based on its voltage rating. Under load transient condition, the input capacitor will momentarily supply the required transient current. The output capacitor for the linear regulator is chosen to minimize any droop during load transient condition. In addition, the capacitor is chosen based on its voltage rating.

Linear Regulator Input/Output MOSFET Selection

The maximum DRIVE3 voltage is determined by the VCC12. Since this pin drives an external N-channel MOSFET, therefore the maximum output voltage of the linear regulator is dependent upon the V_{GS} .

$$V_{OUT3MAX} = VCC12 - V_{GS}$$

Another criteria is its efficiency of heat removal. The power dissipated by the MOSFET is given by:

$$P_{diss} = I_{out} \times (V_{IN} - V_{OUT3})$$

where I_{out} is the maximum load current VOUT3 is the nominal output voltage

In some applications, heatsink might be required to help maintain the junction temperature of the MOSFET below its maximum rating.

Linear Regulator Compensation Selection

The linear regulator is stable over all load current. However, the transient response can be further enhanced by connecting a RC network between the FB3 and DRIVE3 pin. Depending on the output capacitance and load current of the application, the value of this RC network is then varied. A good starting point for the resistor value is 6.8kΩ and 470pF for the capacitor.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP, FB and VOUT should be added. The compensation network is shown in Fig. 9.

The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

Application Information (Cont.)

PWM Compensation (Cont.)

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

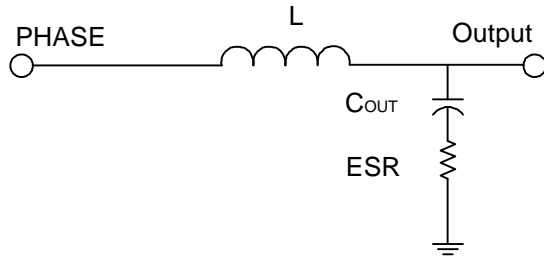


Figure 6. The Output LC Filter

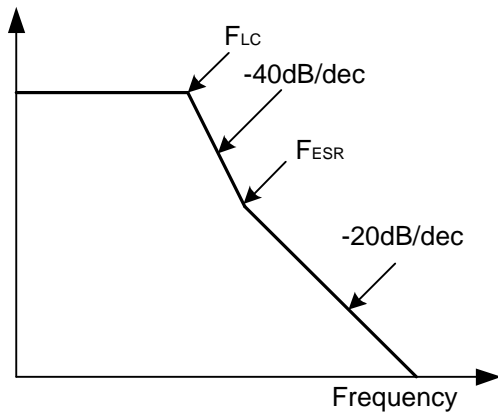


Figure 7. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure. 8. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

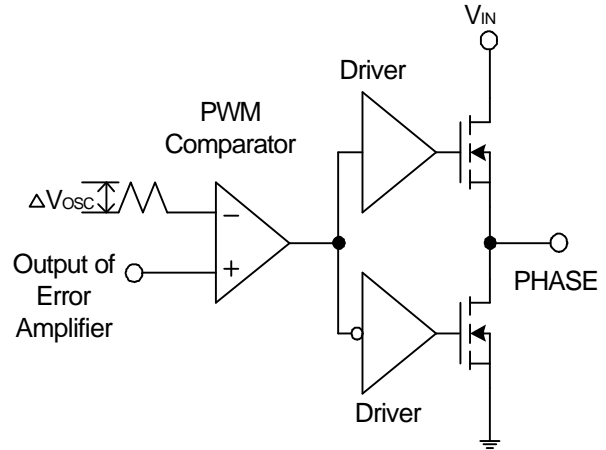


Figure 8. The PWM Modulator

The compensation circuit is shown in Figure 9. It provide a close loop transfer function with the highest zero crossover frequency and sufficient phase margin.

The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1} // \left(R2 + \frac{1}{sC2} \right)}{R1 // \left(R3 + \frac{1}{sC3} \right)}$$

$$= \frac{R1+R3}{R1 \times R3 \times C1} \times \frac{\left(s + \frac{1}{R2 \times C2} \right) \times \left(s + \frac{1}{(R1+R3) \times C3} \right)}{s \left(s + \frac{C1+C2}{R2 \times C1 \times C2} \right) \times \left(s + \frac{1}{R3 \times C3} \right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R1+R3) \times C3}$$

$$F_{P1} = \frac{1}{2 \times \pi \times R2 \times \left(\frac{C1 \times C2}{C1 + C2} \right)}$$

$$F_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

Application Information (Cont.)

PWM Compensation (Cont.)

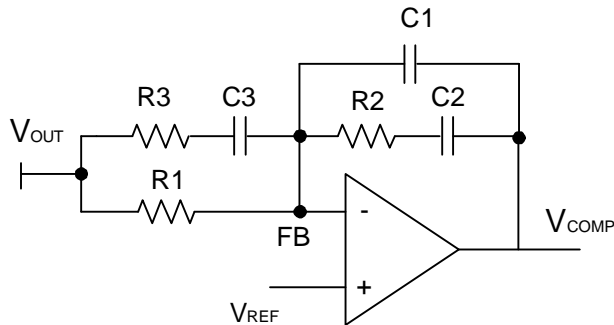


Figure 9. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times GAIN_{AMP}$$

Figure 10. shows the asymptotic plot of the closed loop converter gain and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency F_o :
 $(1/5 \sim 1/10) \times F_s > F_o > F_{ESR}$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_o}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC} .

$$F_{Z1} = 0.75 \times F_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR} :

$$F_{P1} = F_{ESR}$$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at half the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC} . The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

$$F_{P2} = 0.5 \times F_o$$

$$F_{Z2} = F_{LC}$$

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_s}{F_o} - 1} \quad C3 = \frac{1}{\pi \times R3 \times F_s}$$

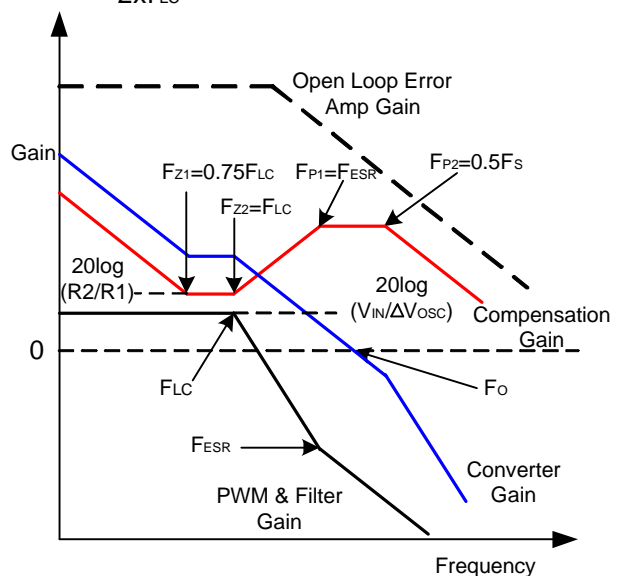


Figure 10. Converter Gain & Frequency

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_s \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

Application Information (Cont.)

Output Inductor Selection (Cont.)

where F_s is the switching frequency of the regulator. Although increase the inductor value and frequency reduce the ripple current and voltage, but there is a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_s) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher Capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore select high performance low ESR capacitors that are intended for switching regulator applications. In some applications, multiple capacitors have to be parallel to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage

rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1uF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following :

$$P_{UPPER} = I_{OUT} (1 + TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_s$$

$$P_{LOWER} = I_{OUT} (1 + TC)(R_{DS(ON)})(1-D)$$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_s is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching interval, t_{SW} , is a function of the reverse transfer capacitance C_{RSS} .

The $(1+TC)$ term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the " $R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Application Information (Cont.)

Connecting One Input from Another Output

It can be connected one of the 3 outputs as the input voltage to the 2nd. In these cases the output current of the first output includes its own load current and the 2nd output's load current. Therefore, the components of the first output must be designed and sized for the both outputs. The soft-start of first output must be faster than the 2nd output. If the first output is not present when the 2nd output tries to start up, the 2nd output cannot get smooth and controlled output voltage rise, even cause short-circuit protection.

Short Circuit Protection

The APW7066 provides a simple short circuit protection function, and it is not easy to predict its performance, since many factors can affect how well it works. Therefore, the limitations and suggestions of this method must be provided for users to understand how to work it well.

- The short circuit protection was not designed to work for the output in initial short condition. In this case, the short circuit protection may not work, and damage the MOSFETs. If the circuit still works, remove the short can cause an inductive kick on the phase pin, and it may damage the IC and MOSFETs.
- If the resistance of the short is not low enough to cause protection, the regulator will work as the load has increased, and continue to regulate up until the MOSFETs is damaged. The resistance of the short should include wiring, PCB traces, contact resistances, and all of the return paths.
- The higher duty cycle will give a higher COMP voltage level, and it is easy to touch the trip point. The compensation components also affect the response of COMP voltage; smaller caps may give a faster response.
- The output current has faster rising time during

short; the COMP pin will have a sharp rise. However, if the current rises too fast, it may cause a false trip. The output capacitance and its ESR can affect the rising time of the current during short.

Layout Considerations

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 10. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout :

- The metal plate of the bottom of the packages (TSSOP-24 and QFN-32) must be soldered to the PCB and connected to the GND plane on the backside through several thermal vias.
- Keep the switching nodes (UGATE, LGATE and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UG1, LG1, UG2, LG2, DRIVE3) should be short and wide.
- Decoupling capacitor, compensation component, the resistor dividers, boot capacitors, and SS capacitors should be close their pins.
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (VIN and phase nodes) should be a large plane for heat sinking.

Application Information (Cont.)

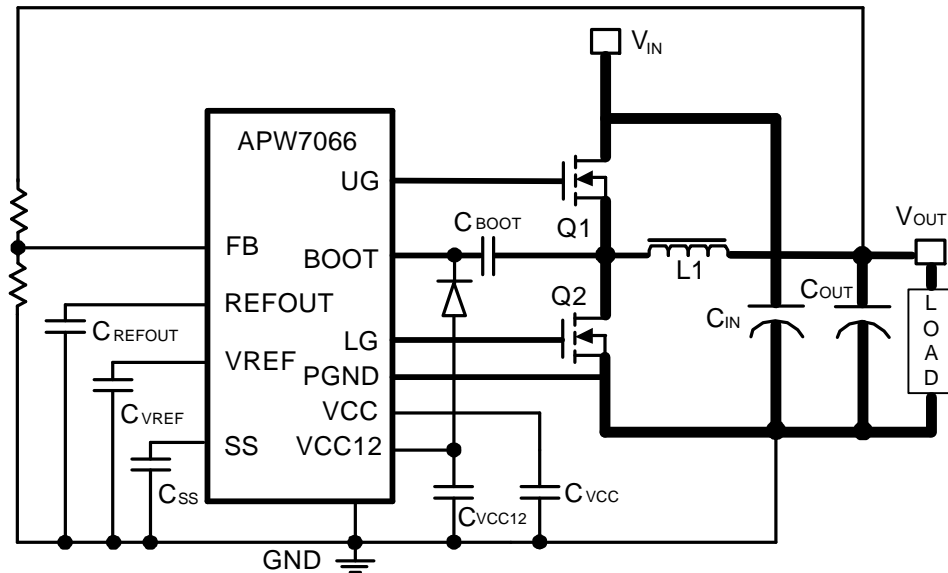
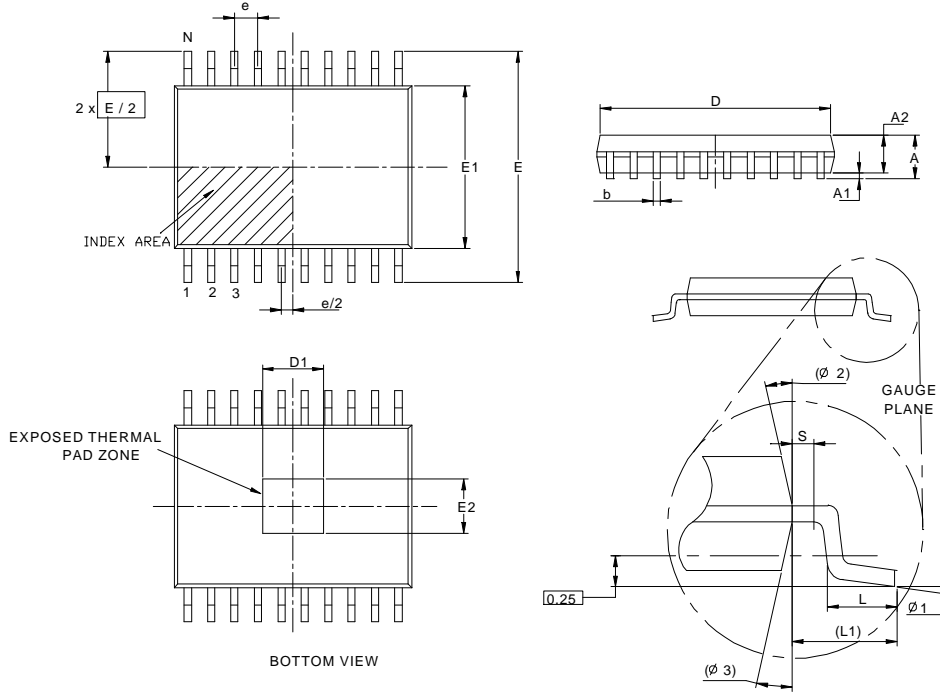


Figure 11. Layout Guidelines

Packaging Information

TSSOP/ TSSOP-P (Reference JEDEC Registration MO-153)

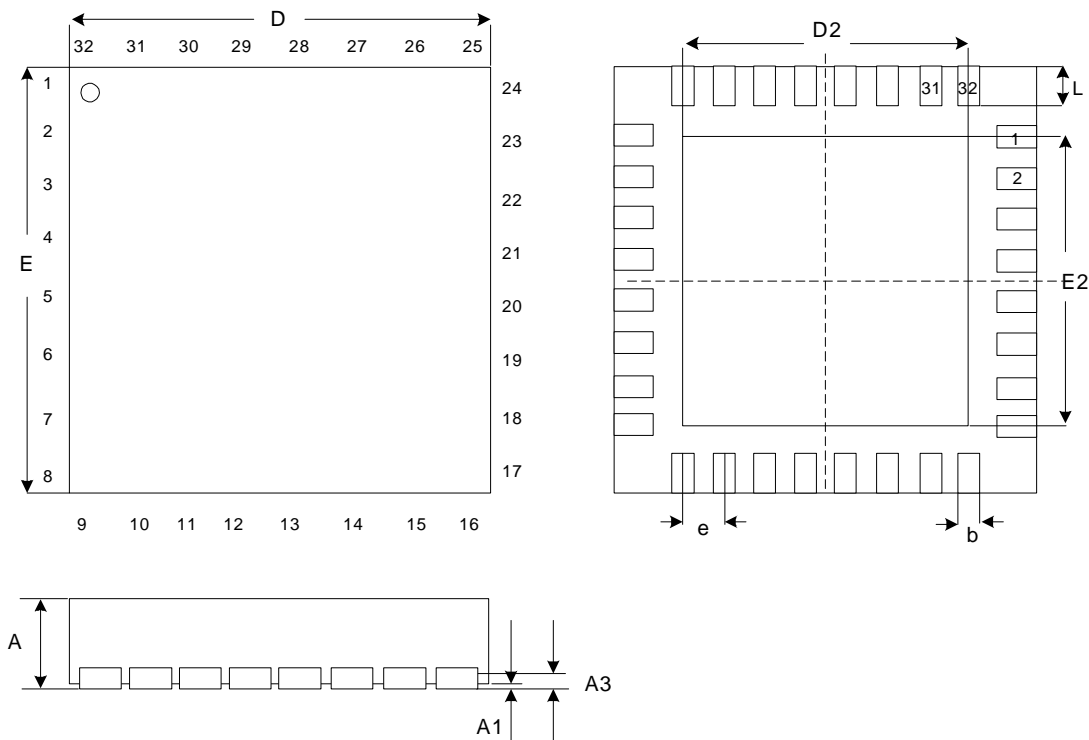


(THERMALLY ENHANCED VARIATIONS ONLY)

| Dim | Millimeters | | Inches | |
|-----|-------------------|---------------|---------------------|-----------------|
| | Min. | Max. | Min. | Max. |
| A | | 1.2 | | 0.047 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| A2 | 0.80 | 1.05 | 0.031 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| D | 6.4 (N=20PIN) | 6.6 (N=20PIN) | 0.252 (N=20PIN) | 0.260 (N=20PIN) |
| | 7.7 (N=24PIN) | 7.9 (N=24PIN) | 0.303 (N=24PIN) | 0.311 (N=24PIN) |
| | 9.6 (N=28PIN) | 9.8 (N=28PIN) | 0.378 (N=28PIN) | 0.386 (N=28PIN) |
| D1 | 4.2 BSC (N=20PIN) | | 0.165 BSC (N=20PIN) | |
| | 4.7 BSC (N=24PIN) | | 0.188 BSC (N=24PIN) | |
| | 3.8 BSC (N=28PIN) | | 0.150 BSC (N=28PIN) | |
| e | 0.65 BSC | | 0.026 BSC | |
| E | 6.40 BSC | | 0.252 BSC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| E2 | 3.0 BSC (N=20PIN) | | 0.118 BSC (N=20PIN) | |
| | 3.2 BSC (N=24PIN) | | 0.127 BSC (N=24PIN) | |
| | 2.8 BSC (N=28PIN) | | 0.110 BSC (N=28PIN) | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| L1 | 1.0 REF | | 0.039 REF | |
| R | 0.09 | | 0.004 | |
| R1 | 0.09 | | 0.004 | |
| S | 0.2 | | 0.008 | |
| ø1 | 0° | 8° | 0° | 8° |
| ø2 | 12° REF | | 12° REF | |
| ø3 | 12° REF | | 12° REF | |

Packaging Information

QFN-32

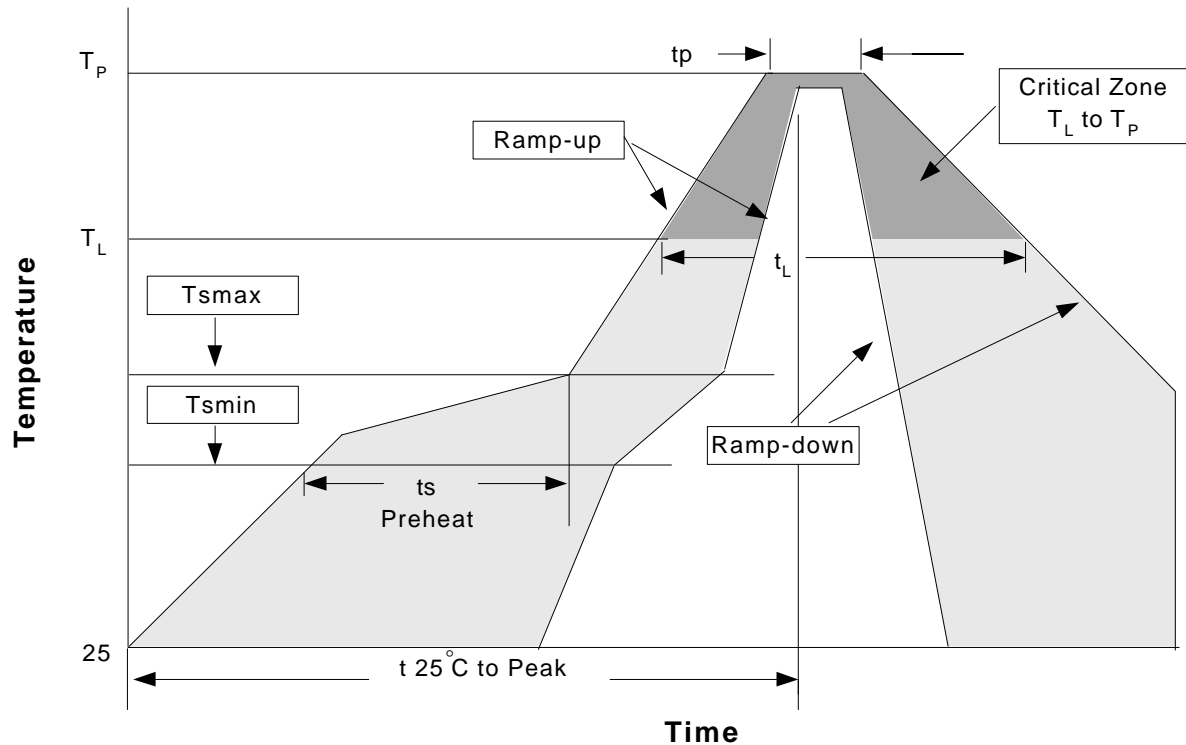


| Dim | Millimeters | | Inches | |
|-----|-------------|------|------------|--------|
| | Min. | Max. | Min. | Max. |
| A | - | 0.84 | - | 0.033 |
| A1 | 0.00 | 0.04 | 0.00 | 0.0015 |
| A3 | 0.20 REF. | | 0.008 REF. | |
| D | 4.90 | 5.10 | 0.192 | 0.200 |
| E | 4.90 | 5.10 | 0.192 | 0.200 |
| b | 0.18 | 0.28 | 0.007 | 0.011 |
| D2 | 3.50 | 3.60 | 0.138 | 0.142 |
| E2 | 3.50 | 3.60 | 0.138 | 0.142 |
| e | 0.500 BSC | | 0.020 BSC | |
| L | 0.35 | 0.45 | 0.014 | 0.018 |

Physical Specifications

| | |
|--------------------|--|
| Terminal Material | Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn |
| Lead Solderability | Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3. |

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|--|-------------------------|------------------|
| Average ramp-up rate (T _L to T _P) | 3°C/second max. | 3°C/second max. |
| Preheat | | |
| - Temperature Min (T _{min}) | 100°C | 150°C |
| - Temperature Max (T _{max}) | 150°C | 200°C |
| - Time (min to max) (ts) | 60-120 seconds | 60-180 seconds |
| Time maintained above: | | |
| - Temperature (T _L) | 183°C | 217°C |
| - Time (t _L) | 60-150 seconds | 60-150 seconds |
| Peak/Classification Temperature (T _P) | See table 1 | See table 2 |
| Time within 5°C of actual Peak Temperature (tp) | 10-30 seconds | 20-40 seconds |
| Ramp-down Rate | 6°C/second max. | 6°C/second max. |
| Time 25°C to Peak Temperature | 6 minutes max. | 8 minutes max. |

Notes: All temperatures refer to topside of the package .Measured on the body surface.

(mm)

Classification Reflow Profiles(Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

| Package Thickness | Volume mm ³ <350 | Volume mm ³ ≥350 |
|-------------------|--------------------------------|--------------------------------|
| <2.5 mm | 240 +0/-5°C | 225 +0/-5°C |
| ≥2.5 mm | 225 +0/-5°C | 225 +0/-5°C |

Table 2. Pb-free Process – Package Classification Reflow Temperatures

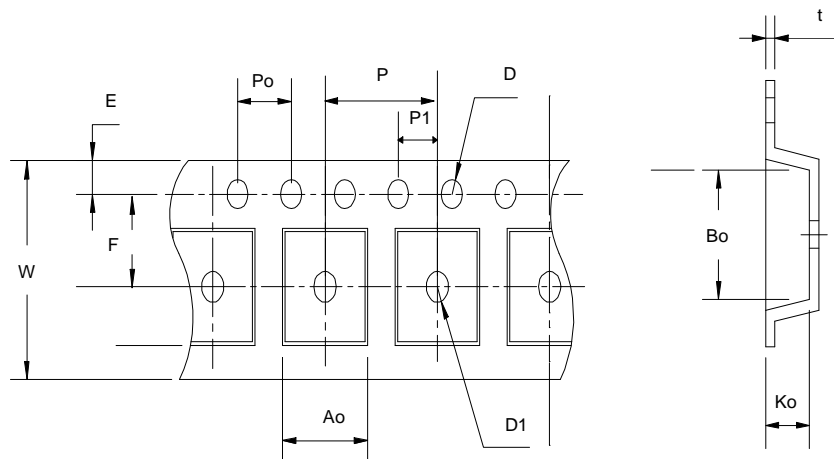
| Package Thickness | Volume mm ³ <350 | Volume mm ³ 350-2000 | Volume mm ³ >2000 |
|-------------------|--------------------------------|------------------------------------|---------------------------------|
| <1.6 mm | 260 +0°C* | 260 +0°C* | 260 +0°C* |
| 1.6 mm – 2.5 mm | 260 +0°C* | 250 +0°C* | 245 +0°C* |
| ≥2.5 mm | 250 +0°C* | 245 +0°C* | 245 +0°C* |

*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

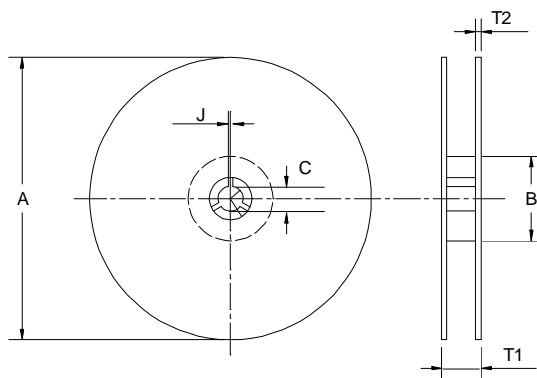
Reliability Test Program

| Test item | Method | Description |
|---------------|---------------------|-------------------------------|
| SOLDERABILITY | MIL-STD-883D-2003 | 245°C, 5 SEC |
| HOLT | MIL-STD-883D-1005.7 | 1000 Hrs Bias @125°C |
| PCT | JESD-22-B,A102 | 168 Hrs, 100%RH, 121°C |
| TST | MIL-STD-883D-1011.9 | -65°C~150°C, 200 Cycles |
| ESD | MIL-STD-883D-3015.7 | VHBM > 2KV, VMM > 200V |
| Latch-Up | JESD 78 | 10ms, 1 _{tr} > 100mA |

Carrier Tape & Reel Dimensions



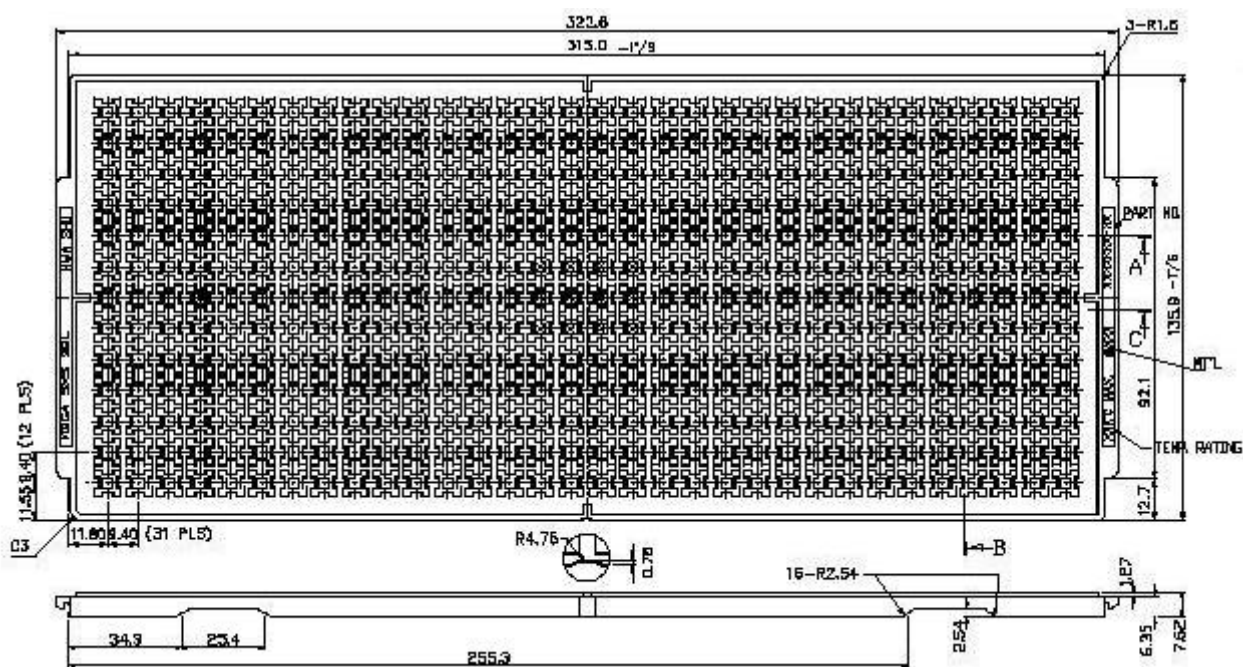
Carrier Tape & Reel Dimensions(Cont.)



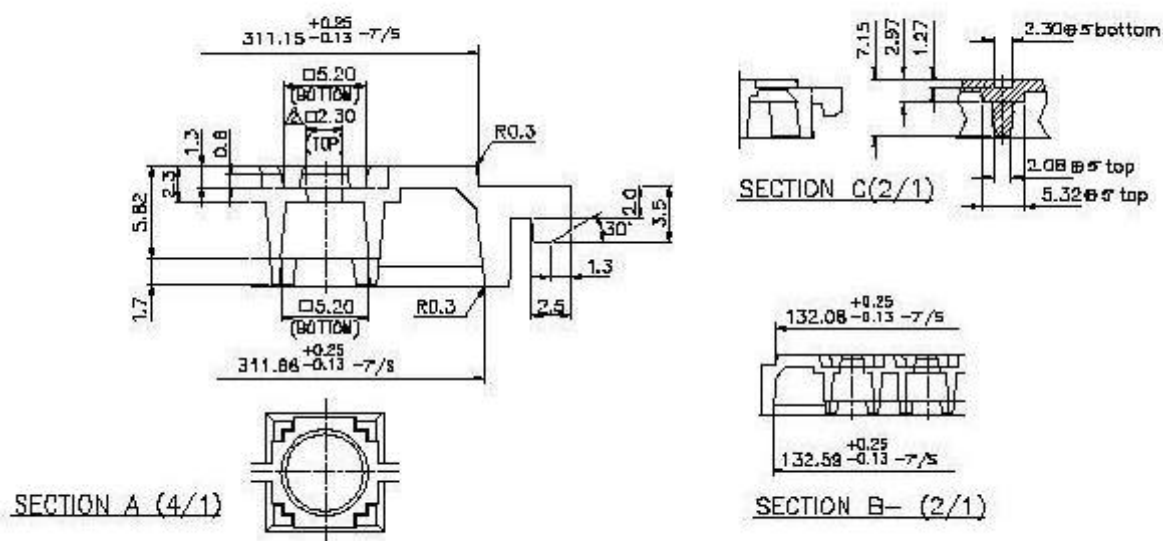
| Application | A | B | C | J | T1 | T2 | W | P | E |
|-------------|----------|----------|---------|----------|-----------|----------|----------|----------|----------|
| TSSOP- 24 | 330 ±1 | 100 ref | 13 ±0.5 | 2 ±0.5 | 16.4 ±0.2 | 2 ±0.2 | 16 ±0.3 | 12 ±0.1 | 1.75±0.1 |
| | F | D | D1 | Po | P1 | Ao | Bo | Ko | t |
| | 7.5 ±0.1 | 1.5 +0.1 | 1.5 min | 4.0 ±0.1 | 2.0 ±0.1 | 6.9 ±0.1 | 8.3 ±0.1 | 1.5 ±0.1 | 0.3±0.05 |

(mm)

5x5 Shipping Tray



5x5 Shipping Tray(Cont.)



Cover Tape Dimensions

| Application | Carrier Width | Cover Tape Width | Devices Per Reel |
|-------------|---------------|------------------|------------------|
| TSSOP- 24 | 16 | 21.3 | 2000 |

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