TNY256

TinySwitch® Plus

Energy Efficient, Low Power Off-line Switcher

Product Highlights

TinySwitch Plus Features

- Extended power range
- Fully integrated auto-restart reduces short circuit current
- Line under-voltage sense eliminates turn-off glitches
- Frequency jittering dramatically reduces EMI (5 to 10 dB)
- TO-220 package option

Lowest Cost, Low Power Switcher Solution

- Lower cost than RCC, discrete PWM and other integrated/hybrid solutions
- Cost effective replacement for bulky linear adapters
- Lowest component count
- Simple ON/OFF control – no loop compensation components
- No bias winding – simpler, lower cost transformer
- Designed to work with low cost external components

Extremely Energy Efficient

- Consumes only 30/60 mW at 115/230 VAC with no load
- Meets Blue Angel, Energy Star, Energy 2000 and 200mW European cell phone requirements for standby
- Saves $1 to $4 per year in energy costs (at $0.12/kWHr) compared to bulky linear adapters
- Ideal for cellular phone chargers and adapters

High Performance at Low Cost

- High voltage powered – ideal for charger applications
- High bandwidth provides fast turn on with no overshoot
- Current limit operation rejects line frequency ripple
- Built-in current limit and thermal protection

Description

The TNY256 extends the power range of the *TinySwitch* family of energy efficient, low power off-line switchers. *TinySwitch* devices use a breakthrough design to provide the lowest cost, high efficiency, off-line switching solution for low power applications. They integrate a 700 V power MOSFET, oscillator, high voltage switched current source, current limit and thermal shutdown circuitry into a single, monolithic device. The devices start-up and operate on power derived from the DRAIN voltage, eliminating the need for a transformer bias winding and associated circuitry. *TinySwitch's* low operating current allows power supply no-load consumption to be kept under 100 mW, even at 265 VAC input.

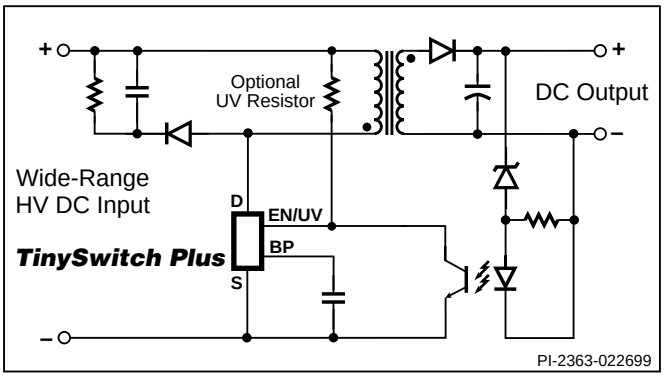


Figure 1. Typical Standby Application.

OUTPUT POWER CAPABILITY*			
ORDER PART NUMBER	**PACKAGE**	**230 VAC or 115 VAC w/Doubler**	**85-265 VAC**
TNY256P	DIP-8	8-15 W	5-10 W
TNY256G	SMD-8		
TNY256Y	TO-220-7B	8-19 W	5-11 W

*Table 1. * The low end of the power ranges shown represent enclosed adapters with minimal heat sinking whereas, the high end of the power ranges represent open frame power supplies with adequate heat sinking, both measured at an ambient of 50 °C. Please refer to the Key Application Considerations section for more details.*

The *TinySwitch Plus* incorporates auto-restart, line under-voltage sense, and frequency jittering features. The auto-restart circuit safely limits output power during fault conditions such as output short or open loop. The auto-restart circuit is fully integrated and does not require external timing components. The line under-voltage sense threshold can be externally programmed using a line sense resistor. During start-up, this feature keeps the TNY256 off until the input line voltage reaches the under-voltage threshold. When the input line voltage is removed, the line under-voltage circuit prevents auto-restart attempts after the output goes out of regulation. This eliminates power down glitches caused by the slow discharge of input storage capacitors present in applications such as standby supplies. A single resistor is used to implement this feature, eliminating what normally takes five to six components. The line sense resistor is optional. The TNY256 operating frequency of 130 kHz is jittered (frequency modulated) to reduce both quasi-peak and average EMI, minimizing filtering costs.

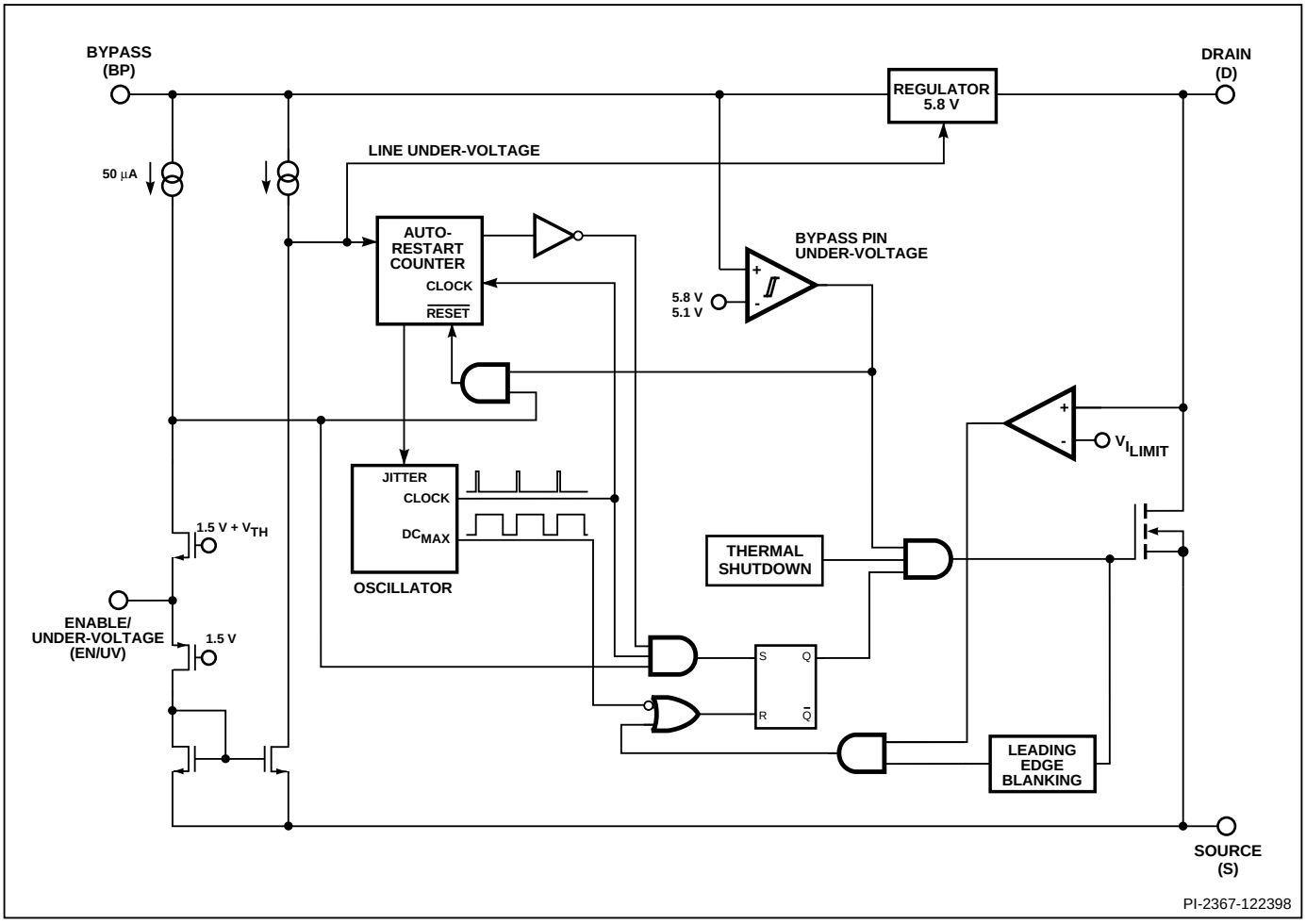


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. Provides internal operating current for both start-up and steady-state operation.

BYPASS (BP) Pin:
Connection point for a 0.1 µF external bypass capacitor for the internally generated 5.8 V supply.

ENABLE/UNDER-VOLTAGE (EN/UV) Pin:
This pin has dual functions, enable input and line under-voltage sense. During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than 50 µA is drawn out of this pin. This pin also senses line under-voltage conditions through an external resistor connected to the DC line voltage. If there is no external resistor connected to this pin, TNY256 detects this and disables the line under-voltage function.

SOURCE (S) Pin:
Power MOSFET source connection. Primary return.

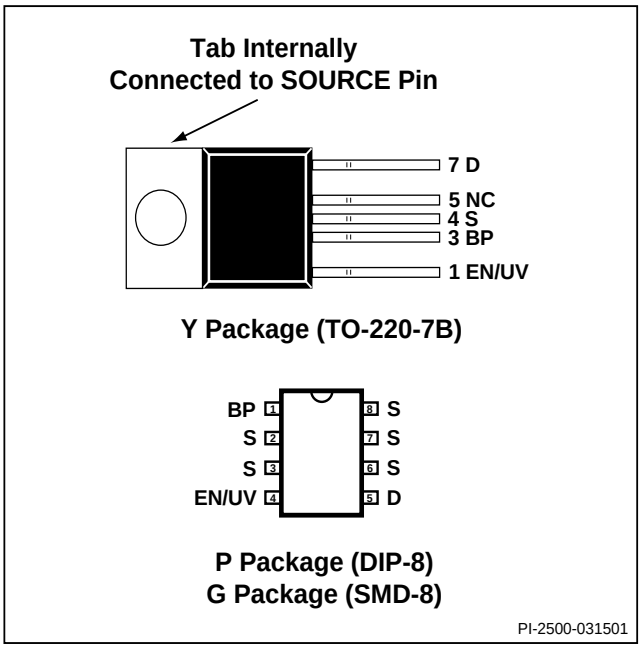


Figure 3. Pin Configuration.

NO CONNECT (N) Pin
No connection.

TinySwitch Functional Description

TinySwitch combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (Pulse Width Modulator) controllers, *TinySwitch* uses a simple ON/OFF control to regulate the output voltage.

The TNY256 controller consists of an Oscillator, Enable (Sense and Logic) circuit, 5.8 V Regulator, Bypass pin Under-Voltage circuit, Over Temperature Protection, Current Limit circuit, Leading Edge Blanking and a 700 V power MOSFET. The TNY256 incorporates additional circuitry for Line Under-Voltage Sense, Auto-Restart and Frequency Jitter. Figure 2 shows the functional block diagram with the most important features.

Oscillator
The typical oscillator frequency is internally set to an average of 130 kHz. Two signals are generated from the oscillator, the Maximum Duty Cycle signal (DC_{MAX}) and the Clock signal that indicates the beginning of each cycle.

The TNY256 oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 5 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter (1 kHz) is set to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure4 illustrates the frequency jitter of the TNY256.

Enable Input Circuit
The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.5 V. The current through the source follower is limited to 50 µA with 10 µA of hysteresis. When the current drawn out of the this pin exceeds

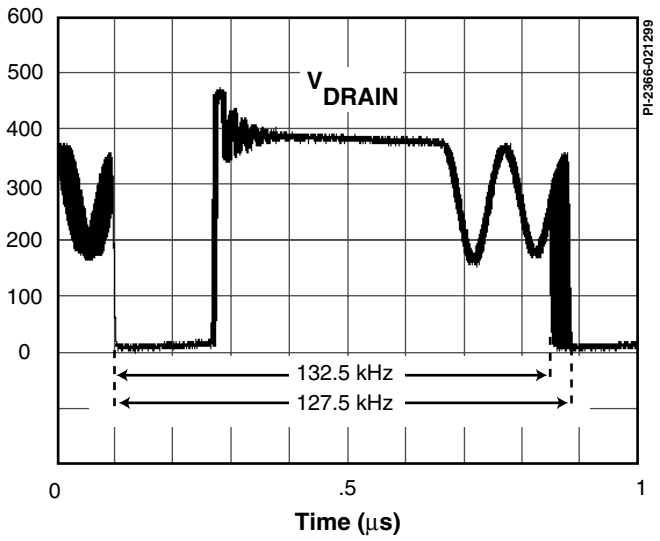


Figure 4. Frequency Jitter.

50 µA, a low logic level (disable) is generated at the output of the enable circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored.

Under most operating conditions (except when close to no-load), the low impedance of the source follower, keeps the voltage on the EN/UV pin from going much below 1.5 V, in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

5.8 V Regulator
The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node for the *TinySwitch*. When the MOSFET is on, the *TinySwitch* runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the *TinySwitch* to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency de-coupling and energy storage.

BYPASS Pin Under-Voltage
The BYPASS pin under-voltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 5.1 V. Once the BYPASS pin voltage drops below 5.1 V, it must rise back to 5.8 V to enable (turn-on) the power MOSFET.

Over Temperature Protection
The thermal shutdown circuitry senses the die temperature. The threshold is set at 135 °C with 70 °C hysteresis. When the die temperature rises above this threshold (135 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 70 °C, at which point it is re-enabled.

Current Limit
The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by primary-side capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

Auto-Restart
In the event of a fault condition such as output overload, output

short, or an open loop condition, TNY256 enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the EN/UV pin is pulled low. If the EN/UV pin is not pulled low for 32 ms, the power MOSFET switching is disabled for 128 ms (except in the case of line under-voltage condition). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 5 illustrates auto-restart circuit operation in the presence of a temporary output short.

In the event of line under-voltage condition, the switching of the power MOSFET is disabled beyond its normal 128 ms time until the line under-voltage condition goes away.

Line Under-Voltage (UVLO) Sense Circuit

The DC line voltage can be monitored by connecting an external resistor from the DC line to the EN/UV pin. During power-up or when the switching of the power MOSFET is disabled in auto-restart, the current into the EN/UV pin must exceed 50 µA to initiate switching of the power MOSFET. During power-up, this is implemented by holding the BYPASS pin to 5.1 V while the line under-voltage condition exists. The BYPASS pin then rises from 5.1 V to 5.8V when the line under-voltage condition goes away. When the switching of the power MOSFET is disabled in auto-restart mode and the line under-voltage condition exists, the counter is stopped. This stretches the disable time beyond its normal 128ms until the line under-voltage condition goes away.

The line under-voltage circuit also detects when there is no external resistor connected to the EN/UV pin. In this case the line under-voltage function is disabled.

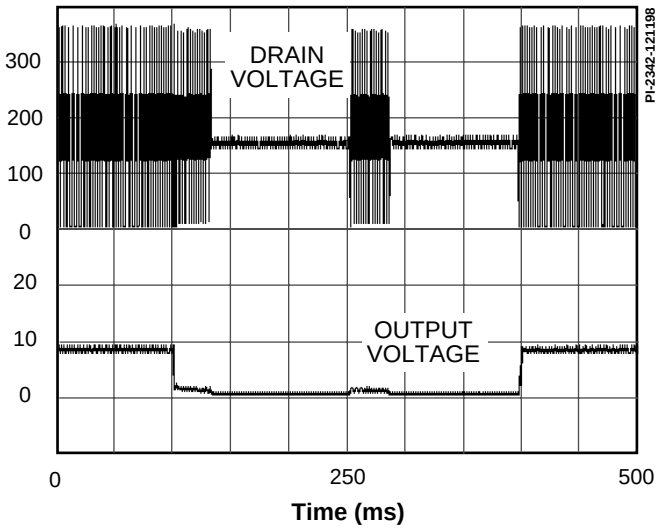


Figure 5. TNY256 Auto-Restart Operation.

TinySwitch Operation

TinySwitch devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit. The maximum on-time of the MOSFET is limited to DC_{MAX} by the oscillator. Since the current limit and frequency of the TNY256 is constant, the power delivered is proportional to the primary inductance of the transformer and is relatively independent of the input voltage. Therefore, the design of the power supply involves calculating the primary inductance of the transformer for the maximum power required. If the TNY256 is appropriately chosen for the

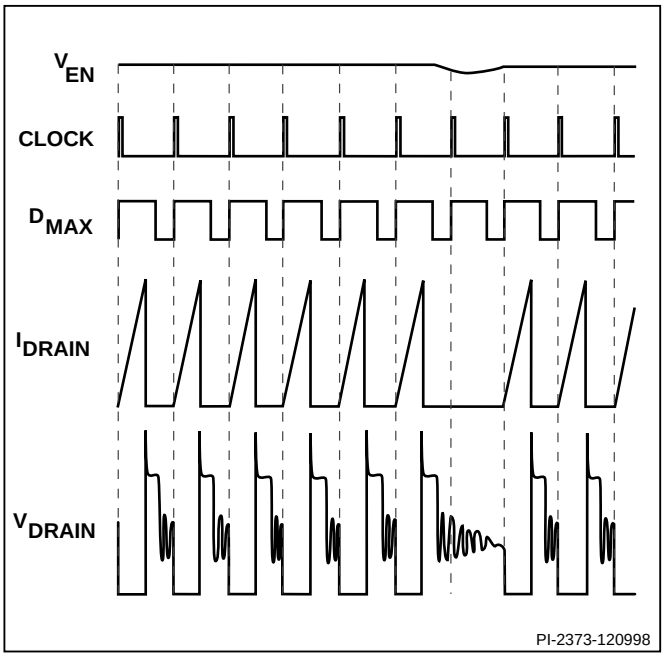


Figure 6. TNY256 Operation at Heavy Load.

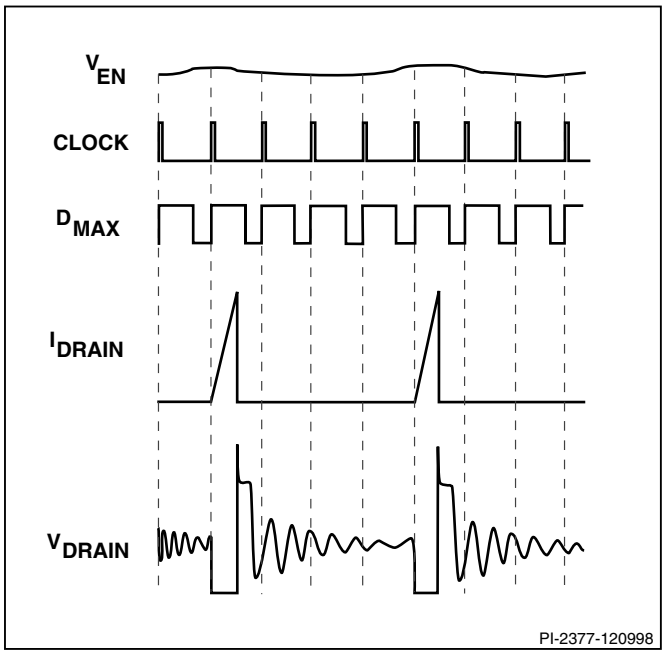


Figure 7. TNY256 Operation at Light Load.

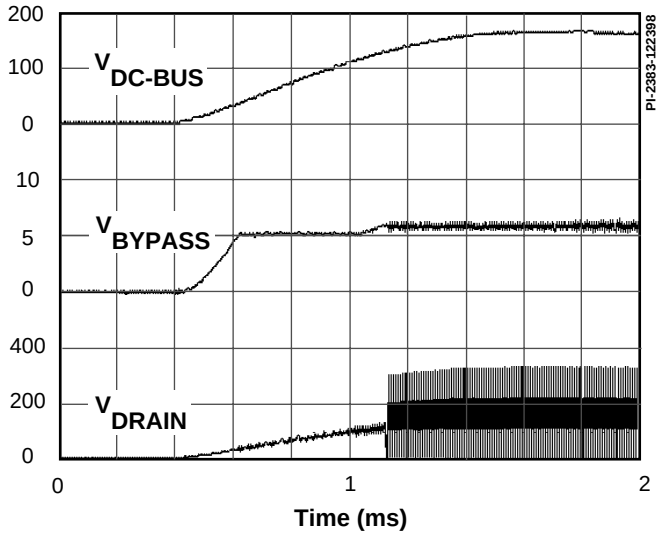


Figure 8. TNY256 Power-up With External Resistor (2 MΩ) Connected to EN/UV Pin.

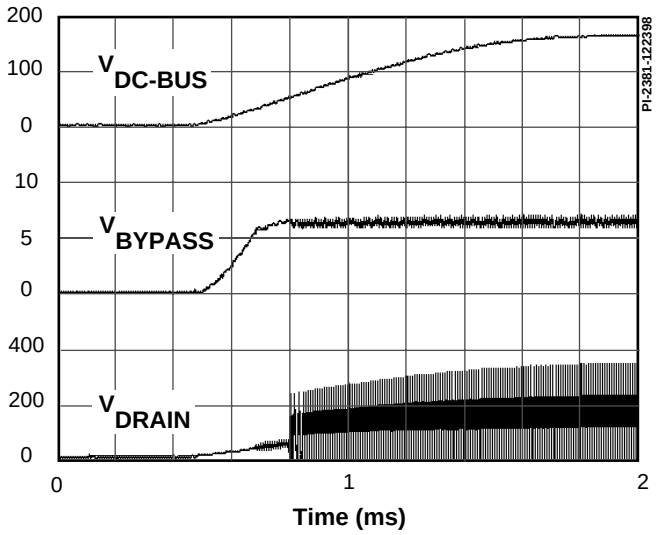


Figure 9. TNY256 Power-up Without External Resistor Connected to EN/UV Pin.

power level at the lowest input voltage, the calculated inductance will ramp up the current to the current limit before the DC_{MAX} limit is reached.

Enable Function

TNY256 senses the EN/UV pin to determine whether or not to proceed with the next switch cycle as described earlier. Once a cycle is started, it always completes the cycle (even when the EN/UV pin changes state half way through the cycle). This operation results in a power supply whose output voltage ripple is determined by the output capacitor, amount of energy per switch cycle and the delay of the feedback.

The EN/UV pin signal is generated on the secondary by comparing the power supply output voltage with a reference voltage. The EN/UV pin signal is high when the power supply output voltage is less than the reference voltage.

In a typical implementation, the EN/UV pin is driven by an optocoupler. The collector of the optocoupler transistor is connected to the EN/UV pin and the emitter is connected to the SOURCE pin. The optocoupler LED is connected in series with a Zener across the DC output voltage to be regulated. When the output voltage exceeds the target regulation voltage level (optocoupler diode voltage drop plus Zener voltage), the optocoupler diode will start to conduct, pulling the EN/UV pin low. The Zener can be replaced by a TL431 device for improved accuracy.

The EN/UV pin pull-down current threshold is nominally 50 µA, but is set to 40 µA the instant the threshold is exceeded. This is reset back to 50 µA when the EN/UV pull-down current drops below the current threshold of 40 µA.

ON/OFF Control

The internal clock of the TNY256 runs all the time. At the beginning of each clock cycle, it samples the EN/UV pin to decide whether or not to implement a switch cycle. If the EN/UV pin is high (< 40 µA), then a switching cycle takes place. If the EN/UV pin is low (greater than 50 µA) then no switching cycle occurs, and the EN/UV pin status is sampled again at the start of the subsequent clock cycle.

At full load, TNY256 will conduct during the majority of its clock cycles (Figure6). At loads less than full load, it will "skip" more cycles in order to maintain voltage regulation at the secondary output. At light load or no load, almost all cycles will be skipped (Figure7). A small percentage of cycles will conduct to support the power consumption of the power supply.

The response time of the TNY256 ON/OFF control scheme is very fast compared to normal PWM control. This provides tight regulation and excellent transient response.

Power Up/Down

The TNY256 requires only a 0.1 µF capacitor on the BYPASS pin. Because of the small size of this capacitor, the power-up delay is kept to an absolute minimum, typically 0.3 ms. Due to the fast nature of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor (2 MΩ) is connected to the EN/UV pin, the power MOSFET switching will be delayed during power-up until the DC line voltage exceeds the threshold (100 V). Figures 8 and 9 illustrate the power-up timing waveform of TNY256 in applications with and without an external resistor (2 MΩ) connected to the EN/UV pin.

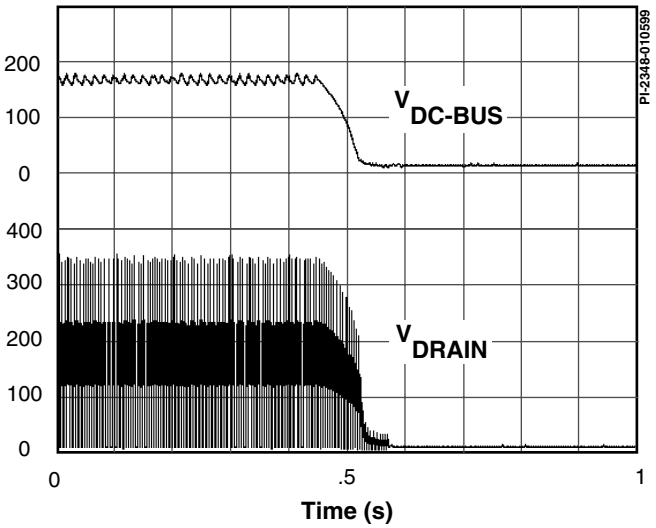


Figure 10. Normal Power-down Timing.

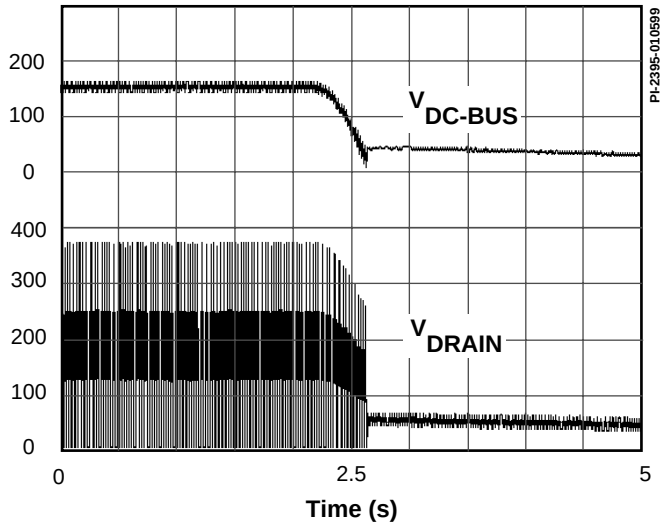


Figure 11. Slow Power-down Timing with External (2 MΩ) Resistor Connected to EN/UV Pin.

During power-down, when an external resistor is used, the power MOSFET will switch for 32 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the under-voltage function prohibits restarts when the line voltage is low.

Figure 10 illustrates a typical power-down timing waveform of TNY256. Figure 11 illustrates a very slow power-down timing waveform of TNY256 as in standby applications. The external resistor (2 MΩ) is connected to the EN/UV pin in this case to prevent restarts.

The TNY256 does not require a bias winding to provide power to the chip, because it draws the power directly from the DRAIN pin (see Functional Description above). This has two main benefits. First, for a nominal application, this eliminates the cost of an extra bias winding and associated components. Secondly, for charger applications, the current-voltage characteristic often allows the output voltage to fall to low values while still delivering power. This type of application normally requires a forward-bias winding which has many more associated components, none of which are necessary with the TNY256.

Current Limit Operation

Each switching cycle is terminated when the DRAIN current reaches the current limit of the TNY256. For a given primary inductance and input voltage, the duty cycle is constant. However, the duty cycle does change inversely with the input voltage providing “voltage feed-forward” advantages: good line ripple rejection and relatively constant power delivery independent of the input voltage.

BYPASS Pin Capacitor

The BYPASS pin uses a small 0.1 µF ceramic capacitor for decoupling the internal power supply of the TNY256.

Application Example

The TNY256 is ideal for low cost, high efficiency power supplies in a wide range of applications such as PC standby, cellular phone chargers, AC adapters, motor control, appliance control and ISDN network termination. The 130kHz operation allows the use of a low cost EE16 core transformer while still providing good efficiency. The frequency jitter in TNY256 makes it possible to use a single inductor (or two small resistors if lower efficiency is acceptable) in conjunction with two input capacitors for input EMI filtering up to the 10W level. The auto-restart function allows the design to be optimized for maximum efficiency without consideration for short-circuit current on the secondary. For applications requiring under-voltage lockout (UVLO), the TNY256 eliminates several components and saves cost.

As an example, Figure12 shows a 9V, 0.6A, AC adapter operating from a universal input range (85-265VAC). The AC input is rectified and filtered by D1-D4, C1 and C2 to create a high voltage DC bus which is connected to T1. Inductor L1 forms a pi-filter in conjunction with C1 and C2. The resistor R1 damps resonance in inductor L1. The frequency jitter in TNY256 allows it to meet worldwide conducted EMI standards using a simple pi-filter in combination with a small value Y1-capacitor C5 and a shield winding between primary and secondary windings inside transformer T1. Diode D5, capacitor C3 and resistor R3 form an RCD clamp circuit that limits the turn-off voltage spike to a safe value on the TNY256 DRAIN pin.

The secondary winding is rectified and filtered by D6, C6 and C7 to provide the 9V output. Additional filtering is provided by L3 and C8. The output voltage is determined by the resistor network R7 and R8. Resistor R9 maintains a bias current

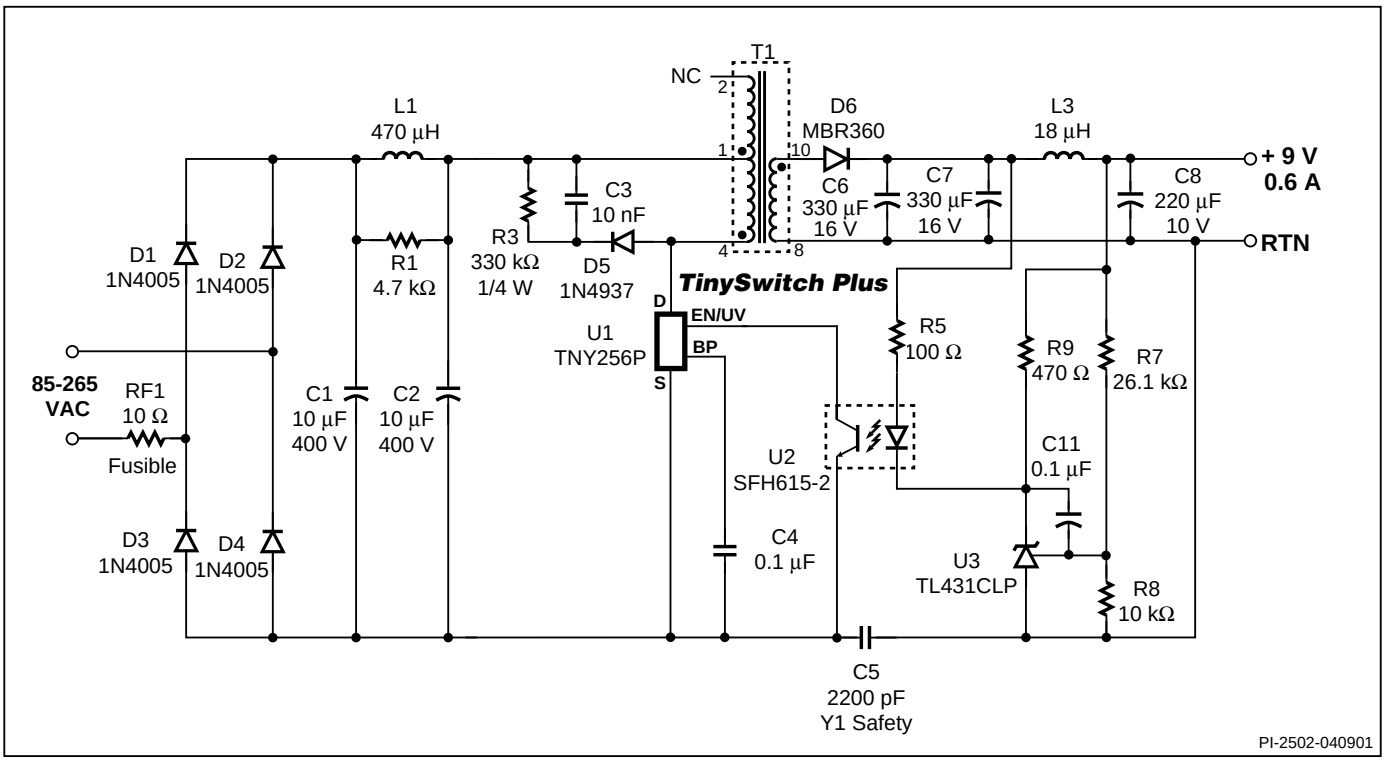


Figure 12. 5.5 W AC Adapter with Universal Input (85-265 VAC).

through the TL431 voltage reference for proper regulation. Capacitor C11 bypasses the TL431 response for improved ripple performance. Resistor R5 determines the AC gain of the circuit.

Key Application Considerations

For the most up to date information visit our Web site at: *www.powerint.com*

Design

Output Power

Table 1 shows the practical maximum continuous output power levels obtainable under following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input or 240 V or higher for 230VAC input or 115 VAC input with a voltage doubler. This corresponds to a filter capacitor of 3 µF/W for universal input and 1 µF/W for 230 or 115 VAC w/doubler input.

2. A secondary output of 5 V with a Schottky rectifier diode.

3. The P and G packaged parts are board mounted with source pins soldered to sufficient area of copper and the Y packaged parts are heat sinked sufficiently to keep the die temperature at or below 100 °C.

The maximum power capability of *TinySwitch* in a given application depends on the thermal environment (sealed enclosure, ventilated, open frame, etc.,), transformer core size and design (continuous or discontinuous), efficiency required, minimum specified input voltage, input storage capacitance, output voltage, output diode forward drop, etc., and can be different from the values shown in Table 1.

Audible Noise

At loads other than maximum load, the cycle skipping mode operation used in *TinySwitch* can generate audio frequency components in the transformer. This can cause the transformer to produce audio noise. Transformer audible noise can be reduced by using appropriate transformer construction techniques and decreasing the peak flux density. For more information on audio suppression techniques, please check the Application Notes section on our Web site at ***www.powerint.com***.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp and snubber circuits, can also generate audio noise due to electrostriction and piezo-electric effects. If this is the case, replacing them with a capacitor having a different type of dielectric is the simplest solution. Polyester film capacitors and ceramic capacitors with dielectrics such as NPO or X7R are good alternatives.

Layout

Single Point Grounding
Use a single point ground connection at the SOURCE pin for the BYPASS pin capacitor and the Input Filter Capacitor (see Figure 13).

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and *TinySwitch* together, should be kept as small as possible.

Primary Clamp Circuit
A clamp or snubber circuit is used to minimize peak voltage and ringing on the DRAIN pin at turn-off. This can be achieved by using an RC snubber for less than 3 W or an RCD clamp as shown in Figure 13 for higher power. A Zener and diode clamp across the primary or a single 550 V Zener clamp from DRAIN to SOURCE can also be used. In all cases care should be taken to minimize the circuit path from the snubber/clamp components to the transformer and *TinySwitch*.

Thermal Considerations
Copper underneath the *TinySwitch* acts not only as a single point ground, but also as a heatsink. The hatched area shown in Figure13 should be maximized for good heat-sinking of *TinySwitch* and output diode.

EN/UV pin layout optimization
The EN/UV pin connection to the opto-coupler should be kept to an absolute minimum (less than 0.5 in.), and this connection should be kept away from the DRAIN pin (minimum of 0.2 in.). These distance limitations are critical only in applications where an external under-voltage resistor (2 MΩ) is not used.

Y-Capacitor
The placement of the Y-capacitor should be directly from the primary single point ground to the common/return terminal on the secondary side. Such placement will maximize the EMI benefit of the Y-capacitor.

Optocoupler
It is important to maintain the minimum circuit path from the optocoupler transistor to the *TinySwitch* EN/UV and SOURCE pins to minimize noise coupling.

Output Diode
For best performance, the area of the loop connecting the secondary winding, the Output Diode and the Output Filter Capacitor, should be minimized. See Figure13 for optimized layout. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode to adequately heatsink the diode under output short circuit conditions.

Input and Output Filter Capacitors
There are constrictions in the traces connected to the input and output filter capacitors. These constrictions are present for two reasons. The first is to force all the high frequency currents to flow through the capacitor (if the trace were wide then it could flow around the capacitor). Secondly, the constrictions minimize the heat transferred from the *TinySwitch* to the input filter capacitor and from the secondary diode to the output filter capacitor. The common/return (the negative output terminal in Figure13) terminal of the output filter capacitor should be connected with a short, low resistance path to the secondary winding. In addition, the common/return output connection should be taken directly from the secondary winding pin and not from the Y-capacitor connection point.

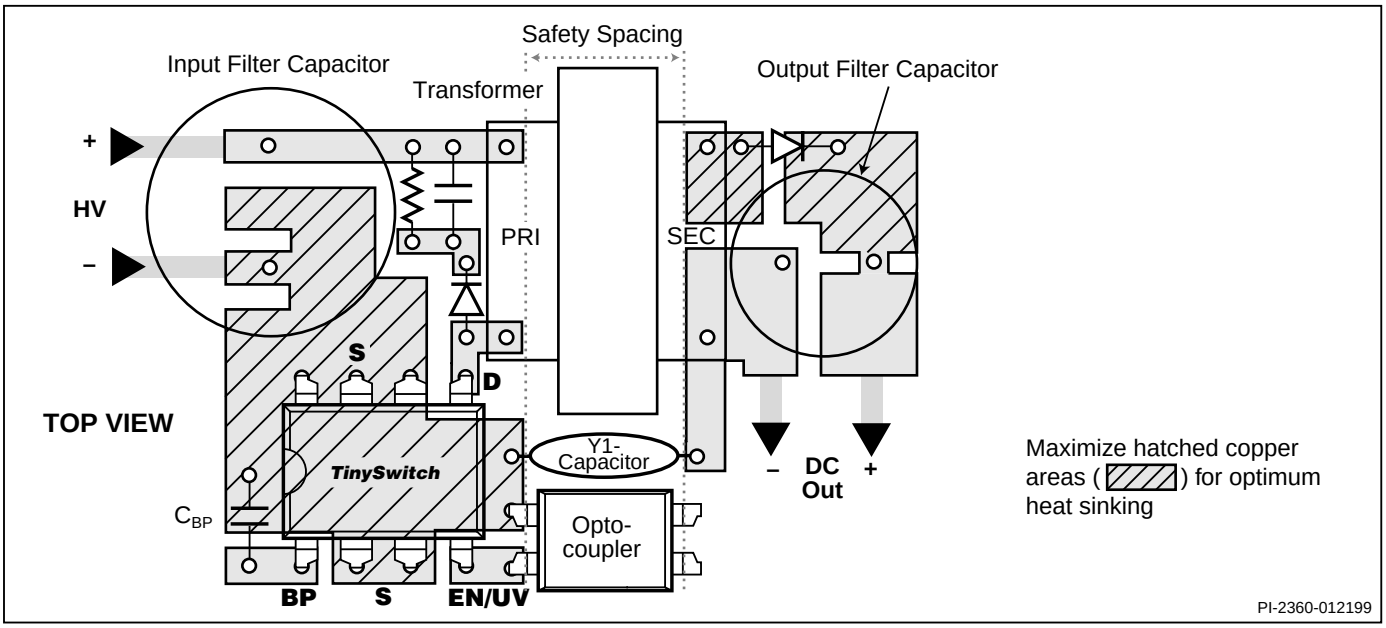


Figure 13. Recommended PC Layout for TinySwitch without Under-Voltage Lock Out Resistor.

ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... - 0.3 V to 700 V
Peak DRAIN Current ..... 800 mA
EN/UV Voltage ..... - 0.3 V to 9 V
EN/UV Current ..... 100 mA
BYPASS Voltage ..... -0.3 V to 9 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature(2) ..... -40 to 150 °C
Lead Temperature(3) ..... 260 °C

1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

THERMAL IMPEDANCE

Thermal Impedance: Y Package (θ_{JA})(1) ..... 70 °C/W
(θ_{JC})(2) ..... 2 °C/W
P/G Package:
(θ_{JA}) ..... 45 °C/W(3); 35 °C/W(4)
(θ_{JC})(2) ..... 11 °C/W

1. Free standing with no heatsink.
2. Measured at tab closest to plastic interface or source pin.
3. Soldered to 0.36 sq. inch (232mm^2), 2oz (610 gm/m^2) copper clad.
4. Soldered to 1 sq. inch (645mm^2), 2oz. (610 gm/m^2) copper clad

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 14 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	T_J = 25 °C See Figure 4	Average	115	130	140	kHz
			Peak-Peak Jitter	3.8	5.0	6.2	
Maximum Duty Cycle	DC_{MAX}	S1 Open		63	66	69	%
EN/UV Pin Turnoff Threshold Current	I_{DIS}	T_J = -40 °C to 125 °C		-68	-50	-28	µA
		T_J = 125 °C		-68	-52	-41	
EN/UV Pin Hysteresis Current	I_{HYS}	See Note A		-15	-10	-5	µA
EN/UV Pin Voltage	V_{EN}	$I_{EN/UV}$ = -25 µA		1.10	1.45	1.80	V
		$I_{EN/UV}$ = 25 µA		1.85	2.70	3.25	
EN/UV Short-Circuit Current	I_{ENSC}	$V_{EN/UV}$ = 0 V, T_J = -40 °C to 125 °C		-58	-40	-25	µA
		$V_{EN/UV}$ = 0 V, T_J = 125 °C		-58	-45	-35	
DRAIN Supply Current	I_{S1}	$V_{EN/UV}$ = 0 V (MOSFET Not Switching) See Note B			170	215	µA
	I_{S2}	EN/UV Open (MOSFET Switching) See Note B, C			255	300	µA
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C See Note D, E		-7.50	-5.50	-3.75	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C See Note D, E		-6.00	-4.10	-2.25	mA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 14 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS (cont.)							
BYPASS Pin Voltage	V_{BP}	See Note D		5.60	5.85	6.10	V
BYPASS Hysteresis	V_{BPH}			0.60	0.72	0.85	V
EN/UV Pin Line Under-voltage Threshold	I_{LUV}	T_J = 25 °C		44	50	55	µA
CIRCUIT PROTECTION							
Current Limit	I_{LIMIT}	di/dt = 120 mA/µs, T_J = 25 °C See Note F		450	500	550	mA
Initial Current Limit	I_{INIT}	See Figure 17 T_J = 25 °C		0.65 x $I_{LIMIT(MIN)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note H		170	215		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C See Note H, I			100	150	ns
Thermal Shutdown Temperature				125	135	145	°C
Thermal Shutdown Hysteresis					70		°C
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 50 mA	T_J = 25 °C		15.6	18.0	Ω
			T_J = 100 °C		25.7	30.0	
OFF-State Leakage	I_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, V_{DS} = 560 V, T_J = 125 °C				50	µA
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, I_{DS} = 100 µA, T_J = 25 °C		700			V
Rise Time	t_R	Measured in a Typical Flyback Converter Application.			50		ns
Fall Time	t_F				50		ns

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 14 (Unless Otherwise Specified)	Min	Typ	Max	Units
OUTPUT (cont.)						
DRAIN Supply Voltage			50			V
Output EN/UV Delay	$t_{EN/UV}$	See Note H			10	µs
Output Disable Setup Time	t_{DST}			0.5		µs
Auto-Restart ON-Time	t_{AR}	T_j = 25 °C See Note I	28.9	32.0	35.2	ms
Auto-Restart Duty Cycle	DC_{AR}		16	20	24	%

NOTES:

A. For a threshold with a negative value, negative hysteresis is a decrease in magnitude of the corresponding threshold.

B. Total current consumption is the sum of I_{S1} and I_{DSS} when EN/UV pin is shorted to ground (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when EN/UV pin is open (MOSFET switching).

C. Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 6.2 V.

D. BYPASS pin is not intended for sourcing supply current to external circuitry.

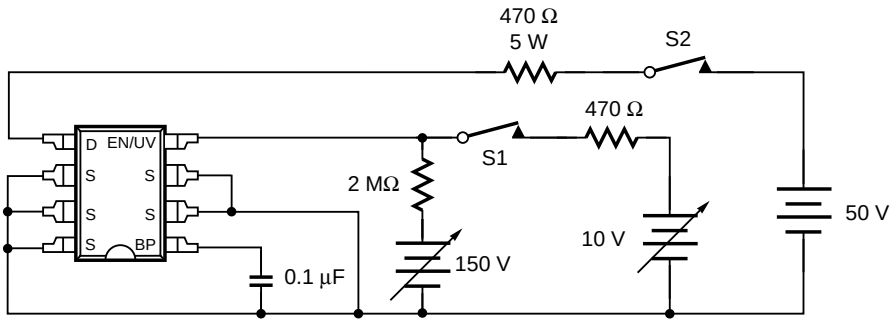
E. See typical performance characteristics section for BYPASS pin start-up charging waveform.

F. For current limit at other di/dt values, refer to current limit vs. di/dt curve under typical performance characteristics.

G. This parameter is derived from characterization.

H. This parameter is derived from the change in current limit measured at 5X and 10X of the di/dt shown in the I_{LIMIT} specification.

I. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).



NOTE: This test circuit is not applicable for current limit or output characteristic measurements.

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Figure 14. TinySwitch General Test Circuit.

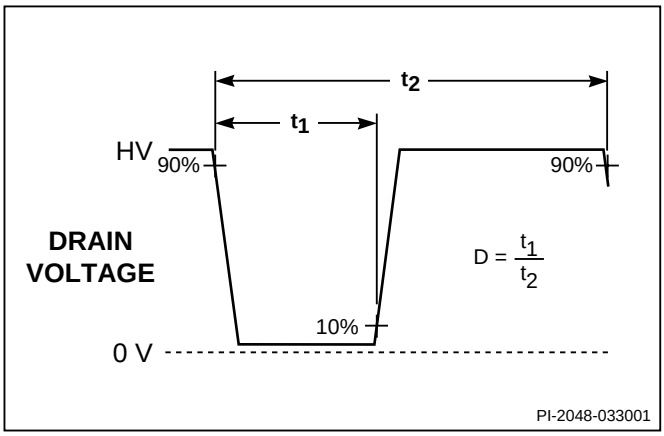


Figure 15. TinySwitch Duty Cycle Measurement.

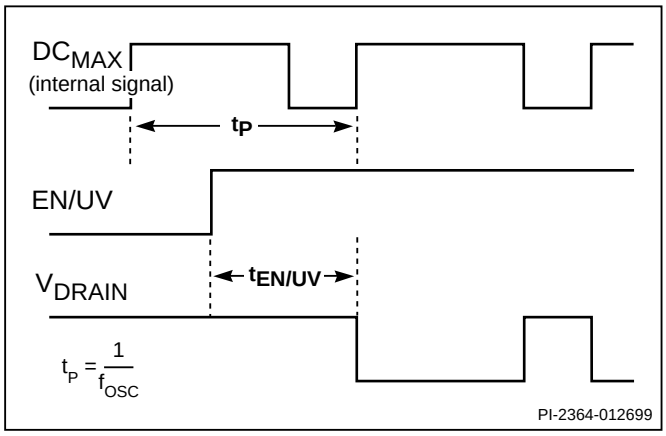


Figure 16. TinySwitch Output Enable Timing.

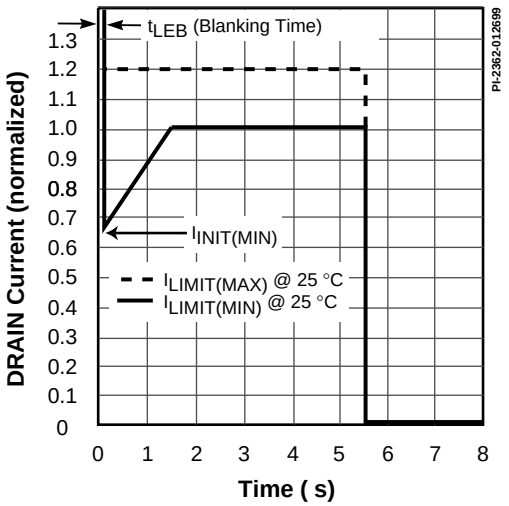
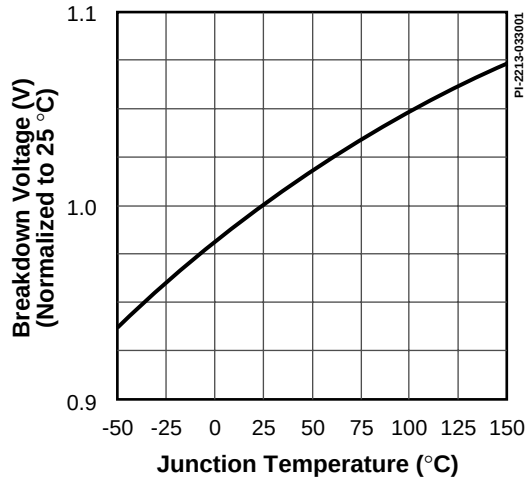


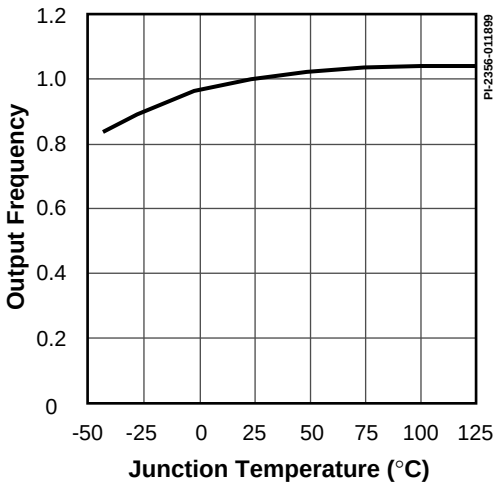
Figure 17. Current Limit Envelope.

Typical Performance Characteristics

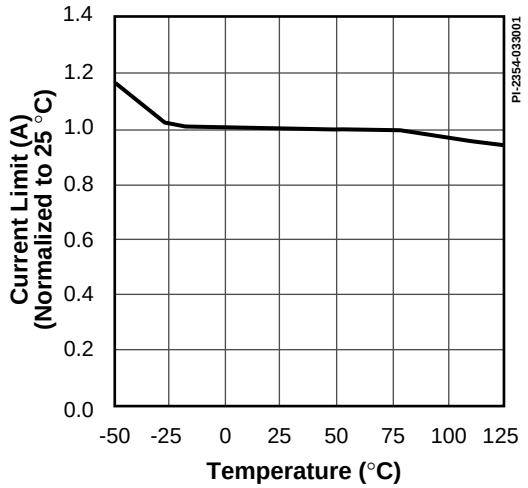
BREAKDOWN vs. TEMPERATURE



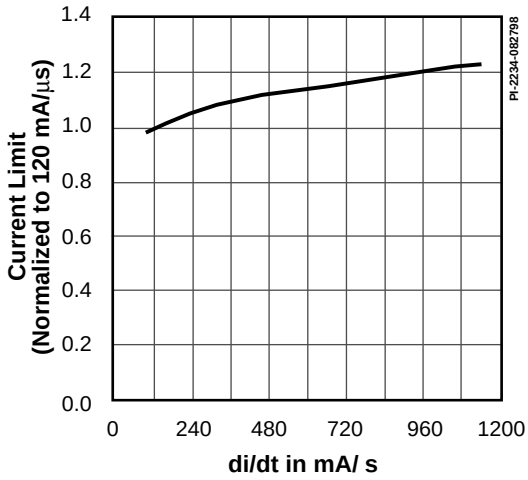
FREQUENCY vs. TEMPERATURE



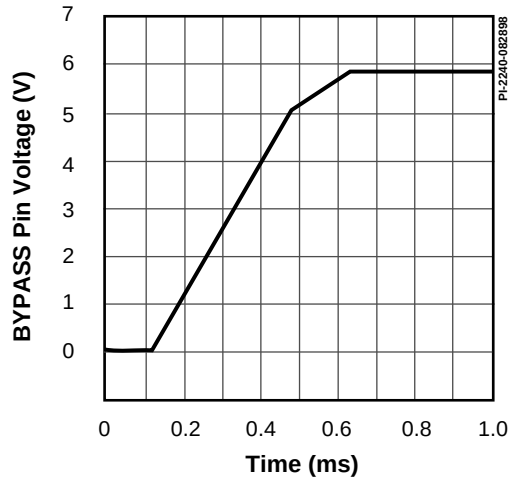
CURRENT LIMIT vs. TEMPERATURE



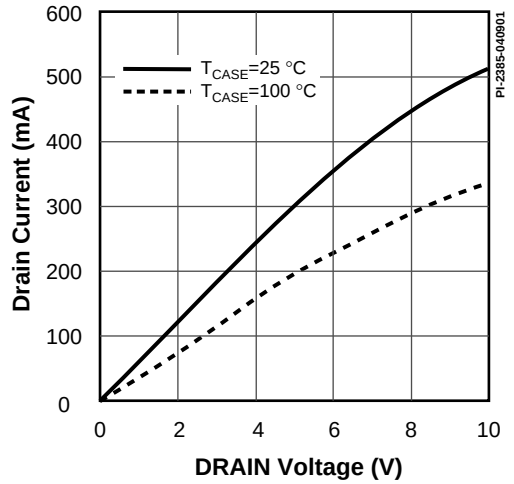
CURRENT LIMIT vs. di/dt



BYPASS PIN START-UP WAVEFORM

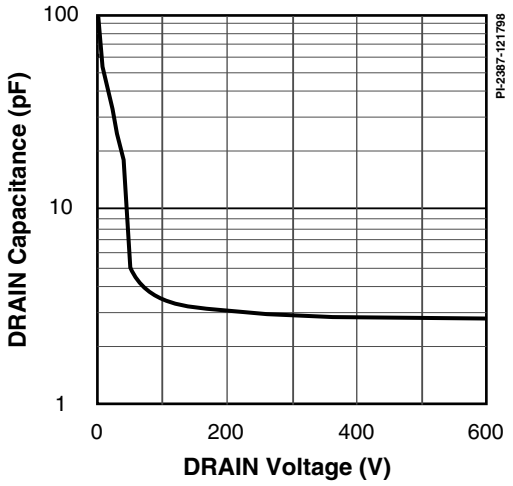


OUTPUT CHARACTERISTIC

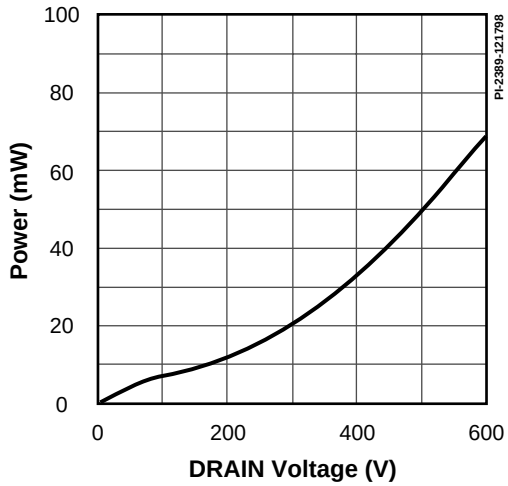


Typical Performance Characteristics (cont.)

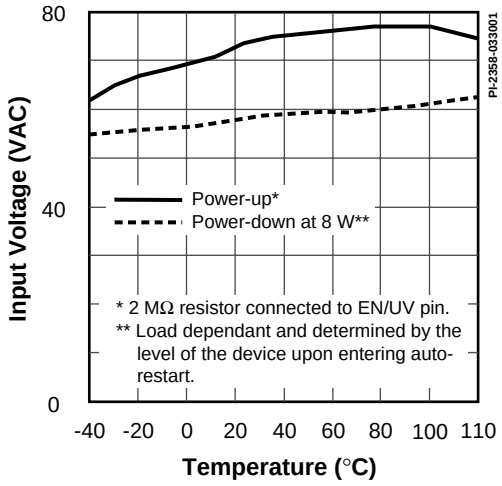
C_{OSS} vs. DRAIN VOLTAGE



DRAIN CAPACITANCE POWER



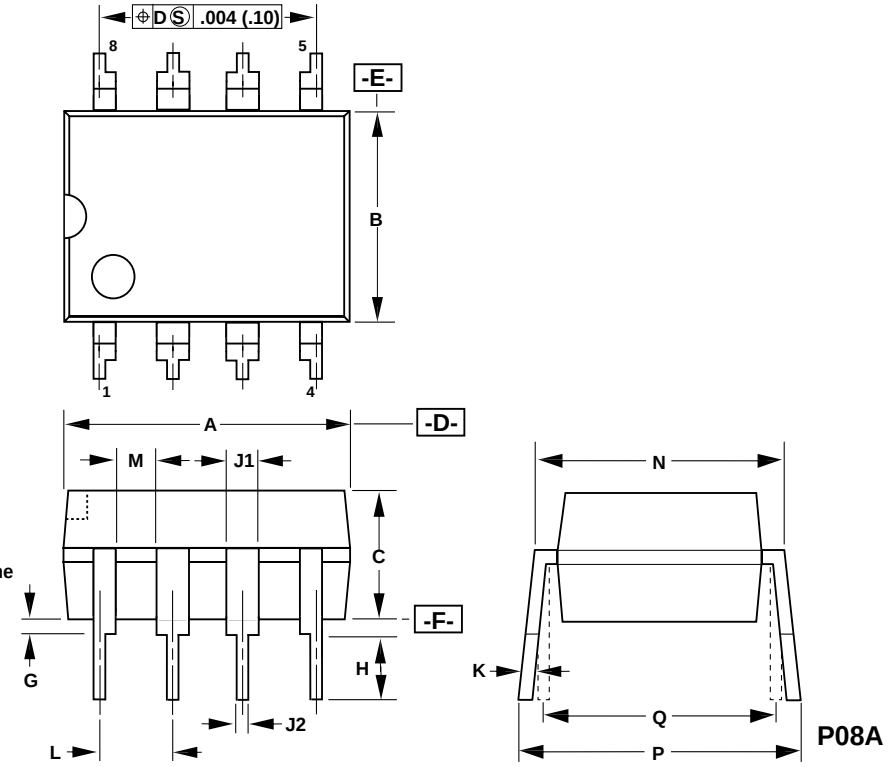
UNDERVOLTAGE THRESHOLD



DIP-8

DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.015-0.040	0.38-1.02
H	0.120-0.135	3.05-3.43
J1	0.060 (NOM)	1.52 (NOM)
J2	0.014-0.022	0.36-0.56
K	0.010-0.012	0.25-0.30
L	0.090-0.110	2.29-2.79
M	0.030 (MIN)	0.76 (MIN)
N	0.300-0.320	7.62-8.13
P	0.300-0.390	7.62-9.91
Q	0.300 BSC	7.62 BSC

Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.



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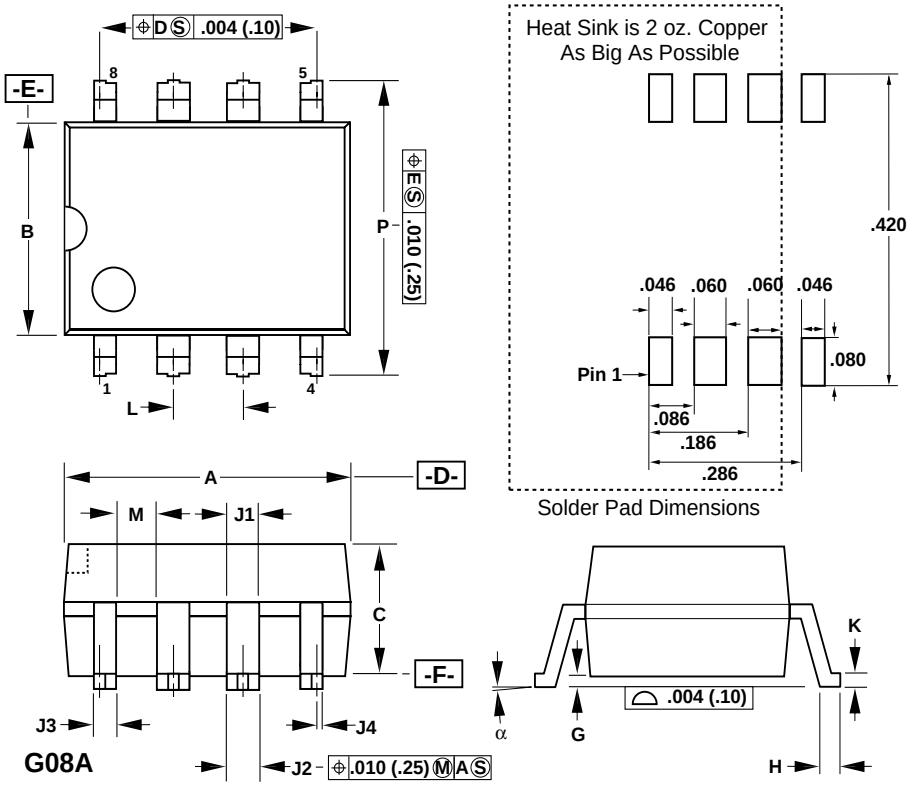
SMD-8



DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.004-0.012	0.10-0.30
H	0.036-0.044	0.91-1.12
J1	0.060 (NOM)	1.52 (NOM)
J2	0.048-0.053	1.22-1.35
J3	0.032-0.037	0.81-0.94
J4	0.007-0.011	0.18-0.28
K	0.010-0.012	0.25-0.30
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
P	0.372-0.388	9.45-9.86
α	0-8°	0-8°

Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (issue B, 7/85) except for lead shape and size.
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.

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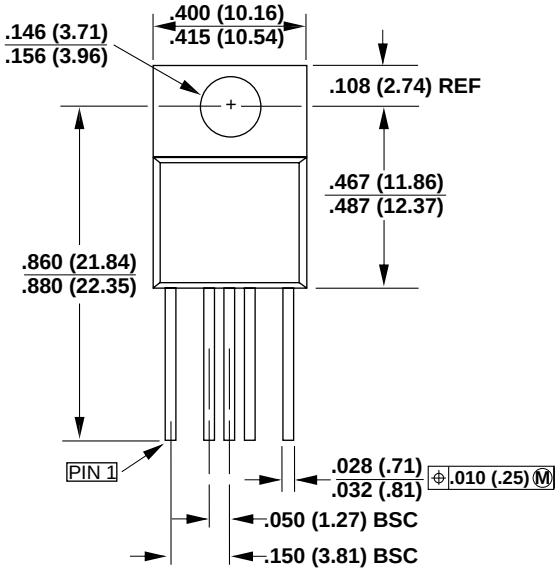
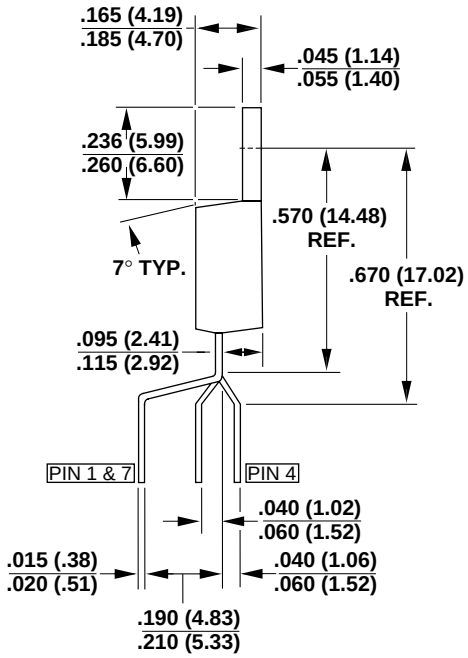
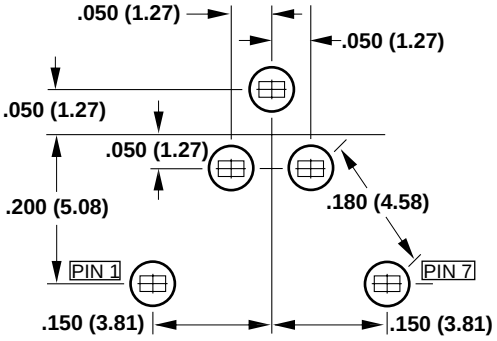
TO-220-7B







Y07B

MOUNTING HOLE PATTERN

Notes:

1. **Controlling dimensions are inches. Millimeter dimensions are shown in parentheses.**
2. **Pin locations start with Pin 1, and continue from left to right when viewed from the front. Pins 2 and 6 are omitted.**
3. **Dimensions do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15mm) on any side.**
4. **Minimum metal to metal spacing at the package body for omitted pin locations is .068 inch (1.73 mm).**
5. **Position of the formed leads to be measured at the mounting plane, .670 inch (17.02 mm) below the hole center.**
6. **All terminals are solder plated.**

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Notes

Notes

Notes

Revision	Notes	Date
A	-	3/99
B	1) TO-220-7B package information added. 2) I_{LUV} minimum increased to 44 µA to reflect production improvements.	8/99
C	1) Updated package references. 2) Corrected spelling. 3) Added Omega symbol (2 MΩ on pg. 8). 4) Corrected storage temperature and θ_{JC} and updated nomenclature in parameter table. 5) Corrected spacing and font sizes in figures.	7/01

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