FAIRCHILD SEMICONDUCTOR®

December 2009

SG5842A/SG5842JA — Highly Integrated Green-Mode PWM Controller

Features

- Green-Mode PWM Controller
- Low Startup Current: 14μA
- Low Operating Current: 4mA
- Programmable PWM Frequency with Hopping (SG5842JA)
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Synchronized Slope Compensation
- Leading-Edge Blanking (LEB)
- Constant Output Power Limit
- Totem-Pole Output with Soft Driving
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Internal Latch Circuit (OTP, OVP)
- Internal Open-Loop Protection
- V_{DD} Under-Voltage Lockout (UVLO)
- GATE Output Maximum Voltage Clamp: 18V

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Notebook Power Adapters
- Open-Frame SMPS

Description

The highly integrated SG5842A/JA series of PWM controllers provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. To further reduce power consumption, SG5842A/JA is manufactured using the BiCMOS process. This allows a low startup current, around 14μA, and an operating current of only 4mA. As a result, a large startup resistance can be used.

The SG5842A/JA built-in synchronized slope compensation achieves stable peak-current-mode control. SG5842JA integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters.

SG5842A/JA provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur. PWM output is disabled until V_{DD} drops below the UVLO lower limit, then the controller starts again. As long as V_{DD} exceeds about 24V, the internal OVP circuit is triggered. An external NTC thermistor can be applied for over-temperature protection.

SG5842A/JA is available in an 8-pin DIP or SOP package.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	OTP Latch	OVP Latch	Frequency Hopping
SG5842JASZ	-40°C to +105°C	RoHS	8-Pin Small Outline Package (SOP)	Yes	Yes	Yes
SG5842JADZ	-40°C to +105°C	RoHS	8-Pin Dual Inline Package (DIP)	Yes	Yes	Yes
SG5842JASY	-40°C to +105°C	Green	8-Pin Small Outline Package (SOP)	Yes	Yes	Yes
SG5842ASZ (Preliminary)	-40°C to +105°C	RoHS	8-Pin Small Outline Package (SOP)	Yes	Yes	No
SG5842ASY (Preliminary)	-40°C to +105°C	Green	8-Pin Small Outline Package (SOP)	Yes	Yes	No

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

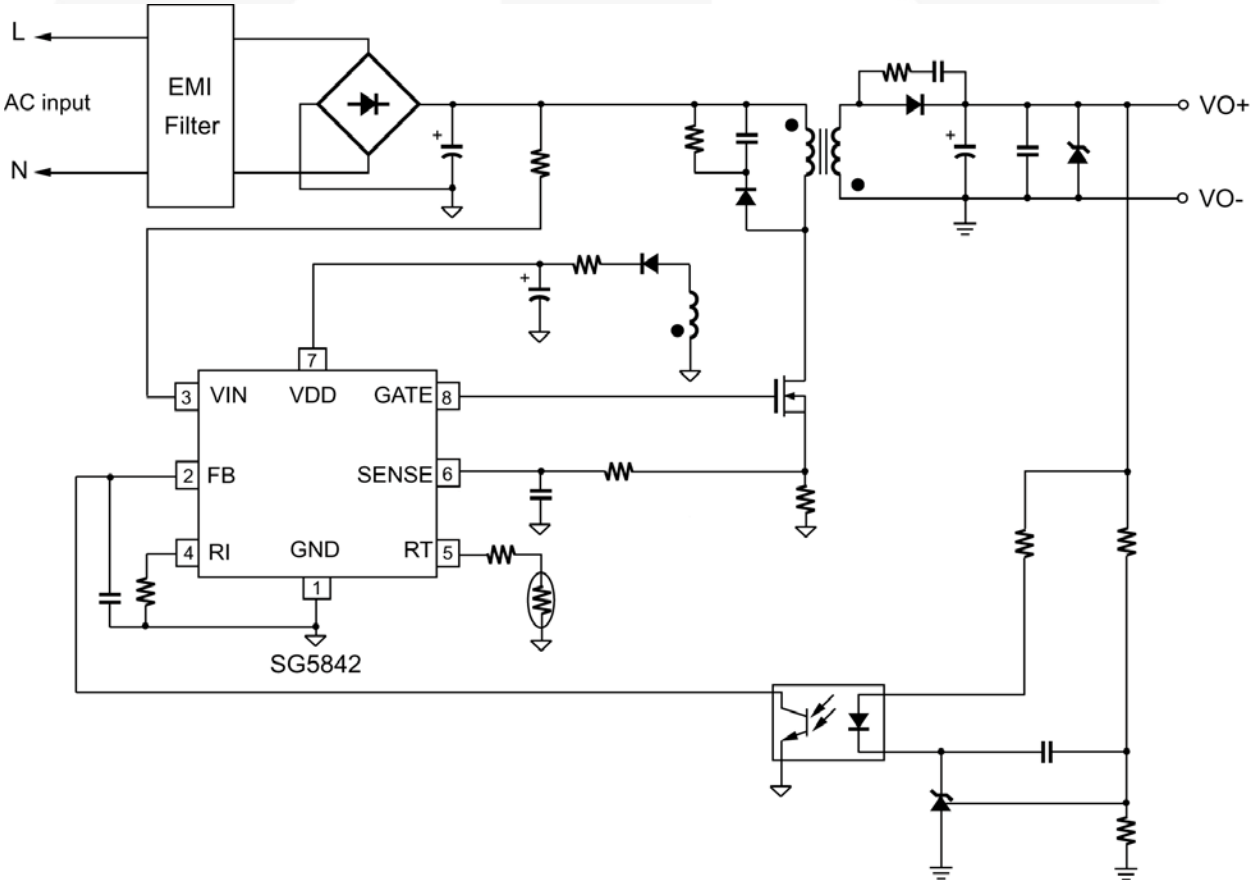


Figure 1. Application Diagram

Block Diagram

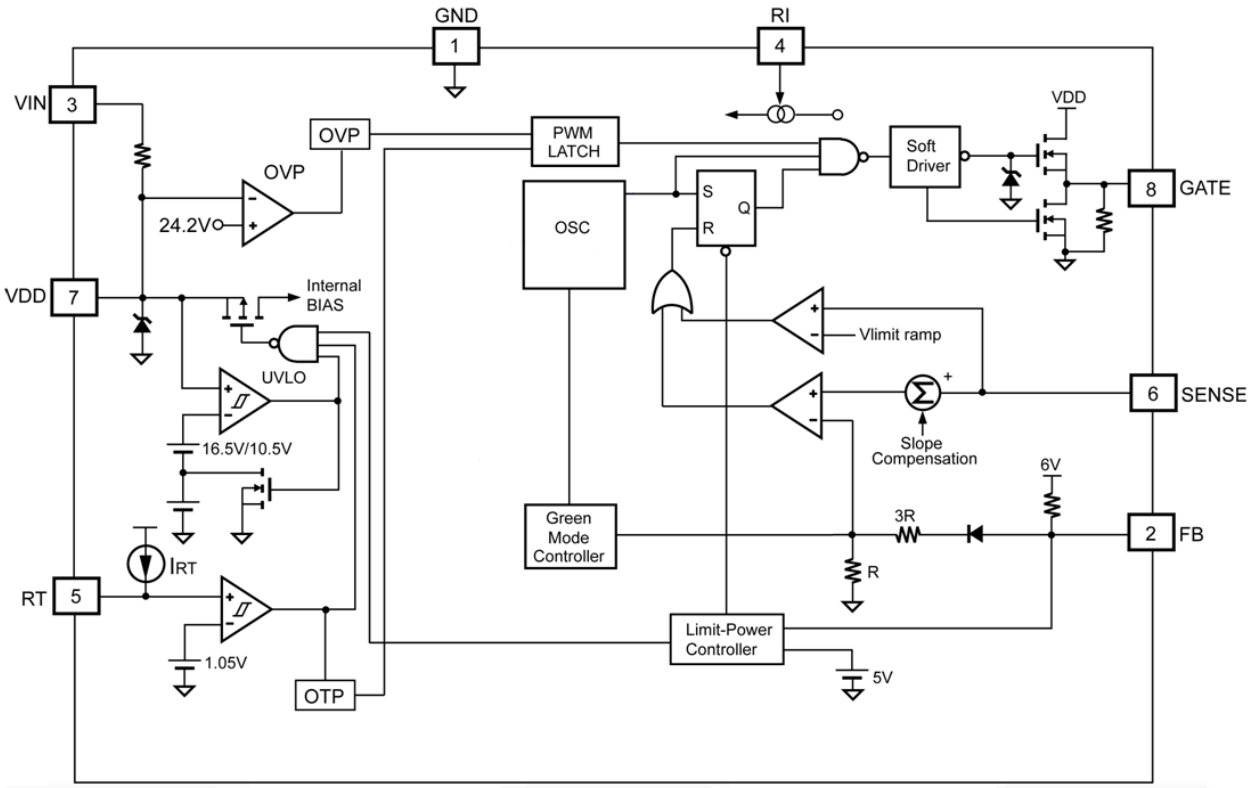
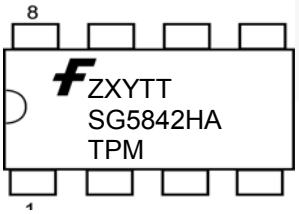


Figure 2. Function Block Diagram

Marking Information

Marking for SG5842JASZ (pb-free)
Marking for SG5842JADZ (pb-free)
Marking for SG5842ASZ (pb-free)
Marking for SG5842ADZ (pb-free)

H: J = with Frequency Hopping
Null = without Frequency Hopping
T: D = DIP, S = SOP
P: Z = Lead Free
Null = Regular Package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location



Marking for SG5842JASY (green-compound)
Marking for SG5842ASY (green-compound)

F- Fairchild Logo
Z- Plant Code
X- 1 Digit Year Code
Y- 1 Digit week Code
TT: 2 Digits Die Run Code
T: Package Type (S=SOP, D=DIP)
P: Y: Green Package
M: Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

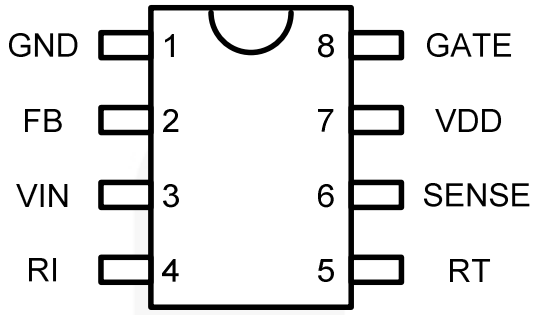


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	Ground
2	FB	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal from this pin and the current-sense signal from Pin 6. If FB voltage exceeds the threshold, the internal protection circuit disables PWM output after a predetermined delay time.
3	VIN	For startup, this pin is pulled HIGH to the rectified line input via a resistor. Since the startup current requirement is very small, a large startup resistance can be used to minimize power loss.
4	RI	A resistor connected from the RI pin to GND provides a constant current source. This determines the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor results in a 65KHz center PWM frequency.
5	RT	For over-temperature protection. An external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a fixed limit, PWM output is latched off.
6	SENSE	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power supply. The internal protection circuit disables PWM output if V_{DD} is over-voltage.
8	GATE	The totem-pole output driver for the power MOSFET, which is internally clamped below 18V.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.		Unit
V_{VDD}	Supply Voltage[1]			30		V
V_{VIN}	Input Terminal			30		V
V_{FB}	Input Voltage to FB Pin		-0.3	7.0		V
V_{SENSE}	Input Voltage to SENSE Pin		-0.3	7.0		V
V_{RT}	Input Voltage to RT Pin		-0.3	7.0		V
V_{RI}	Input Voltage to RI Pin		-0.3	7.0		V
P_D	Power Dissipation (T_A < 50°C)			DIP	800	mW
				SOP	400	
Θ_{JA}	Thermal Resistance (Junction-to-Air)			DIP	82.5	°C/W
				SOP	141	
T_J	Operating Junction Temperature		-40	+125		°C
T_{STG}	Storage Temperature Range		-55	+150		°C
T_L	Lead Temperature (Wave Soldering or Infrared, 10 Seconds)			+260		°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		3		KV
		Charged Device Model, JESD22-C101		1		

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-20	+85	°C

Electrical Characteristics

V_{DD}=15V and T_J=T_A= -40~125°C, unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Section							
V_{DD-OP}	Continuously Operating Voltage					20	V
V_{DD-ON}	Start Threshold Voltage			15.5	16.5	17.5	V
V_{DD-OFF}	Minimum Operation Voltage			9.5	10.5	11.5	V
I_{DD-ST}	Startup Current		V_{DD}=V_{DD-ON}–0.16V		14	30	μA
I_{DD-OP}	Operating Supply Current		V_{DD}=15V, R_I=26KΩ, GATE=OPEN		4	5	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection			23.2	24.2	25.2	V
t_{D-OVP}	V_{DD} Over-Voltage Protection Debounce Time		R_I=26KΩ		100		μs
I_{DD-H}	Holding Current After OVP/OTP Latchup		V_{DD}=5V	40.0	52.5	65.0	μA
RI Section							
RI_{NOR}	R_I Operating Range			15.5		36.0	KΩ
RI_{MAX}	Maximum R_I Value for Protection				230		KΩ
RI_{MIN}	Minimum R_I Value for Protection				10		KΩ
Oscillator Section							
f_{OSC}	Normal PWM Frequency	Center Frequency	R_I=26KΩ	62	65	68	KHz
		Hopping Range	R_I=26KΩ SG5842JA Only	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period		R_I=26KΩ SG5842JA Only	3.9	4.4	4.9	ms
f_{OSC-G}	Green-Mode Minimum Frequency		R_I=26KΩ	18	22	25	KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=11.5V to 20V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A=-20 to 85°C			5	%
Feedback Input Section							
A_V	FB Input to Current Comparator Attenuation			1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Input Impedance			4		7	KΩ
$V_{FB-OPEN}$	Output High Voltage		FB Pin Open	5.5			V
V_{FB-OLP}	FB Open-Loop Trigger Level			5.0		5.4	V
t_{D-OLP}	FB Open-Loop Protection Delay		R_I=26KΩ	50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage		R_I=26KΩ	1.9	2.1	2.3	V
V_{FB-G}	Green-Mode Ending FB Voltage		R_I=26KΩ		V_{FB-N}-0.5		V

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}= 15V and T_J=T_A= -40~125°C, unless otherwise noted.

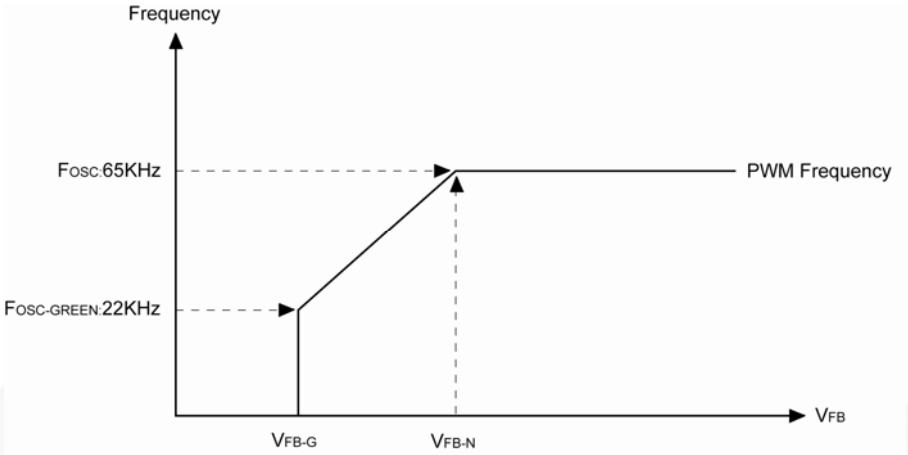


Figure 5. V_{FB} vs. PWM Frequency

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Current Sense Section						
Z_{SENSE}	Input Impedance			12		KΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage		0.85	0.90	0.95	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL}–V_{STHVA}		0.22		V
DCY_{SAW}	Duty Cycle of SAW Limit	Maximum Duty Cycle		45		%
t_{PD}	Propagation Delay to GATE Output	R_I=26KΩ		150	200	ns
t_{LEB}	Leading-Edge Blanking Time	R_I=26KΩ	200	270	350	ns
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		60	65	70	%
V_{GATE-L}	Output Voltage Low	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=12.5V, I_O=-50mA	7.5			V
t_r	Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
t_f	Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
I_O	Peak Output Current	V_{DD}=15V, GATE=6V	230			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=20V		18	19	V
RT Section						
I_{RT}	Output Current of RT Pin	R_I=26KΩ	67	70	73	μA
V_{RTTH}	Over-Temperature Protection Threshold Voltage		1.015	1.050	1.085	V
t_{D-OTP}	Over-Temperature Debounce	R_I=26KΩ	60	100	140	μs

Performance Characteristics

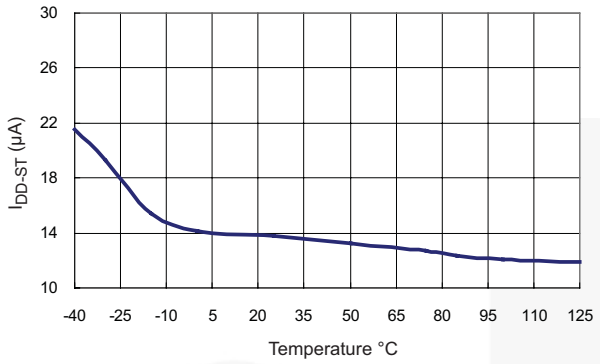


Figure 6. Startup Current (I_{DD-ST}) vs. Temperature

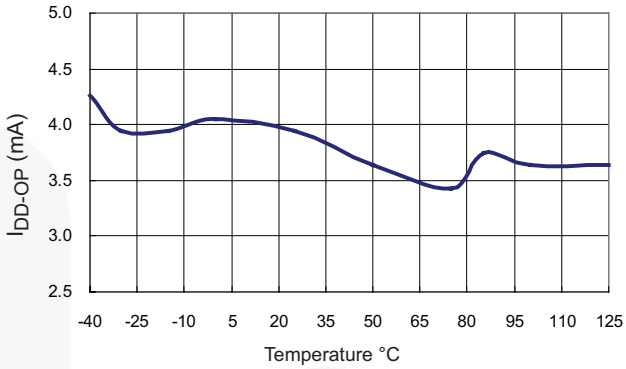


Figure 7. Operating Supply Current (I_{DD-OP}) vs. Temperature

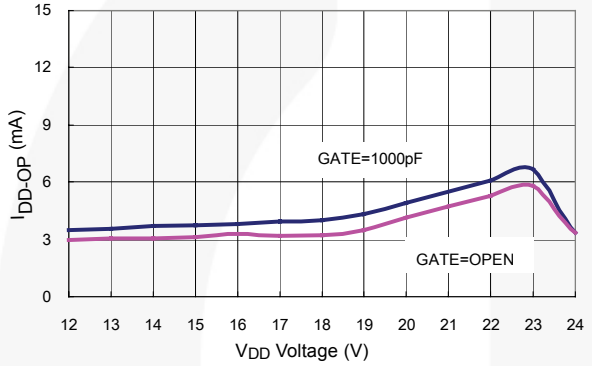


Figure 8. Operation Current (I_{DD-OP}) vs. V_{DD} Operation

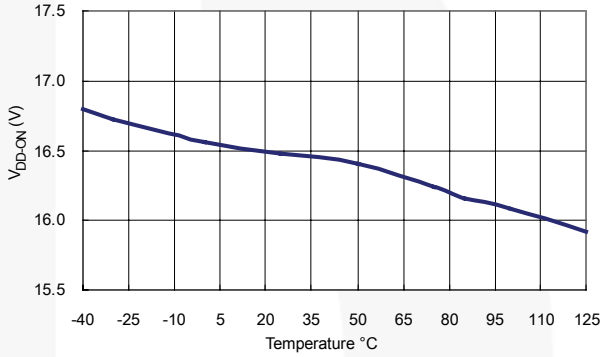


Figure 9. Start Threshold (V_{DD-ON}) vs. Temperature

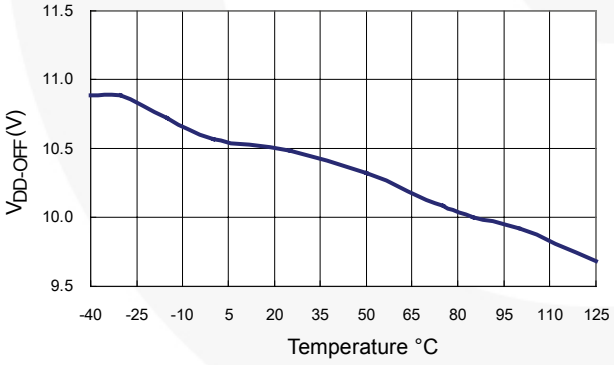


Figure 10. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

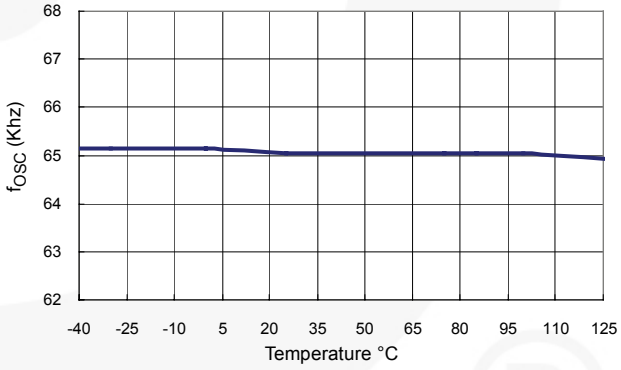


Figure 11. PWM Frequency (f_{OSC}) vs. Temperature

Performance Characteristics (Continued)

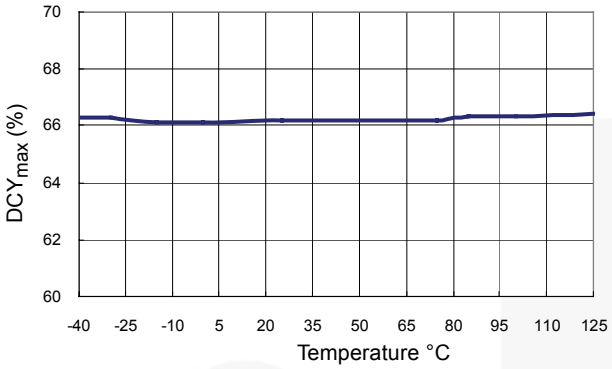


Figure 12. Maximum Duty Cycle (DCY_{max}) vs. Temperature

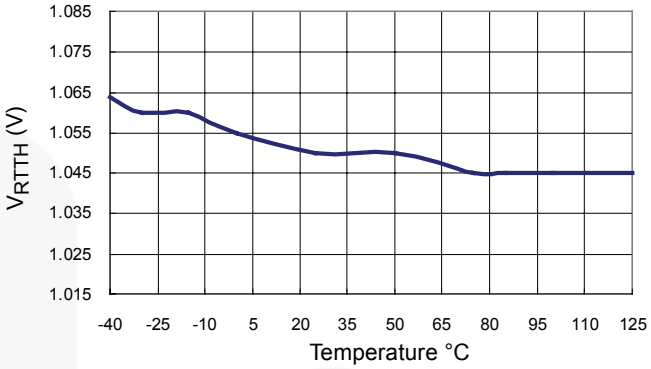


Figure 13. Trigger Voltage for Over-Temperature Protection (V_{RTTH}) vs. Temperature

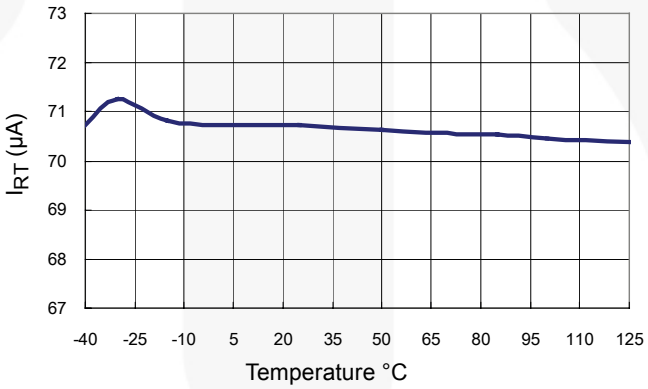


Figure 14. Output Current of RT Pin (I_{RT}) vs. Temperature

Functional Description

Startup Current

The typical startup current is only 14μA, which allows a high-resistance, low-wattage startup resistor to be used to minimize power loss. A 1.5MΩ/0.25W startup resistor and a 10μF/25V V_{DD} hold-up capacitor are sufficient for an AC/DC adapter with a universal input range.

Operating Current

The required operating current has been reduced to 4mA. This results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to continuously decrease the PWM frequency under light-load conditions. To avoid acoustic noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using this controller can meet even the strictest international standby power regulations.

Oscillator Operation

A resistor connected from the RI pin to the GND pin generates a constant current source for the controller. This current is used to determine the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor, R_I, results in a corresponding 65KHz PWM frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (K\Omega)} (KHz) \qquad (1)$$

The range of the PWM oscillation frequency is designed as 47KHz ~ 109KHz.

SG5842JA also integrates a frequency hopping function internally. The frequency variation ranges from around 62KHz to 68KHz for a center frequency of 65KHz. The frequency hopping function helps reduce EMI emission of a power supply with minimum line filters.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate drive.

Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 16.5V/10.5V. To enable a SG5842A/JA controller during startup, the hold-up capacitor must first be charged to 16.5V through the startup resistor.

The hold-up capacitor continues to supply V_{DD} before energy can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 10.5V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply V_{DD} during startup.

Gate Output / Soft Driving

The SG5842A/JA BiCMOS output stage is a fast totem-pole gate driver. Cross-conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET transistors from harmful over-voltage gate signals. A soft-driving waveform is implemented to minimize EMI.

Slope Compensation

The sensed voltage across the current sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. The built-in slope compensation function improves power supply stability and prevents peak-current-mode control from causing sub-harmonic oscillations. Within every switching cycle, the SG5842A/JA controller produces a positively sloped, synchronized ramp signal.

Constant Output Power Limit

When the SENSE voltage across the sense resistor, R_S, reaches the threshold voltage, around 0.85V; the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces additional current proportional to $t_{PD} \bullet V_{IN} / L_P$. The delay is nearly constant regardless of the input voltage $V_{IN.}$ Higher input voltage results in a larger additional current and the output power limit is higher than under low input line voltage. To compensate this variation for a wide AC input range, a sawtooth power-limiter (saw limiter) is designed to solve the unequal power-limit problem. The saw limiter is designed as a positive ramp signal (V_{LIMIT_RAMP}) fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection is built in to prevent damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over-voltage protection voltage ($V_{DD\text{-}OVP}$) and lasts for $t_{D\text{-}OVP}$, the PWM pulse is latched off. The PWM pulses stay latched off until the power supply is unplugged from the mains outlet.

Functional Description (Continued)

Limited Power Control

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, the supply voltage V_{DD} begins decreasing.

$$t_{D-OLP}\ (ms) = 2.154 \times R_I(K\Omega) \quad (2)$$

When V_{DD} goes below the turn-off threshold (eg. 10.5V), the controller is totally shut down. V_{DD} is charged up to the turn-on threshold voltage of 16.5V through the startup resistor until PWM output is restarted. This protection feature remains activated as long as the overloading condition persists. This prevents the power supply from overheating due to overloading conditions.

Protection Latch Circuit

The built-in latch function provides a versatile protection feature that does not require external components *(see ordering information for a detailed description)*. To reset the latch circuit, disconnect the AC line voltage of the power supply.

Thermal Protection

An external NTC thermistor can be connected from the RT pin to ground. A fixed current, I_{RT}, is sourced from the RT pin. Because the impedance of the NTC decreases at high temperatures, when the voltage of the RT pin drops below 1.05V, PWM output is latched off. The RT pin output current is related to the PWM frequency programming resistor R_I.

Noise Immunity

Noise from the current sense or the control signal may cause significant pulse width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoid long PCB traces and component leads. Compensation and filter components should be located near the SG5842A/JA. Increasing the power-MOS gate resistance is advised.

Reference Circuit

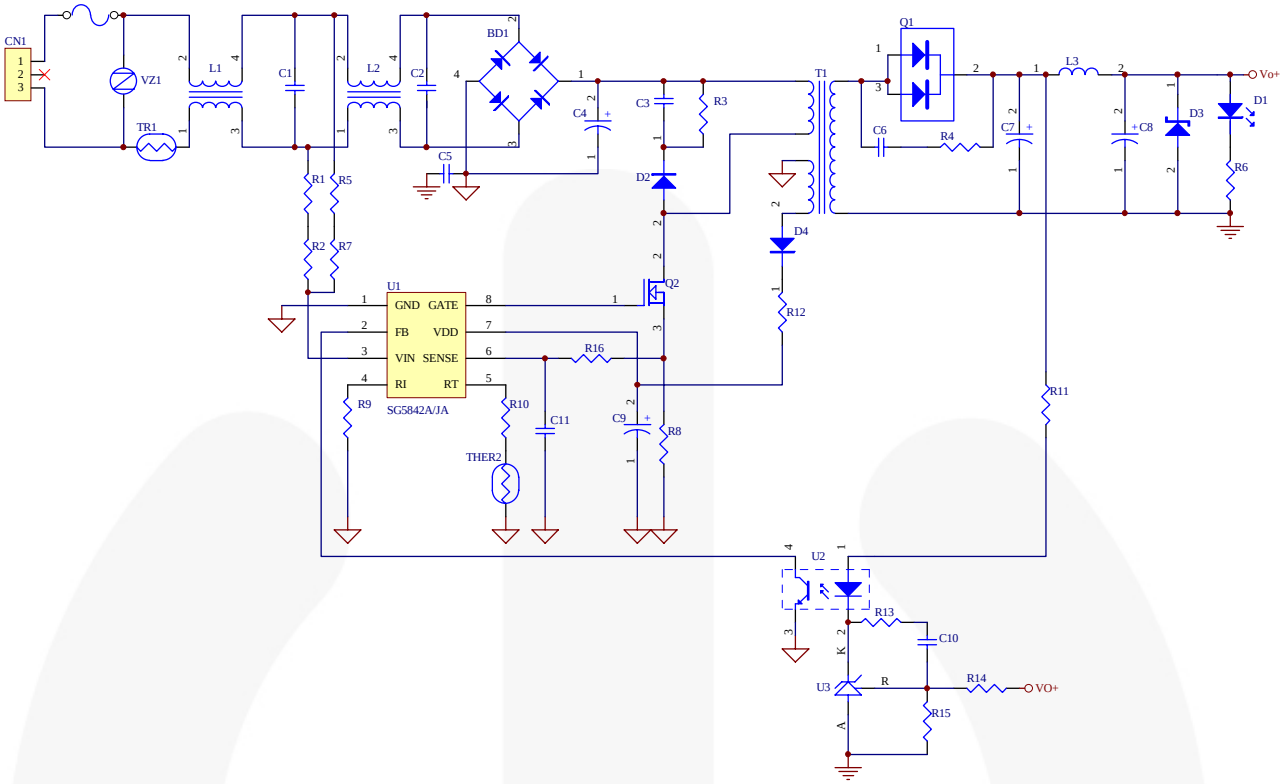


Figure 15. Reference Circuit

BOM

Reference	Component	Reference	Component
BD1	BD 4A/600V	Q2	MOS 7A/600V
C1	XC 0.68μF/300V	R1, R2, R5, R7	R 470KΩ 1/4W
C2	XC 0.1μF/300V	R3	R 100KΩ 1/2W
C3	CC 0.01μF/500V	R4	R 47Ω 1/4W
C4	EC 120μ/400V	R6	R 2KΩ 1/8W
C5	YC 222p/250V	R8	R 0.3Ω 2W
C6	CC 1000pF/100V	R9	R 33KΩ 1/8W
C7	EC 1000μF/25V	R10	R 4.7KΩ 1/8W
C8	EC 470μF/25V	R11	R 470Ω 1/8W
C9	EC 10μF/50V	R12	R 0Ω 1/8W
C10	CC 222pF/50V	R13	R 4.7KΩ 1/8W
C11	CC 470pF/50V	R14	R 154KΩ 1/8W 1%
D1	LED	R15	R 39KΩ 1/8W 1%
D2	Diode BYV95C	R16	R 100Ωm 1/8W
D3	TVS P6KE16A	THER2	Thermistor TTC104
D4	Diode FR103	T1	Transformer (600μH-PQ2620)
F1	FUSE 4A/250V	U1	IC SG5842A/JA
L1	Choke (900μH)	U2	IC PC817
L2	Choke (10mH)	U3	IC TL431
L3	Inductor (2μH)	VZ1	VZ 9G
Q1	Diode 20A/100V		

Physical Dimensions

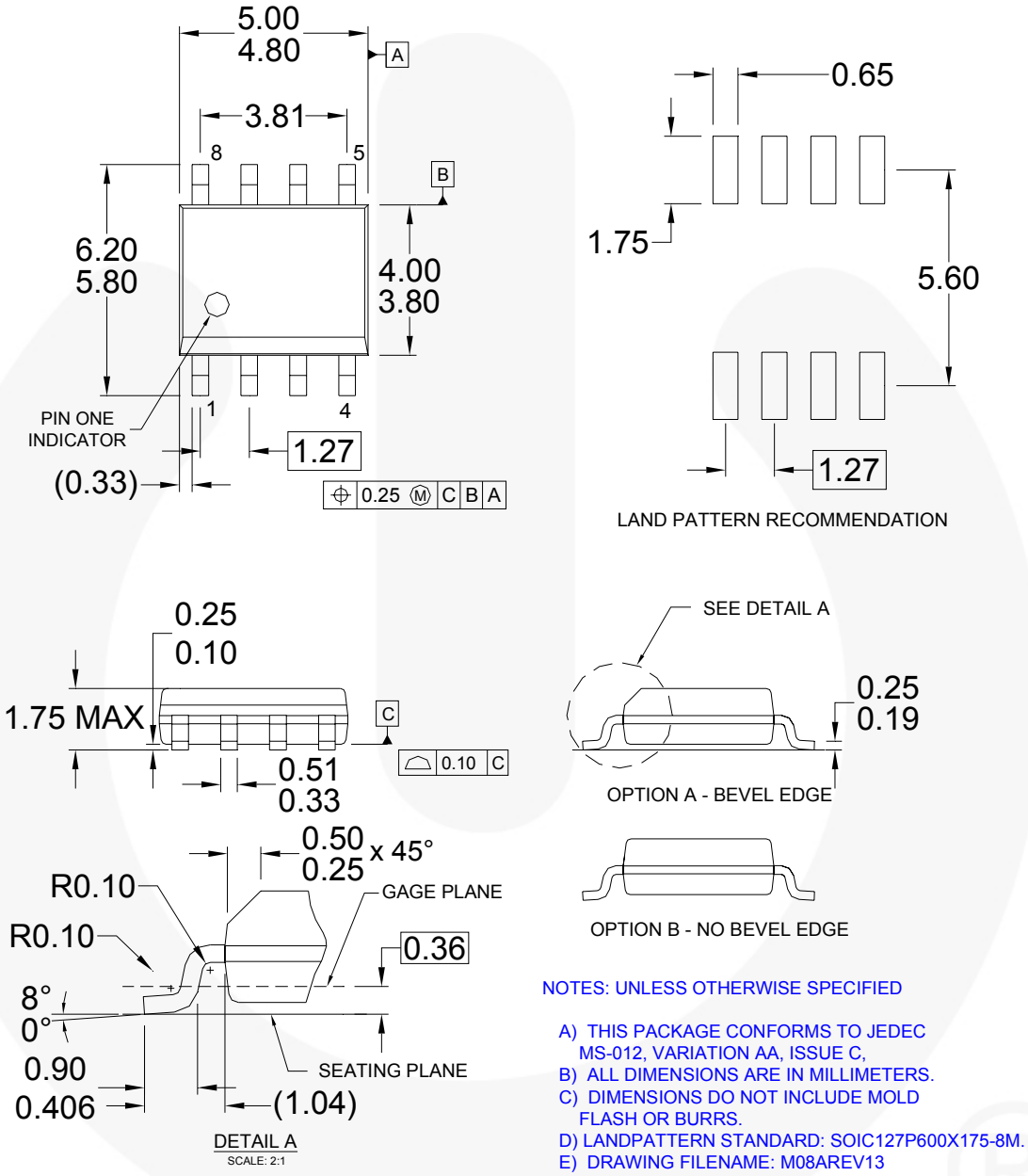
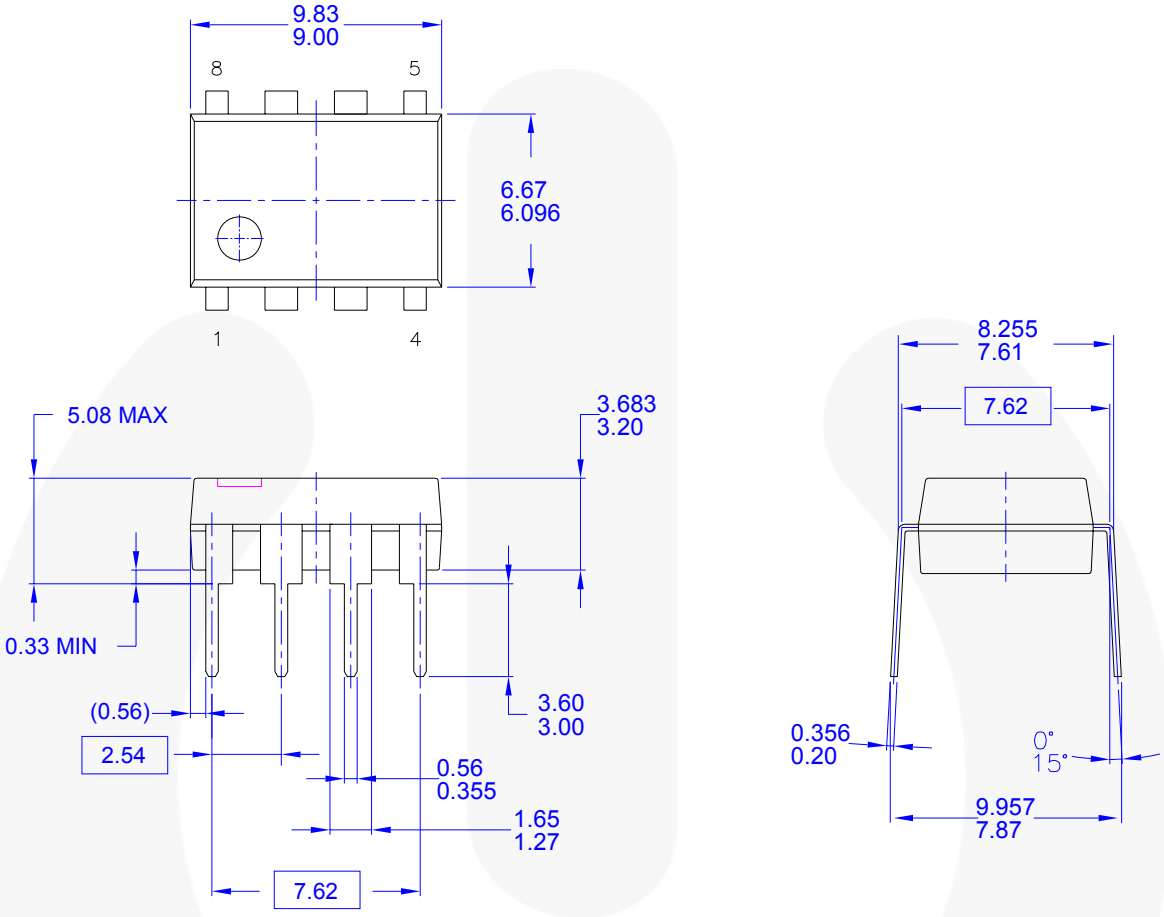


Figure 16. 8-Pin, Small Outline Package (SOP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

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Figure 17. 8-Pin, Dual Inline Package (DIP)

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